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Handbook
PREFERRED CIRCUITS
Navy Aeronautical Electronic Equipment

PREPARED BY
NATIONAL BUREAU OF STANDARDS
DEPARTMENT OF COMMERCE
FOR
BUREAU OF AERONAUTICS
DEPARTMENT OF THE NAVY

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PREFACE

This Preferred Circuits Manual has been prepared within the Engineering Electronics Section, Electricity and Electronics Division, of the National Bureau of Standards under the sponsorship of the Industrial Planning Division, Bureau of Aeronautics, Department of the Navy. Much of this material was first distributed in report form to obtain comment. The assistance, suggestions, and encouragement received from many segments of the electronics industry are gratefully acknowledged.

Those contributing directly to this publication are J. F. Brooks, E. J. Chapin, Jr., H. D. Cook, L. A. Marzetta, G. J. Rogers, S. Rubin, Sachio Saito, and M. Sigman. Credit is due R. J. Berry, M. R. Doggett, G. S. Ginsberg and M. C. Ryan for laboratory assistance. Drafting was capably performed by E. W. Duck, and editing by I. M. Reihm and K. M. Schwarz.

J. H. MUNCY
National Bureau of Standards

FOREWORD

The purpose of the Preferred Circuits Manual is to encourage better engineering practice in the design of circuits for military electronic equipment. The manual may be considered as a compilation of good design practice, not toward the limiting of effort in circuit design, but as a standard against which true progress in circuit design may be measured. Although there is no current plan for issuing a military specification covering its use, the employment of the Preferred Circuits Manual is recommended as a guide in designing Navy aeronautical equipment.

In the past, electronics engineering practice has been unique in the complete freedom of the circuit designer to choose his individual circuit elements with little regard to engineering already accomplished and proven. This lack of standardization was possible due to the availability of a vast choice of circuit elements and to the ease of correcting design errors in hand assembled production. However, with the advent of mechanical assembly, mechanized production and the prospect of automation of electronics production, it is becoming more and more necessary for designs to be reliable and frozen prior to production and subsequent field use. In the event of mobilization the man hours wasted in the analysis of poor performance and in the replacement of individual components during production testing and field maintenance will not be feasible when the quantities of electronic equipments produced by any method of machine manufacture are considered.

Preliminary studies sponsored by the Bureau of Aeronautics indicate that a high percentage of circuit functions are subject to standardization while still retaining the desired flexibility of equipment performance. For the military services such standardization will result in greater operational reliability, simpler maintenance training and procedures, shorter lead time on delivery of equipment, faster acceleration of production, more efficient use of engineers, lower original purchase prices of equipment, and fewer spare parts at field installations. For the equipment producer, standardization will result in lower production costs, quicker shifting of equipment from development to production phases, better conservation of scarce engineering manpower, and lower parts inventories.

The Navy is pleased to note the interest of many commercial groups in this program. Several manufacturers are offering packaged circuits for sale patterned after the circuits published in a preliminary edition of the manual. Other organizations have expressed their interest by utilizing the preliminary manual in forming company circuit standardization programs, in developing personnel training programs, in educational programs, or as a convenient technical reference. The heavy demand by industry for copies of the preliminary manual has made it advisable to make this formal printing available through the Government Printing Office.

The Preferred Circuits Manual is being prepared as an Industrial Preparedness Measure by a large and varied group in the engineering electronics laboratories of the National Bureau of Standards under the guidance and sponsorship of the Bureau of Aeronautics. As additional circuits are chosen, they will be issued through the Government Printing Office for inclusion in the manual.

The success of this circuit standardization program depends ultimately upon the active participation of the design engineer and equipment manufacturer in utilizing the circuits, in criticising material presently in the manual and in submitting improved or additional circuits for inclusion in the manual. Such material should be addressed to the Chief of the Bureau of Aeronautics (IP-43), Department of the Navy, Washington 25, D. C.

James S. Russell

CHIEF, BUREAU OF AERONAUTICS

INTRODUCTION

Standardization within United States industry has been obtained only through full discussion and agreement by all interested parties. In the field of military electronic equipment, this has not been possible, partially because of security.

The Industrial Planning Division of the Bureau of Aeronautics, Department of the Navy, requested the National Bureau of Standards to undertake a study and gather data to implement a program of circuit standardization. If standardization of electronic circuits can be achieved, even in part, considerable economies will result. These savings will include more economical utilization of engineering manpower in the development, production design and maintenance of equipment. Additionally, economies will accrue in equipment procurement and in spare parts distribution. Equipment reliability should also improve, since well-tried circuits would be used wherever possible. Such a program will in no way limit or retard progress because circuits of insufficient performance would not be used.

The name "preferred circuit" was chosen rather than "standard circuit" since a circuit cannot become a "standard" until is it widely adopted. Also "preferred" was adopted because the connotation that has been widely established from the several "preferred tube" lists is exactly the same as that meant here.

The "preferred circuits" of this manual are not offered as being considerably superior to available alternates or to other circuits that might be devised to replace them. Yet these preferred circuits represent, so to speak, a least-common-denominator, in that a large percentage of applications can be satisfactorily fulfilled by their employment. These preferred circuits have been derived on the basis of experimental measurements on a large number of examples taken from both commercial and military equipments and represent designs that are well stabilized. In almost all cases, similar circuits have been in use for at least 10 years with only very minor improvement.

The "preferred circuits" of this manual are not offered as definitive solutions. It is hoped that engineers will use this compilation as a convenient summary of the state of the art, and as a means of avoiding unnecessary diversification and design effort. This is a very loose form of standardization, but constitutes a step in the right direction.

The preferred circuits may seem to be needlessly complex for general application, particularly in regard to dependence upon negative supplies. Although for individual circuits the negative source might be eliminated, designers are universally employing negative supplies, as may be seen from the examples given in the Notes.

ORGANIZATION OF THE MANUAL

To achieve flexibility, the manual is arranged by preferred circuit numbers. The circuit is given first with its characteristics and other information enabling the engineer to select and construct the circuit. Successive pages carry a discussion, giving more information on use and design methods.

For the designer whose interest extends beyond an immediate design problem, the steps which led to each preferred circuit are summarized in Part 2, "Notes to the Preferred Circuits Manual." The several steps covered with varying emphasis are:

(1) Examples taken from an equipment survey.
(2) A brief discussion of major differences and similarities in the several examples.
(3) A summary of ranges of performance required.
(4) A presentation of design considerations too extensive to be included in the "Preferred Circuits Manual."

DIRECTIONS FOR USE

Within this manual there is no attempt to completely specify all component parts since the environment is usually the determining factor. In determining the values of resistors and capacitors, particular care should be taken. The values are given with a plus and minus limit that should not be confused with manufacturer's tolerance. The limit should be interpreted to include all the sources of change during the use of the circuit.

Among the choices left to the designer are:

(1) Choice of one out of several electrically equivalent tube types, reliability being the controlling factor.
(2) Resistor wattage rating, since ambient temperature is the controlling factor.
(3) Capacitor voltage rating, since ambient temperature is the controlling factor.
(4) Choice of configuration if several alternatives are offered.
(5) Choice of component values in some cases depending on functional parameter such as frequency.
(6) Choice of construction and assembly technique.

For information, the following partial listing of reliable tube types and their lower quality counterparts is included. Complete interchangeability is not implied. Such information is available from manufacturers' literature.

Preferred Type	*Prototype*
5654/6AK5W	6AK5
5670WA	2C51
5725/6AS6W	6AS6
5726/6AL5W	~~6AK5~~ 6AL5
5751WA	12AX7
5814WA	12AU7
6005/6AQ5W	6AQ5
6080WA	6AS7
6098/6AR6WA	6AR6

INTRODUCTION

In 1952 the Industrial Planning Division of the Bureau of Aeronautics (now integrated into the Bureau of Naval Weapons), Department of the Navy, requested the National Bureau of Standards to undertake a preliminary program leading toward electronic circuit standardization. This interest in circuit standardization was prompted by the increasing use of mechanized production of electronic equipment with the prospect of automatic production, and by the belief that the reliability of electronic equipment could be improved by the use of circuit designs which had been proven in field use. The life data accumulated from the increased use of these circuits would provide further basis for circuit improvements resulting in further increases in equipment reliability. Other advantages of circuit standardization are the more efficient utilization of scarce engineering manpower in the design, development, production, and maintenance of electronic equipment; economies in the production and procurement of equipment and spare parts; and improvements in spare parts distribution.

Preliminary studies indicated that a large percentage of the circuit functions could be standardized without adverse effect on equipment performance. The program of vacuum-tube circuit selection and testing which followed resulted in the publication of the Handbook Preferred Circuits in September 1955. The circuits in this handbook were derived on the basis of experimental measurements on a large number of examples taken from both commercial and military equipment, and represent designs that are well established. In almost all cases, similar circuits had been in use for at least 10 years with only minor improvements. Since publication of the Handbook, more vacuum-tube circuits which meet these same qualifications have been added by means of published supplements.

The success and acceptance of the vacuum-tube program led to the initiation of a similar program for transistor circuits. Transistor preferred circuits cannot be based on a large sampling of existing systems, because only a few transistorized equipments have seen extensive field service. Furthermore, since transistor circuits are undergoing constant improvement, transistor preferred circuits can be expected to become outdated and require replacement more frequently than vacuum-tube circuits. Nevertheless, many of the advantages outlined for the vacuum-tube preferred circuits apply as well to transistor preferred circuits. As a result, beginning with Supplement Number 1, transistor circuits have been included in the Preferred Circuits Manual. These circuits, which have been chosen from the functional circuit types whose design has become relatively stable, serve as a guide to current design practice and as a base against which improvement can be measured.

The name "preferred circuit" rather than "standard circuit" was chosen to take advantage of the connotation established by the publication of the several "preferred" lists of electronic components. Further, it was realized that a true standard can be obtained only through the combined efforts of all interested parties. The preferred circuits of this Manual, whether vacuum tube or transistor, represent, so to speak, a least-common-denominator, in that a large percentage of applications can be satisfactorily fulfilled by their employment. They are not offered as definitive solutions nor as being considerably superior to available alternates or to other circuits that might be devised

to replace them. It is hoped that engineers will use the preferred circuits as a convenient summary of the state of the art, and as a means of avoiding unnecessary diversification and design effort.

In the selection of circuits of mature design for inclusion in the Handbook Preferred Circuits, first preference has been given to circuit types which are applicable in many different types of electronic equipment. The preferred circuits are designed for tubes or transistors which appear on the appropriate military preferred list (MIL–STD–200 or MIL–STD–701). When regulated supply voltages are required, those specified in MIL–STD–706 [1] are used. Where possible, component values have been restricted to those appearing in MIL–STD–242C (NAVY).

No attempt has been made to completely specify all the components used in the preferred circuits, since such specifications must take into consideration the environment in which the circuit is expected to operate.[2] Instead, the nominal component values are specified, together with plus and minus limits. The specified performance is based on component values which remain within these limits during the time that the circuit is in operation. As used in the preferred circuits, the term "limits" includes the initial tolerance of the part and the drifts caused by environmental change, aging, or any other cause.

The preferred circuits are designed to operate as specified with any vacuum tube, transistor, crystal, or other critical component which is acceptable under the military specifications for its type. The performance specified for the circuit is generally based on "worst case" design. However, the performance is specified as realistically and in as much detail as possible, so that the designer who uses the statistical approach will have a basis for determining the relative effect of supply voltage and component characteristic changes.

In the design of the preferred circuits, every effort has been made to minimize the interaction between them; however, electronic circuits are not ideal building blocks. In particular, users of the Handbook Preferred Circuits are cautioned against the indiscriminate mixing of vacuum-tube and transistor circuits. The use of a transistor circuit to drive a vacuum-tube circuit usually presents no problem. The use of a vacuum-tube circuit to drive a transistor circuit, however, may lead to difficulties unless intermediate devices are used to facilitate the transition from the relatively high output impedance of the vacuum tube to the low input impedance of the transistor. Suitable coupling devices include transformers, cathode followers used as the vacuum-tube output stage, or high-impedance transistor preamplifiers used as the transistor input stage.

The Handbook Preferred Circuits is designed for loose leaf binding to facilitate the addition of new circuits and the revision of existing circuits as they are updated. The pages in each preferred circuit are numbered independently for the same reason. The material in the Handbook is divided into two parts: Part 1 is the Preferred Circuits Manual and contains the recommended circuits; Part 2 is Notes to the Preferred Circuits Manual and contains related information not essential to the building and use of the preferred circuit. Part 1 is further subdivided into two parts, the first part containing the vacuum-

[1] MIL–STD–706 establishes nominal values for regulated direct-current supply voltages in the range of 100 to 500 volts; it is being revised to include voltages less than 100 volts for transistor circuits. The voltages tentatively selected are 1.5, 3, 6, 12, 25, and 50 volts, positive and negative.

[2] Some of the preferred circuits have been published in MIL–STD–439(AER) with parts completely specified for operation from −55 to +85° C and from −55 to +125° C.

tube circuits, which have numbers less than 200, and the second containing the transistor circuits, whose numbers start with PC 201.

The preferred circuit numbers have been assigned in blocks according to the circuit function. Unused numbers in the blocks have been left for future additions to the Handbook; thus, the present numbering of the preferred circuits is not necessarily consecutive. Each preferred circuit consists of the circuit schematic, specifications, and text giving application, design, and performance information about the circuit. The user of the Handbook may readily determine whether or not a preferred circuit meets his needs by referring to the circuit diagram, the specification, and the first section of the text headed APPLICATION. This section summarizes the capabilities of the circuit and its uses. Information necessary for the design and construction of the circuit is presented under DESIGN CONSIDERATIONS. Performance is discussed in detail in the section headed PERFORMANCE. Other sections are added as necessary.

For the designer whose interest extends beyond the immediate design problem, additional material on each category of preferred circuit is included in the Notes to the Preferred Circuits Manual. The information found in these notes falls into one or more of the following categories:

1. General information, or information applying to more than one of the preferred circuits.

2. Circuit examples taken from an equipment survey, with a brief discussion of the similarities and differences of the circuits. This information may show other methods of obtaining the same circuit function, compare the several methods, summarize the range of performance required, and justify the choice of the preferred circuit.

3. Design considerations which are too lengthy to be included in the Preferred Circuits Manual, and which are of the "nice to know" rather than the "need to know" variety.

CONTENTS

[1] Issued in Supplement 1.
[2] Issued in Supplement 2.
[3] Issued in Supplement 3.

PART 1 PREFERRED CIRCUITS MANUAL—Continued

PART 2 NOTES TO THE PREFERRED CIRCUITS MANUAL

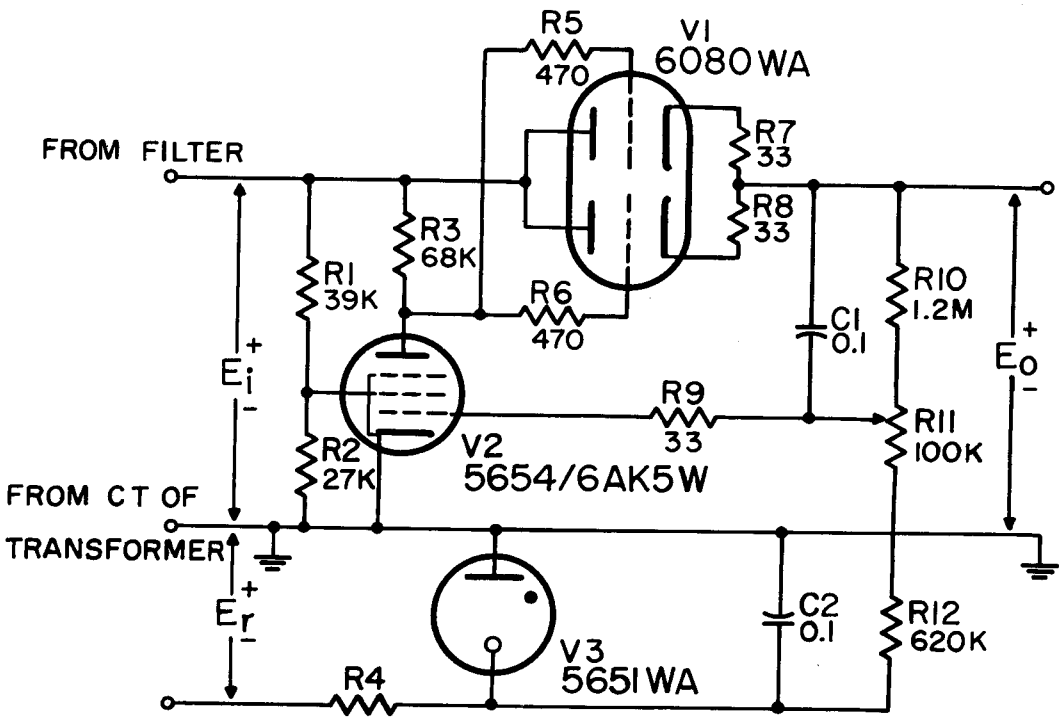
[1] Issued in Supplement 1.
[2] Issued in Supplement 2.
[3] Issued in Supplement 3.

PART 1
PREFERRED CIRCUITS MANUAL

A. VACUUM-TUBE CIRCUITS

NBS PREFERRED CIRCUIT NO. 1
DC REGULATOR FOR POSITIVE OUTPUT 150 VOLTS

NBS PREFERRED CIRCUIT NO. 1
DC REGULATOR FOR POSITIVE OUTPUT 150 VOLTS



Unless otherwise stated: R in ohms; C>1 in $\mu\mu$f; C<1 in μf; L in μh

Output volts E_o	*+Input volts (minimum)* E_i	*−Ref. volts (minimum)* E_r	*R4*
150	200	150	(See Note 1)

Maximum load current per triode section of 6080WA:

1 only	125 ma
2 or more in parallel	100 ma

R10, R12: ±1% limits; R1, R2, R7, R8, R11: ±5% limits; R3, R4: ±10% limits; R5, R6, R9: ±20% limits. (Note 2.)

All C: ±20% limits.

NOTES:

1. Select R4 according to available E_r so as to draw 2.5 ma through 5651WA.
2. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified above. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.
3. R1, R2, R4, R10, R11, R12: Select for temperature stability.

PC 1 DC REGULATOR +150 VOLTS: 1% REGULATION

1. APPLICATION

This circuit has been designed for use where a 1% regulation is acceptable. PC 1 is intended for use with any unregulated power source to provide low output impedance, stability against input voltage variations and output load changes, and ripple reduction. Output variation will be less than ±1% under the normal line and load variations encountered in military equipment.

2. DESIGN CONSIDERATIONS

Considerations concerning design and circuit performance are discussed below.

2.1 *Definitions of Terms:*

(*a*) Stabilization Ratio—S: The change in output voltage for a given change in input voltage with load constant. Stabilization ratio may be used as a percentage or as the inverse ratio, 1/S.

(*b*) DC Output Resistance—R_o: Ratio of change in output voltage to change in output current with input voltage held constant.

(*c*) Output Impedance—Z_o: Ratio of the ac components of output voltage and current when load is varied sinusoidally with input voltage held constant.

(*d*) Ripple Gain—e_i/e_o(120cps): Ratio of the ac components of input voltage to output voltage at ripple frequency. The frequency of 120cps is selected as lowest frequency usually encountered.

2.2 *Reference Circuit:* Although complete comparison data are not available, the 5651 and electrical equivalents appear to be the most stable glow discharge devices available.

By feeding the 5651 from a regulated external negative source rather than connecting it between the cathode of the dc amplifier tube and ground, three improvements are effected: first, the cathode of the amplifier is at ground rather than 90 volts above ground, thereby allowing a larger plate swing; second, the 5651 is in a grid rather than a cathode circuit and therefore operates under constant current conditions; and third, the dc amplifier gain is greater with this connection because cathode degeneration caused by gas tube impedance is not present. The choice of current is a compromise between higher noise level at lower currents and shortened life at higher currents. The bypass capacitor, C2, is the largest value recommended by tube manufacturers.

2.3 *Amplifier Circuit:* The 5654 and electrical equivalents were chosen for the amplifier because of their recurrence in equipment design and their generally satisfactory operation. The plate feed is

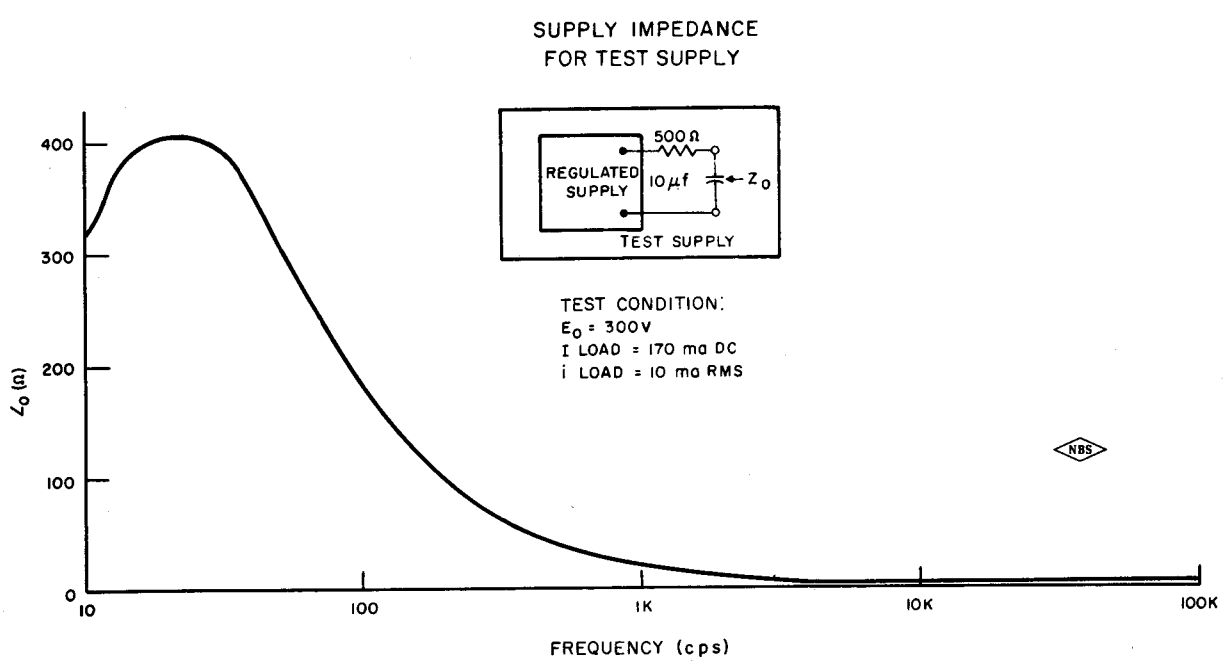
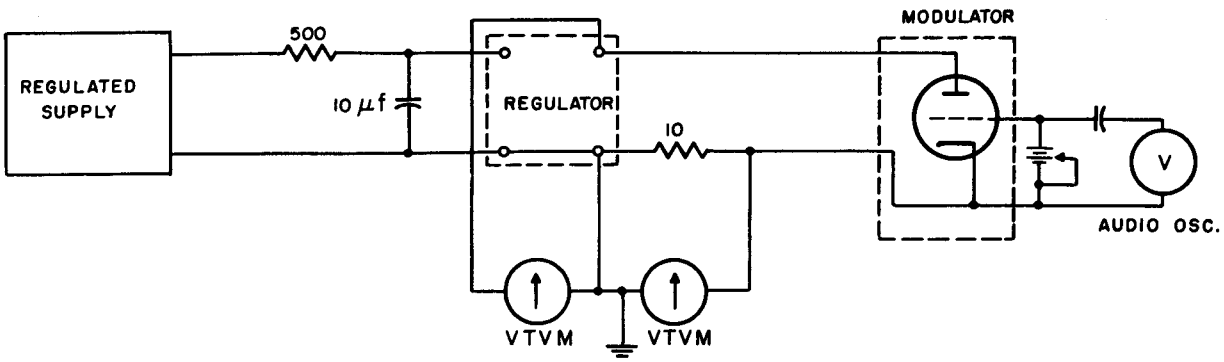


Fig. 1-1



TEST CIRCUIT FOR MEASURING RELATIVE OUTPUT IMPEDANCE OF A VOLTAGE REGULATOR

Fig. 1-2

taken from the unregulated output. Screen grid sensing from the unregulated voltage increases the gain of the amplifier. The 33Ω resistor in the control grid circuit is a parasitic oscillation suppressor.

2.4 *Series Tube:* The 6080 and equivalents were chosen because of their low static plate resistance and high heater-to-cathode voltage rating. Cathode resistors are included for the purpose of equalizing current flow when triode sections are connected in parallel. The grid resistors are parasitic oscillation suppressors.

2.5 *Measured Performance:* Z_o of the test supply used for measurements is shown in figure 1-1.

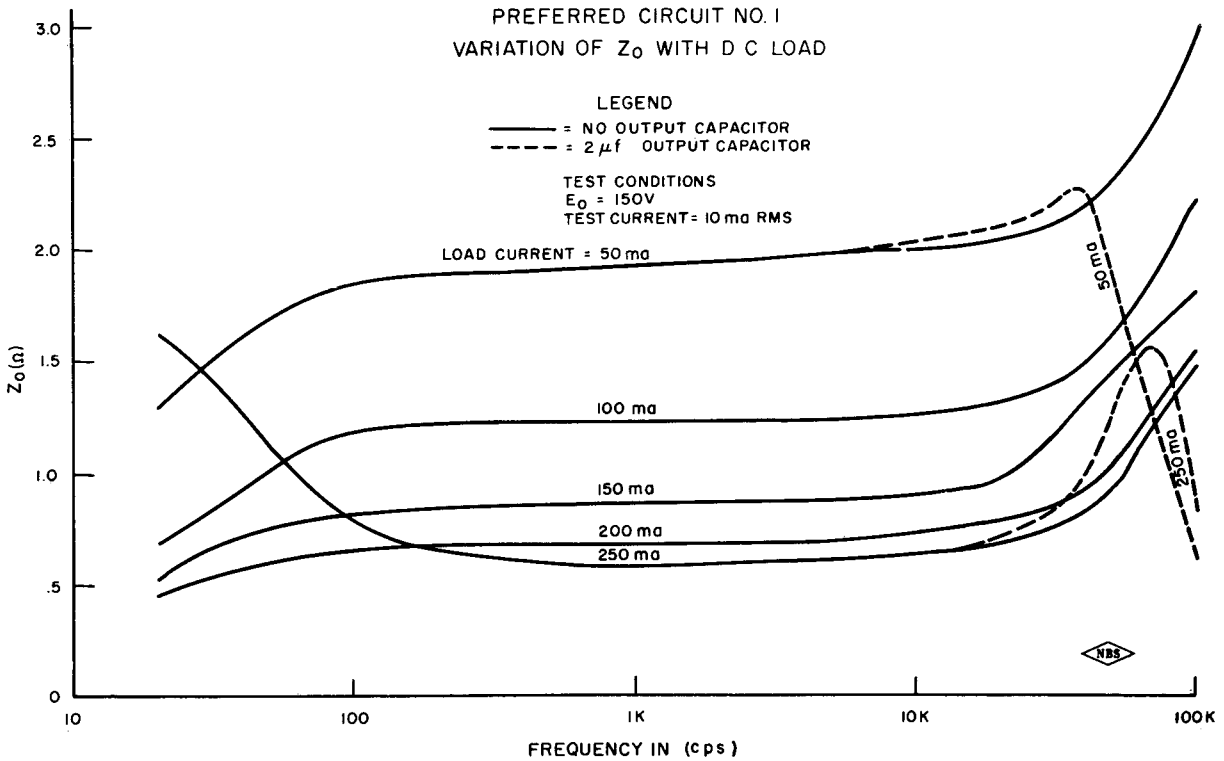


Fig. 1-3

This test supply is a simulated unregulated supply formed by adding series resistance and shunt capacitance to a standard laboratory power supply. A supply of this type was used to keep power source ripple from masking the output impedance measurements. Figure 1–2 shows the test setup used for deriving the impedance curve. [1] [2] In figure 1–3 typical impedance curves of the combined regulator and supply are shown as a function of load current. Since reduction of impedance is a function of the series tube transconductance, and transconductance is a function of tube current, the increase of effective impedance with decrease in load current is expected. The effect of output capacity on impedance is shown by the dotted lines for two cases of load current. A value of 2μf was used as the lowest value to be expected in practice. Increased capacity decreases the magnitude of the hump and the frequency at which the maximum occurs. In the preferred circuit, increased capacity will not cause oscillation.

The 6080 series tube in the degenerative electronic regulator of PC 1 regulates by simulating a variable resistor in series with the supply voltage. The difference between the supply or input voltage, E_i, and the regulated output voltage, E_o, is the plate-cathode voltage drop, E_{pk}, across the series tube. When the regulator is operating, an increase in input voltage results in an increase in the magnitude of the negative grid cathode bias of the series tube. This increases the effective resistance of the series tube. The plate cathode drop across this tube is thereby increased (assuming constant load current) while the output voltage remains approximately constant. When the input voltage drops, the magnitude of the negative grid cathode bias of the series tube is reduced by the action of the 5654 regulator amplifier, the tube becomes a smaller effective series resistor, its E_{pk} decreases, and the output voltage remains essentially constant. If the input voltage continues to decrease, a point will be reached where

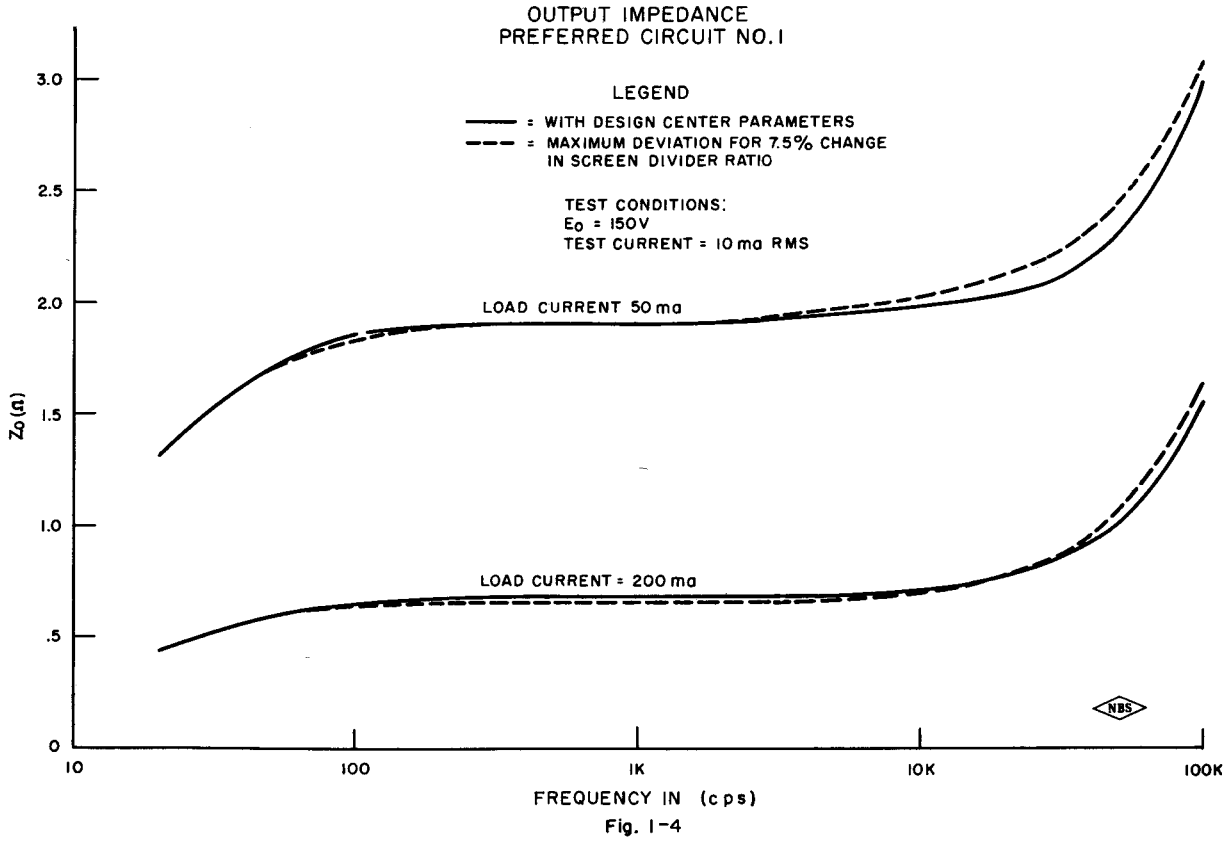


Fig. 1–4

[1] J. H. Hersey, *Dynamic Impedance of Regulated Power Supplies*, Bell Lab. Rec., vol. 27, p. 216, June 1949.
[2] 50 IRE 23, S3, Proc. IRE, Jan. 1951, fig. 3, par. 3.5.2.

the grid cathode potential of the series tube will become zero. At this point, the series tube grid will draw current and the regulator amplifier will lose control. The output voltage will now drop sharply. This value of E_{pk} which is a function of input voltage (output voltage remaining constant until this point) is known as the break point voltage, because it is the point at which the output voltage breaks sharply when the input voltage is continually decreased. In the test noted, the plate cathode voltage, E_{pk}, of the series tube was set 10v greater than the break point voltage. The test supply shown in figure 1-1 has an LC filter. This filter is resonant in the vicinity of 20cps. This resonance together with the high impedance of the simulated supply is sufficient at 250ma load to drive the 6080 grid to its positive region on negative peaks at low frequencies.

The curves in figure 1-4 show the effect of a 7.5% variation in the screen divider ratio, R1/(R1+R2), on Z_o for load currents of 50 and 200ma. Substitution of a range of tubes shows a variation of ±50% in performance. The optimum screen divider ratio, however, is relatively constant. The gain of the regulator with respect to power frequency variations of input voltage is shown in figure 1-5. All curves were taken with a ripple amplitude of 1 volt rms. The average 5654 or equivalent will allow satisfactory operation at minimum input voltage (50v plus the output voltage). In the case of some tubes, poor ripple-reduction and low-frequency stabilization will be encountered at full load-minimum input voltage conditions. With tubes giving the results shown in the composite curve of figure 1-5, little improvement with change in screen divider ratio is found. The bottom curve of figure 1-5 shows the operation of this regulator with screen divider connected to the regulated output. The improvement afforded by input side connection of the screen divider is considerable.

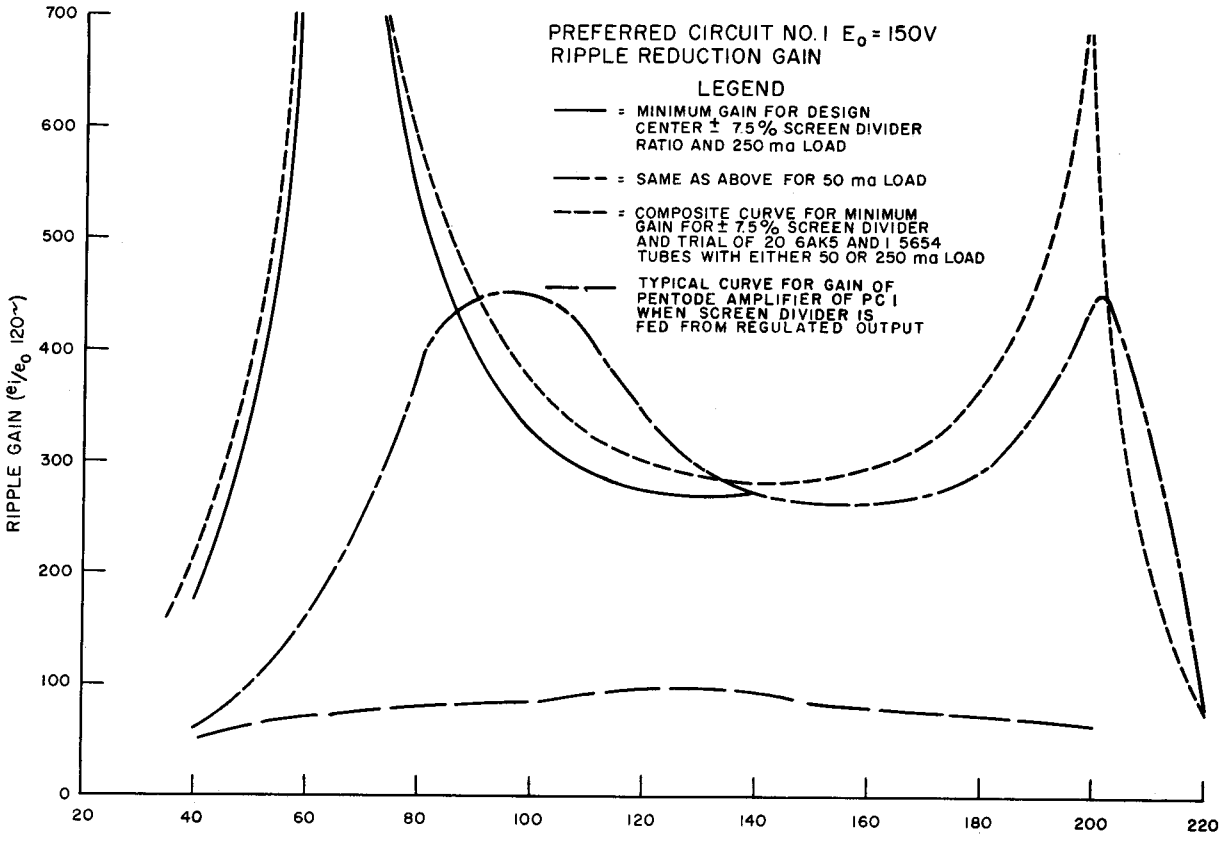


Fig. 1-5

Typical dc characteristics of the circuit are shown in figure 1-6. The over-all regulation is better than 0.33%. This regulation compares favorably with the stability of the reference source, which may be ±0.5% including effects of temperature and long time changes.

The output current is:

(*a*) Maximum load current per triode section of 6080:

1 only	125ma
2 or more in parallel	100ma

This limitation is dictated by the plate dissipation limits allowed by MIL-E-1B.

(*b*) Some deterioration in Z_o at high frequencies should be anticipated when additional 6080 sections are paralleled to obtain higher output current.

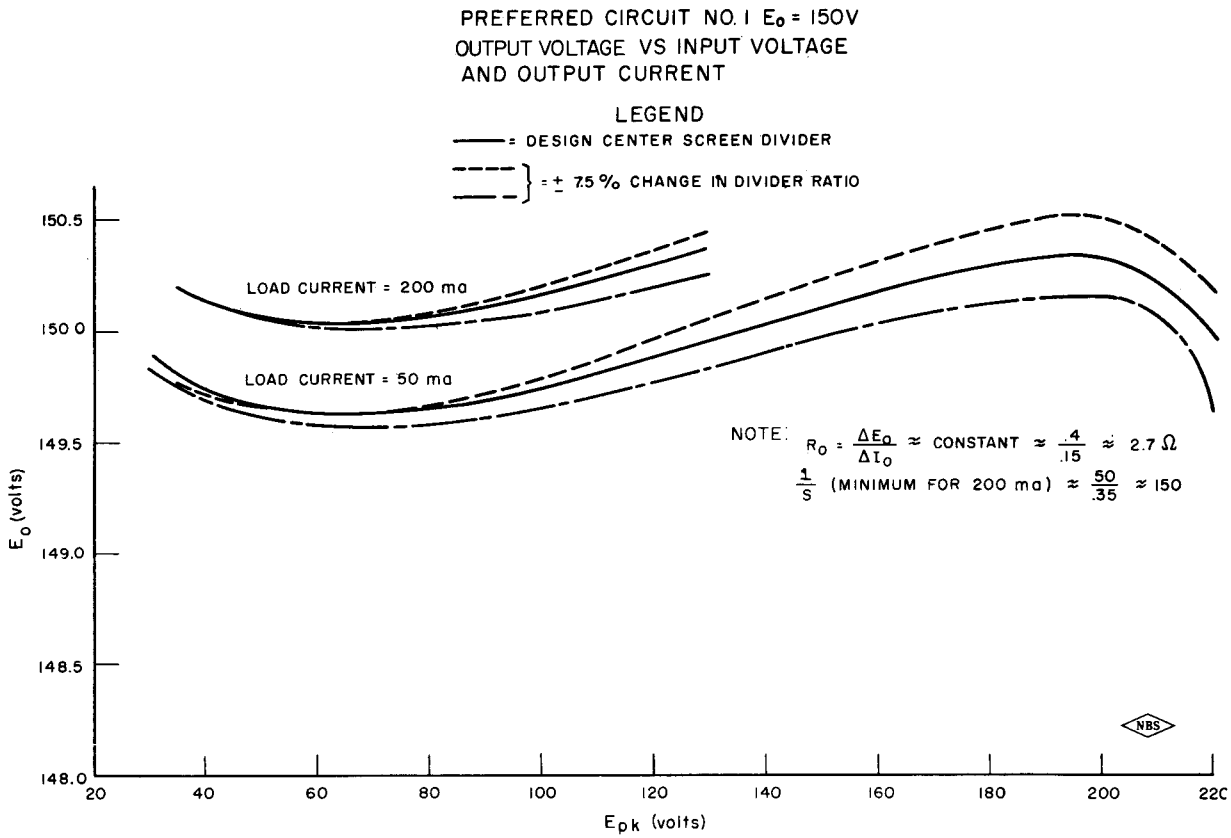
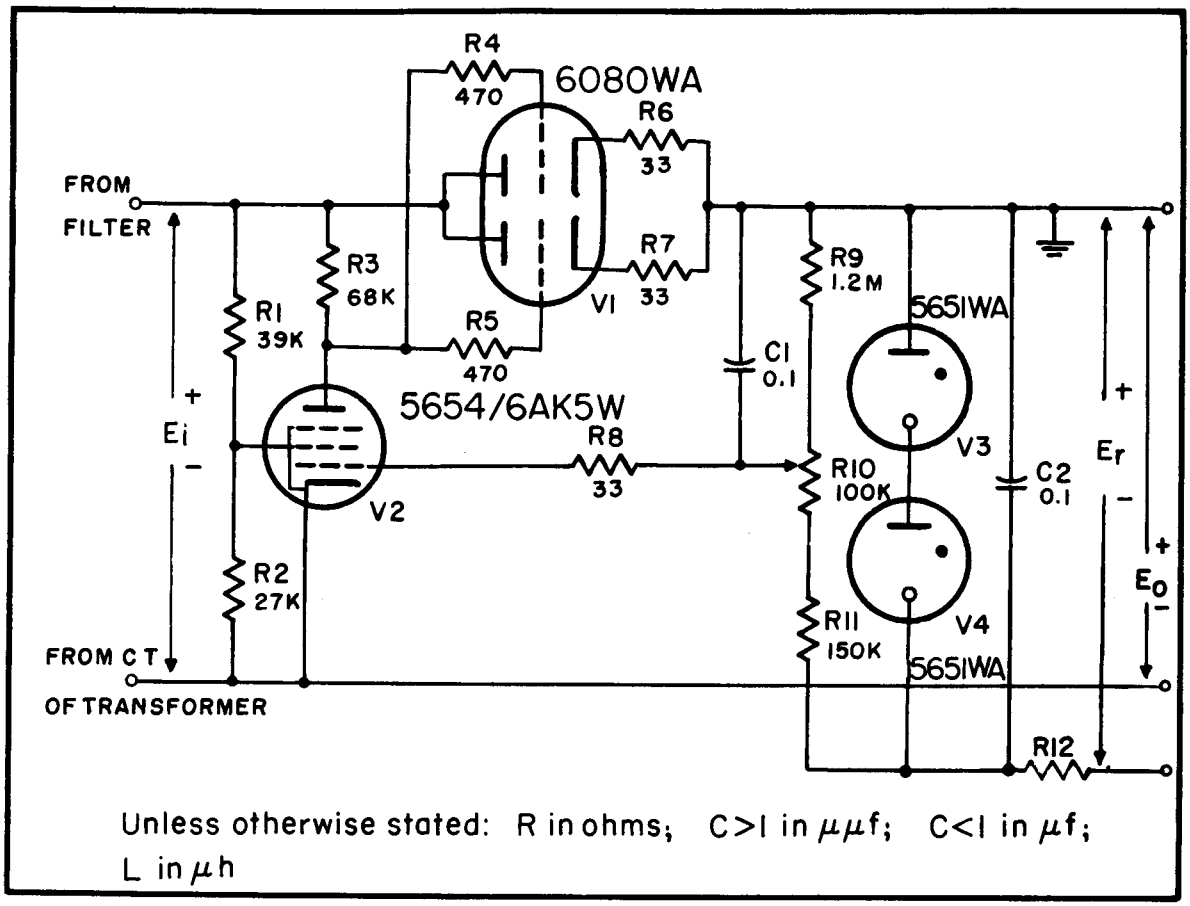


Fig.1-6

NBS PREFERRED CIRCUIT NO. 2

DC REGULATOR FOR NEGATIVE OUTPUT 150 VOLTS: 1% REGULATION

NBS PREFERRED CIRCUIT NO. 2
DC REGULATOR FOR NEGATIVE OUTPUT 150 VOLTS



Output volts E_o	*Input volts (minimum)* E_i	*−Ref. volts (minimum)* E_r	*Resistors* R1	R2	R12
150	200	300	39KΩ	27KΩ	(See Note 1)

Maximum load current per triode section of 6080WA:

1 only	125 ma
2 or more in parallel	100 ma

R9,R10,R11: ±1% limits; R1,R2,R6,R7: ±5% limits; R3,R12: ±10% limits; R4,R5,R8: ±20% limits. (Note 2.)

All C: ±20% limits.

NOTES:

1. Select R12 according to available E_r so as to draw 2.5 ma through 5651WA.
2. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified above. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.
3. R1,R2,R9,R10,R11,R12: Select for temperature stability.

PC 2 DC REGULATOR FOR −150 VOLTS: 1% REGULATION

1. APPLICATION

This circuit has been designed for use where a 1% regulation is satisfactory. PC 2 is intended for use with any unregulated power source to provide low output impedance, stability against input voltage variations and output load changes, and ripple reduction. Output variation will be less than ±1% under the normal line and load variations encountered in military equipment.

2. DESIGN CONSIDERATIONS

All considerations given in PC 1 apply to this circuit. Only deviations from this circuit will be discussed.

2.1 *Reference Circuit:* A second reference tube is required to provide negative bias.

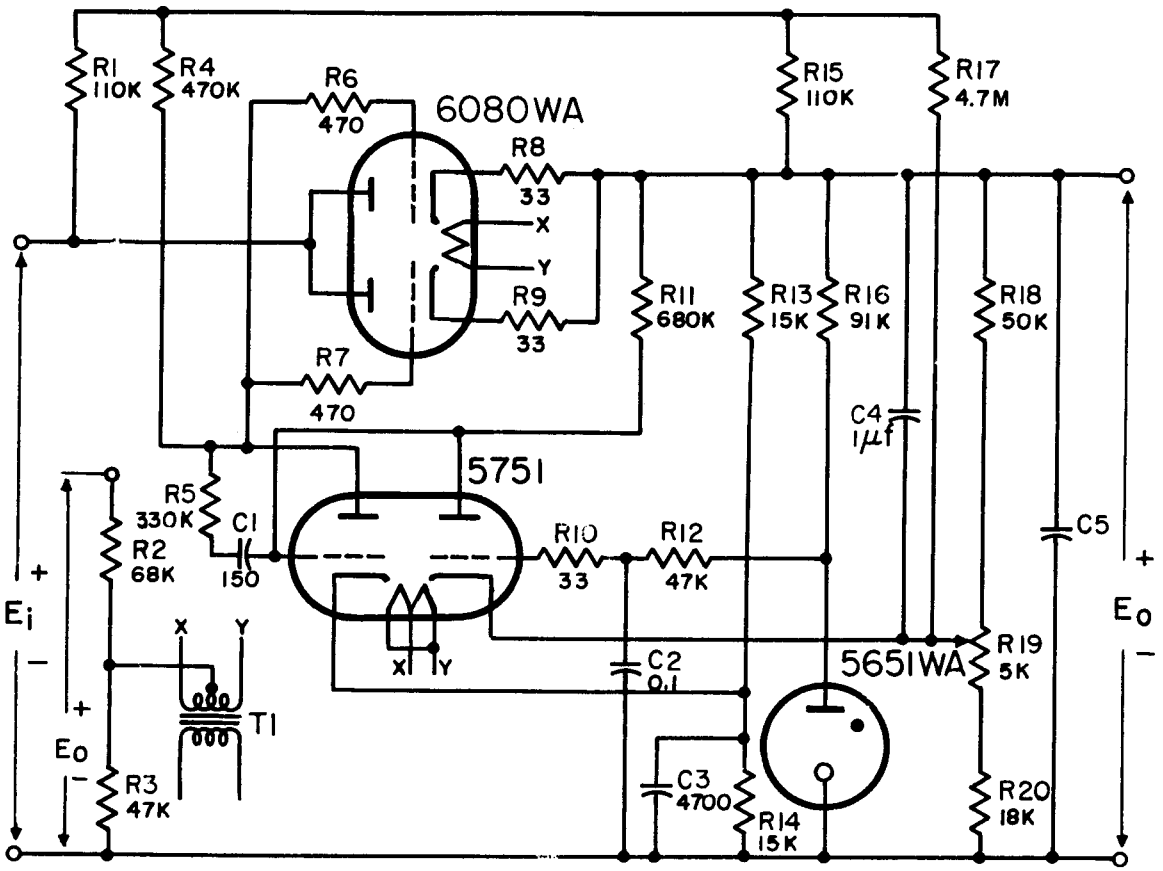
The characteristic curves shown for PC 1 apply to this circuit also. The dc characteristics such as R_o are improved because of the lower attenuation in the comparison circuit.

NBS PREFERRED CIRCUIT NO. 3A

DC REGULATOR FOR PLUS OR MINUS 300 VOLTS: 1% REGULATION

NBS PREFERRED CIRCUIT NO. 3A

DC REGULATOR FOR PLUS OR MINUS 300 VOLTS



Unless otherwise stated: R in ohms; C > 1 in μμf; C < 1 in μf; L in μh

Output volts E_o	*Input volts (minimum)* E_i	*C5 (minimum)*
300 (Note 1)	350	4μf

Maximum load current per triode section of 6080WA: 1 only, 125 ma; 2 or more in parallel, 100 ma.

R17: Temperature and voltage stable.

R18,R19,R20: Wire-wound or other temperature stable type. Use equal wattage per ohm rating in each arm of divider.

R18,R20: ±1% limits; R8,R9,R13,R14,R17,R19: ±5% limits; R5: ±10% limits; R1,R2,R3,R4, R6,R7,R10,R11,R12,R15,R16: ±20% limits. (Note 2.) All C: ±20% limits.

NOTES:

1. Ground one side of the regulated output to obtain the desired polarity. For negative outputs, the input voltage must be ungrounded.

2. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified above. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.

Positive input Terminal
must not be grounded

PC 3A DC REGULATOR ±300 VOLTS: 1% REGULATION

1. APPLICATION

This circuit has been designed for use when 1% regulation is satisfactory. PC 3A is intended for use with any unregulated power source to provide low output impedance, stability against input voltage variations and output load changes, and ripple reduction. This circuit was chosen to meet the many needs for a supply with self-contained reference source, low impedance, and high gain with respect to low-frequency input disturbances.

2. DESIGN CONSIDERATIONS

Considerations concerning design and circuit performance are discussed below. Figures 3-1 and 3-2 show typical operating conditions.

2.1 *Reference Circuit:* Although complete comparison data are not available, the 5651 and electrical equivalents appear to be the most stable glow discharge devices available. The 5651 is fed from the regulated output. The choice of current is a compromise between higher noise level at lower currents and shortened life at higher currents. The bypass capacitor and resistor network R12, C2 is designed to attenuate the transient noise spikes characteristic of glow discharge tubes. R10 is a parasitic oscillation suppressor.

2.2 *Amplifier Circuit:* The 5751 and electrical equivalents were chosen for the amplifier because of their recurrence in equipment design and generally satisfactory performance. The plate feed is taken from a voltage divider across the series tube to decrease the plate swing required of the output section of the 5751. This circuit is a compromise between higher plate supply potential allowing linearity of operation at low input voltage and high load conditions, and constant voltage plate-feed to yield better gain and lower required plate swing at normal operating conditions.

The need for lower plate swing may be seen by the following illustration. Assume an increase in input voltage. The plate of the output tube now swings negative in order to pull the grids of the series tubes more negative. The supply of the output section of the regulator has become more positive since it is fed from the unregulated input. Therefore the tube must swing negative by an additional amount to compensate for this rise in supply voltage. The divider cuts this compensating swing in half.

Without this arrangement, it is difficult to design the amplifier with a reasonable plate load resistor in the 5751 output stage and at the same time allow the regulator to operate at high-vol-

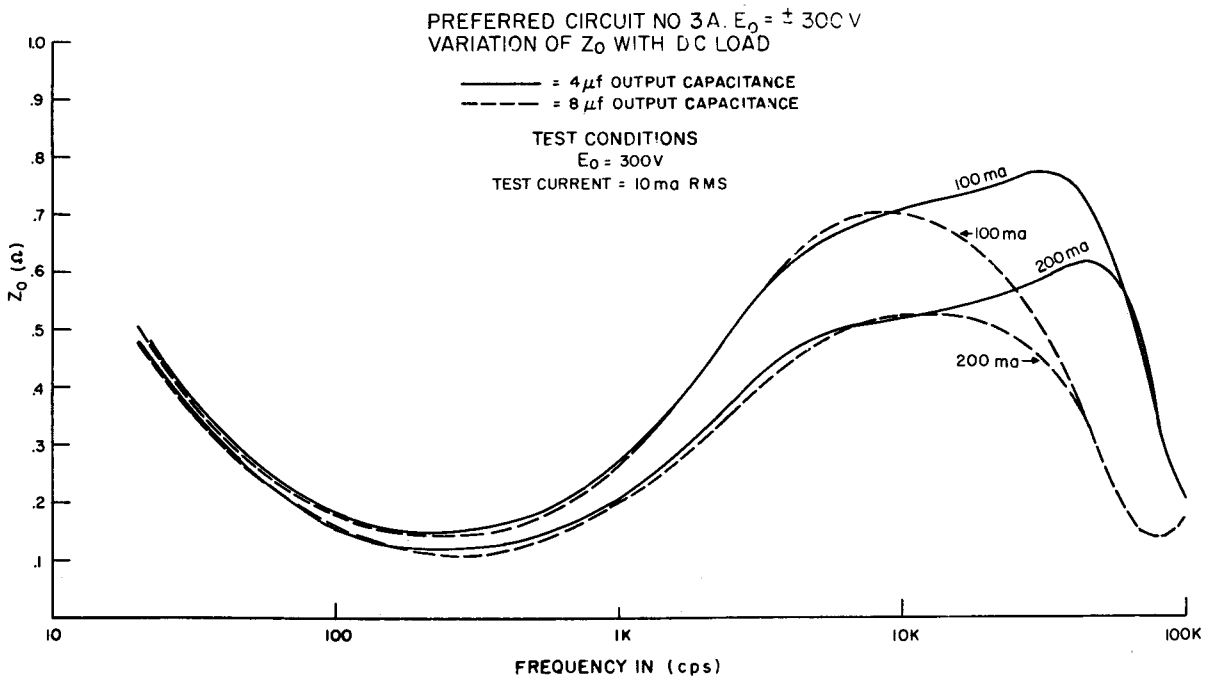


Fig. 3-1

tage, low-current levels without driving the grid of the output section of the 5751 positive. The loop gain of the amplifier exceeds 1000.

The divider in the input stage of the 5751 is not within this loop. The circuit is very sensitive to changes in divider ratio. The use of a low resistance divider causes appreciable power dissipation; this divider should therefore employ resistors whose wattage ratings are very conservative. These wattages should be in the same ratio as the power dissipation so as to yield a reasonably constant ratio. This factor is one of the most critical aspects of regulator stability.

The feedback network R5, C1 provides frequency selective negative feedback across the output stage of the regulator amplifier. This decreases the regulator high frequency output impedance at the cost of increased mid-frequency output impedance. Resistor R17 decreases output resistance and increases stabilization by feeding a portion of the input voltage change to the regulator-amplifier cathode.

2.3 *Series Tube:* For a discussion of the series tube refer to PC 1, Section 2.4.

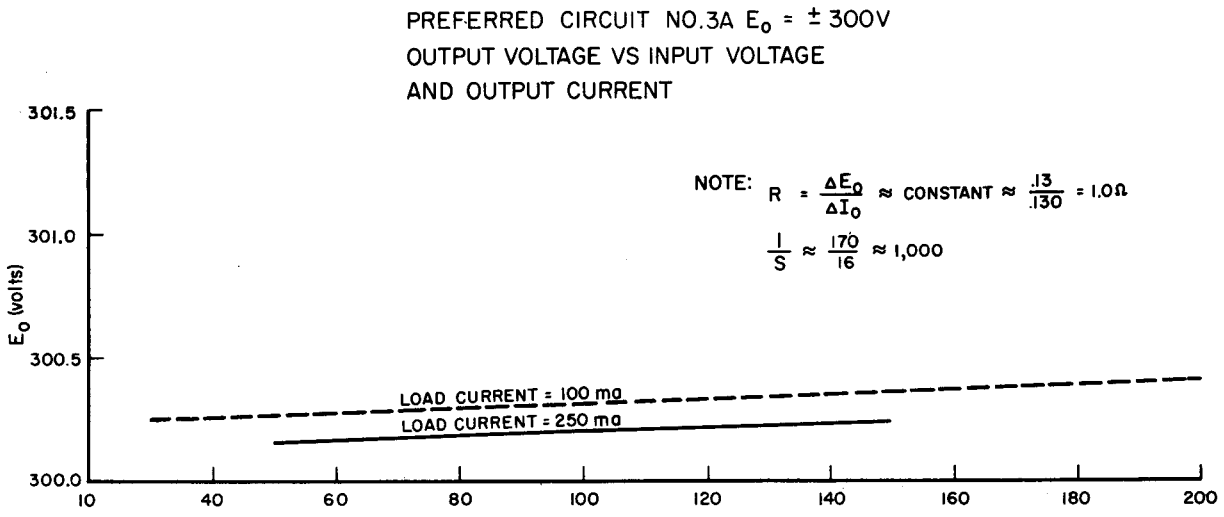


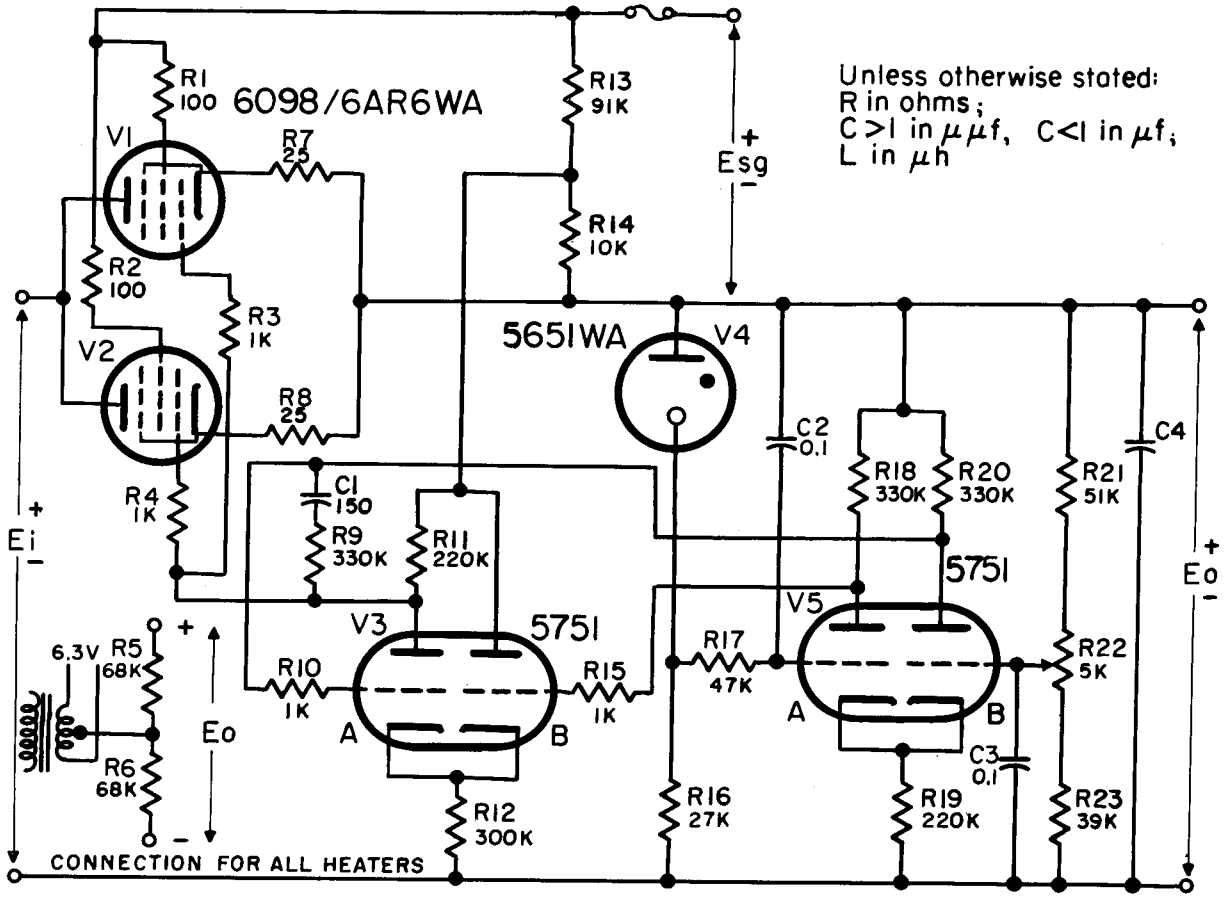
Fig. 3-2

NBS PREFERRED CIRCUIT NO. 4

DC REGULATOR FOR PLUS OR MINUS 150 VOLTS: 0.1% REGULATION

NBS PREFERRED CIRCUIT NO. 4

DC REGULATOR FOR PLUS OR MINUS 150 VOLTS



Output volts E_o	*Input volts (minimum)* E_i	*Screen volts (minimum)* E_{sg}	*C4*
150 (Note 1)	190	150 (Note 2)	4 μf

Maximum load current: 100 ma per series tube.

R7,R8,R16,R19,R21,R22,R23: Wire-wound or other temperature stable type. Use equal wattage per ohm in each arm of reference divider.

R19,R21,R23: ±1% limits; R7,R8: ±2% limits; R16,R22: ±5% limits; R9,R11,R12,R18,R20: ±10% limits; R1,R2,R3,R4,R5,R6,R10,R13,R14,R15,R17: ±20% limits. (Note 3)

C1: ±10% limits; all other C: ±20% limits.

NOTES:

1. Either output terminal may be grounded; however, the positive input terminal must not be grounded. Positive Input Terminal Must Not be Grounded

2. Screen supply should be fused for 20 ma per series tube to prevent damage to the screen if the input voltage is off while the screen supply is on. If an unregulated screen supply is used, maximum ripple should be 1.0 volt rms.

3. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified above. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.

PC 4 DC REGULATOR ±150 VOLTS: 0.1% REGULATION

1. APPLICATION

This circuit has been designed for use in applications requiring superior regulation and long time stability. The factors affecting output voltage stability with respect to temperature and time are the characteristics of the glow-discharge reference tube, the input-stage cathode-balance, and the reference-voltage divider.

2. DESIGN CONSIDERATIONS

2.1 *Definition of Terms:* See PC 1, Section 2.1.

2.2 *Series Tube:* A 6098 pentode-connected series tube was chosen for use with this circuit because it requires less control grid voltage variation to compensate for a given change in load current or line voltage as compared with a low-mu triode, and thereby allows considerable simplification of the associated control circuitry. This advantage more than makes up for the added complexity and increased power consumption of the screen-voltage supply.

In the operation of the pentode-connected 6098 series tube, under conditions of zero control grid bias and 150v difference of potential between the screen and cathode, a maximum load current of 100ma will flow when the plate cathode voltage is 35v. Under these conditions the screen will draw 12.5ma.

The separate screen supply can be connected between the screen of the 6098 tube and the positive side of the PC 4 output, as shown. If a separate 300v supply is available, it may be connected between the 6098 screen and the negative side of the output, with the advantage that the screen current in this case adds to the load current.

While a regulated voltage source in the screen circuit of the PC 4 yields smaller changes in output voltage for given changes in input voltage and output current, an unregulated screen supply will keep output voltage changes less than 150 millivolts, or 0.1%.

The current output of PC 4 has been nominally rated at 100ma per series tube, by allowing for the maximum screen current consumption and 10% cathode current derating of the 6098. If the current that the screen draws adds to the load current, then the maximum load current is increased to 112.5ma per tube.

2.3 *Amplifier Circuit:* The regulator amplifier has two cascaded twin triode stages, (i. e., the plates of the input stage feed the grids of the output stage). The input stage, V5, is a balanced differential amplifier, while the output stage is a cathode-coupled differential amplifier. [1] A change in the dc output voltage, E_o, appears in full at the grid of V5A but is attenuated at the grid of V5B. Initial velocity and contact potential changes are balanced out in a common cathode resistor, R19.

The balanced output of V5 is fed to the grids of V3. A single-ended output is taken from the plate of V3A and used to drive the control grids of V1 and V2.

Filter R17, C2 attenuates noise generated by gas tube V4 before it reaches the grid of V5A.

Neglecting R22, the voltage change seen at the grid of V5B for slow changes in E_o is R23/(R21+R23) of the change in E_o. For more rapid changes in E_o, R23 is bypassed by C3 and the change seen at the grid of V5B is therefore zero. The differential voltage seen by the grids of V5 for rapid changes in output voltages is therefore equal to the total change in output voltage.

A series RC circuit (R9, C1) is connected between the plate and grid of V3A. This circuit provides negative feedback which reduces the gain of the output stage, thus decreasing the over-all loop gain with a resulting increase in the output impedance of the regulator at frequencies higher than 500cps. However, in the vicinity of 50kc, the feedback network produces a phase shift which prevents the regulator from becoming unstable and oscillating.

The output capacitor C4 acts as a low output impedance at frequencies above 60kc where the gain of the amplifier is too low to be effective. It also acts to decrease the signal fed to the amplifier so that phase shift present in the loop at these high frequencies cannot cause oscillation.

The cumulative effect of R3, C1, C3, and C4 is to produce an output impedance which decreases

[1] George E. Valley, Jr. and Henry Wallman, ed., *Vacuum Tube Amplifiers, Rad. Lab. Series*, vol. 18, McGraw-Hill, 1948, p. 441.

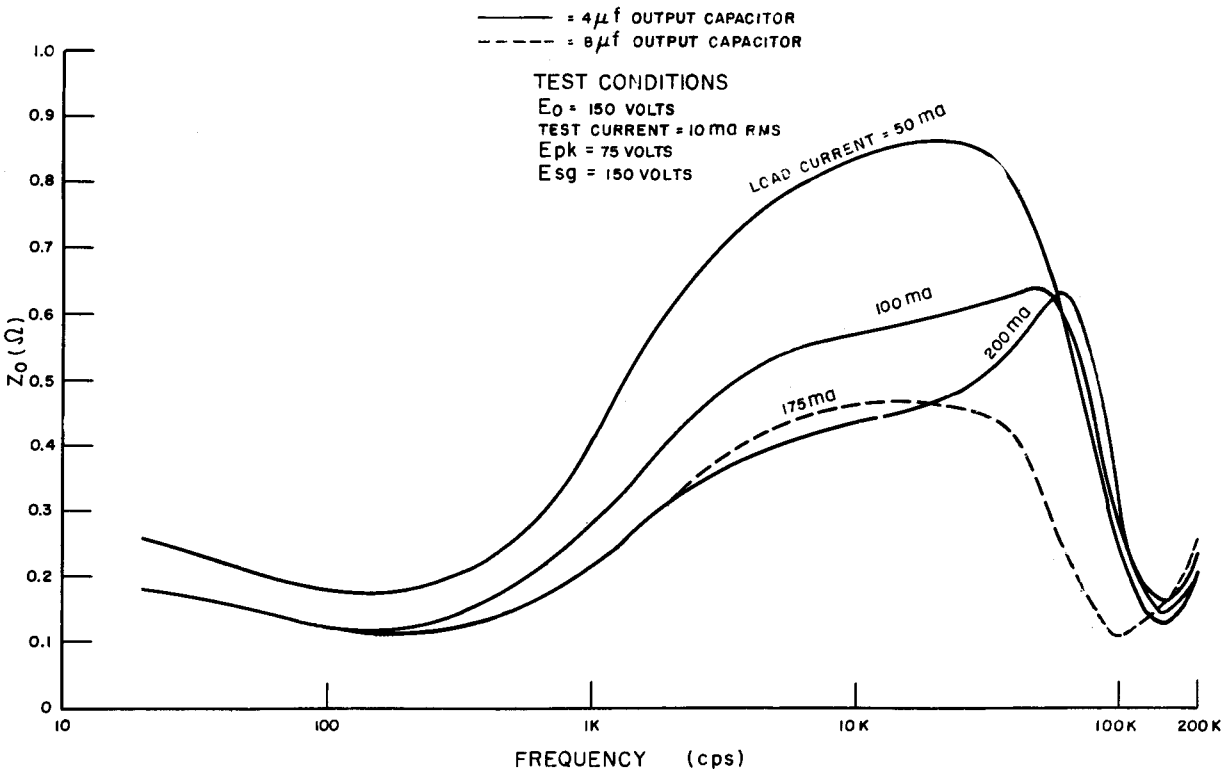


Fig. 4-1

in magnitude from zero frequency to about 200cps because of C3, increases in magnitude from 200cps to about 50kc, then is restricted in magnitude between 50kc and 70kc due to R9, C1, and decreases in magnitude between 70kc and 150kc due to C4. At about 150kc, C4 is series resonant. Above this frequency the impedance is determined by lead inductance.

The plates of the output amplifier tube, V3, are fed from a divider across the separate screen supply. The screen supply is used because even when unregulated, it varies less than the input voltage, while the divider further reduces this variation and allows optimum setting of the plate supply voltage.

2.4 *Measured Performance:* Impedance was measured in the same manner as described in Section 2.5 of PC 1. Measurements taken with both regulated and unregulated screen supplies showed negligible differences. Typical results for full, half, and quarter maximum-load currents are shown as solid lines in figure 4-1. All three of these curves were taken with a 4μf capacitor across the supply output. A fourth curve, shown dotted, was taken with a load of 175ma and an output capacitor of 8μf, to show the effect of increasing the output capacity. The impedance is less than 1 ohm under all the conditions shown in figure 4-1, and the lack of sharp peaks in the characteristic indicates stability against oscillation.

A typical curve showing output voltage as a function of series tube plate-cathode voltage, when input voltage only is varied and screen and heater voltages are held constant, is shown by the solid line of figure 4-2. The variation of output voltage as a function of plate-cathode voltage when both screen and input voltage are varied is shown by the broken line of figure 4-2, while the variation of output voltage as a function of plate-cathode voltage when screen, input, and heater supplies are simultaneously varied is shown by the dotted line of figure 4-2. These

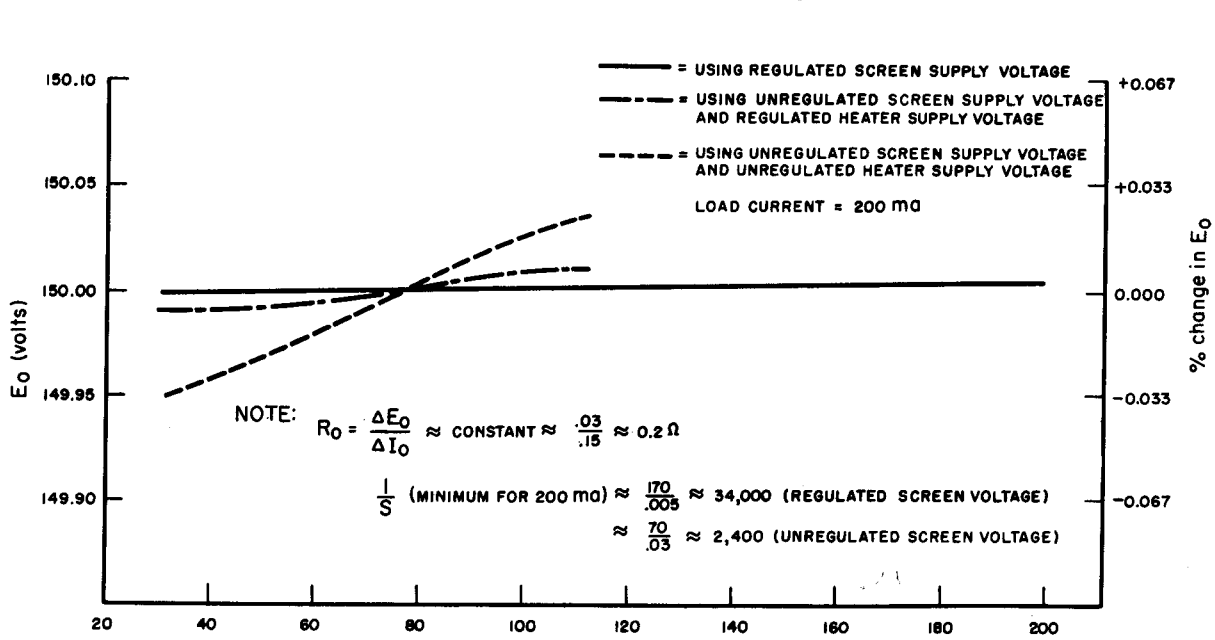


Fig. 4-2

latter two measurements were taken by connecting first the screen and input, and secondly the screen, input, and heater supplies to the output of a variable transformer. The relation between AC line, screen, and plate-cathode voltages is show in figure 4–3 (page 4–6). The nominal line voltage was taken as 115v and variations were ±10% about this value. Heater voltage as a function of plate-cathode voltage is not shown as it is an essentially linear function of ~~the~~ LINE voltage, and in general, restrictions in performance specifications are on line rather than heater voltage.

The over-all conclusion to be drawn from the curves shown is that heater voltage variation is the prime offender in changing output voltage in PC 4. However, adding the effect of change in load current (which is 0.03v for a reduction in load current from full to quarter load) to the worst over-all variation shown, the change in output is less than 0.1% or 0.15v.

The measured dc resistance was approximately 0.2Ω. An input ripple of 10 volts results in an output ripple of less than 1 millivolt.

PREFERRED CIRCUIT NO. 4 E_0 = ±150V

RELATION OF AC LINE VOLTAGE AND
SCREEN VOLTAGE TO PLATE-CATHODE VOLTAGE

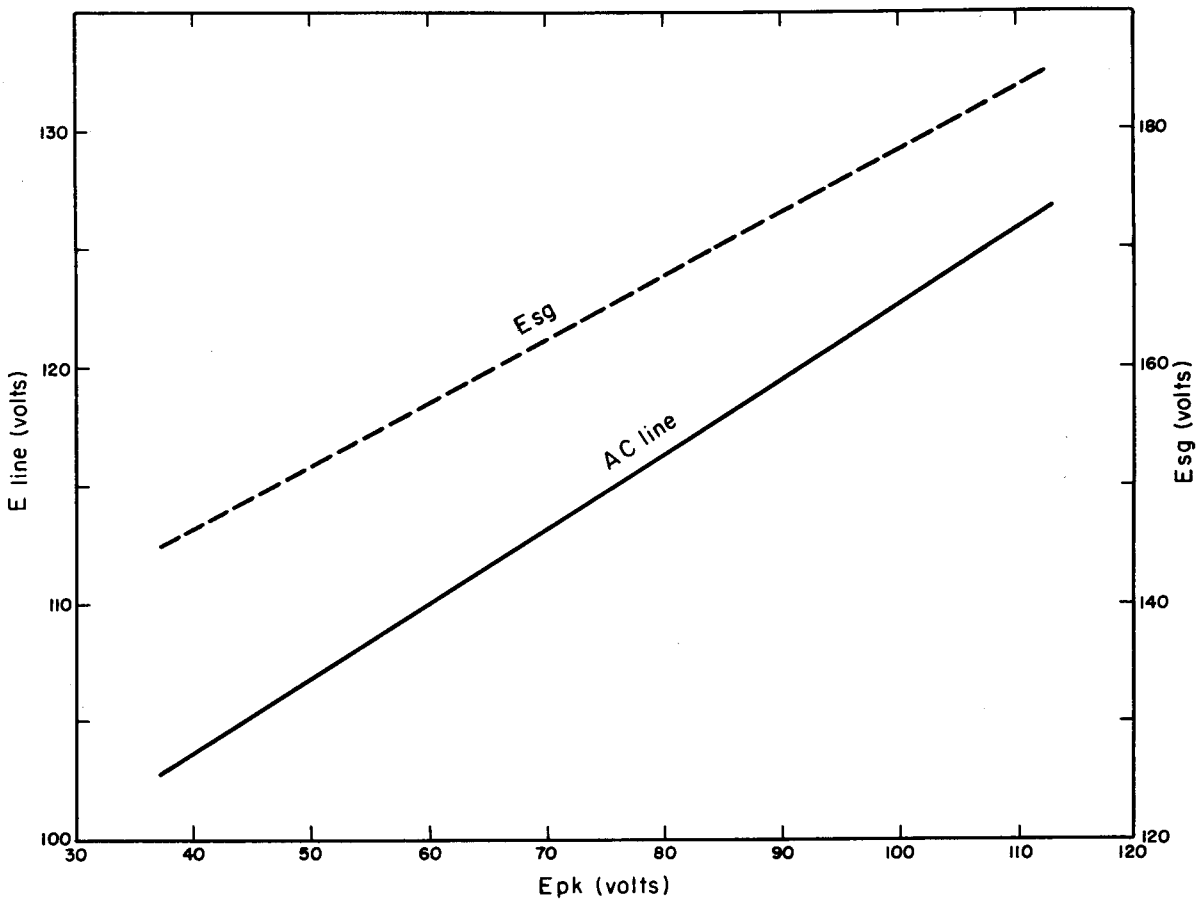


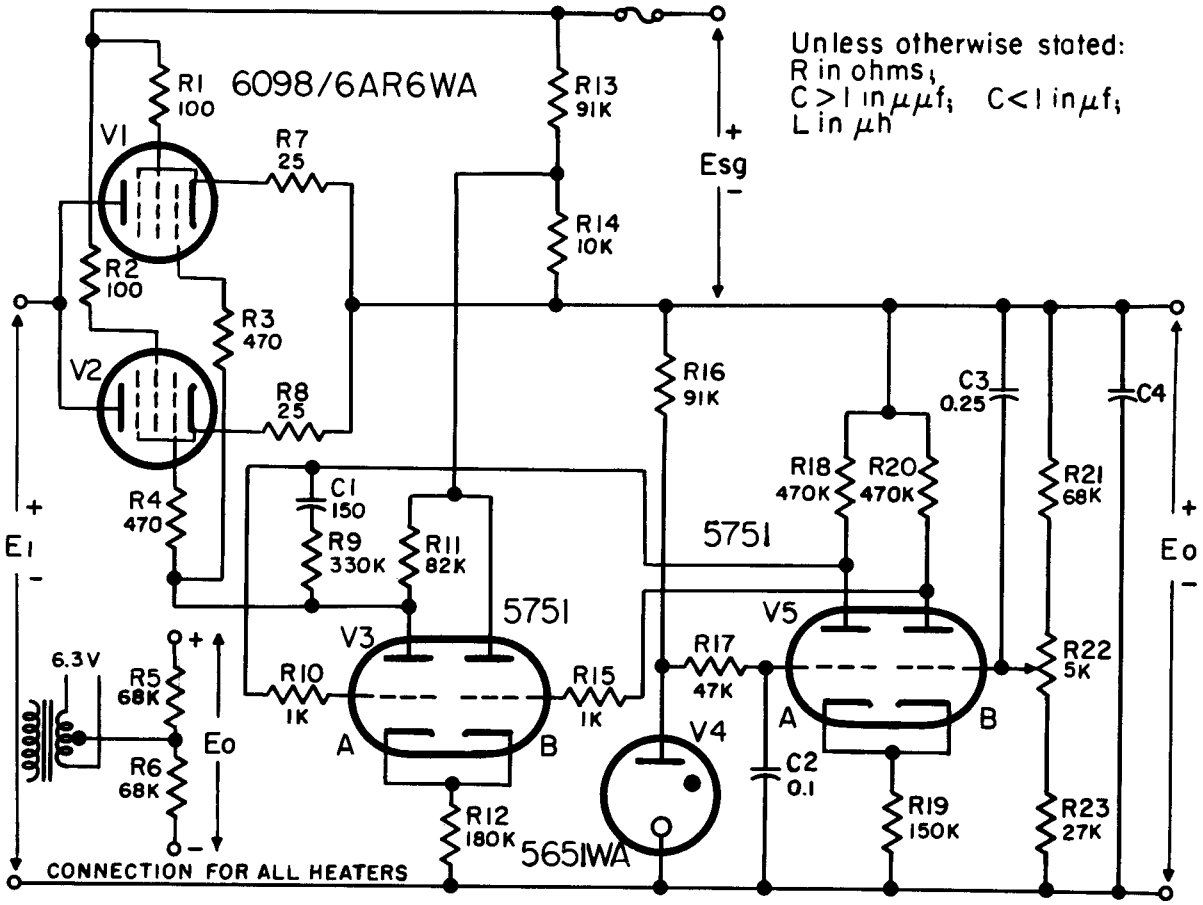
Fig. 4-3

NBS PREFERRED CIRCUIT NO. 5

DC REGULATOR FOR PLUS OR MINUS 300 VOLTS: 0.1% REGULATION

NBS PREFERRED CIRCUIT NO. 5

DC REGULATOR FOR PLUS OR MINUS 300 VOLTS



Output volts E_o	*Input volts (minimum)* E_i	*Screen volts (minimum)* E_{sg}	*C4 (minimin)*
300 (Note 1)	340	150 (Note 2)	4μf

Maximum load current: 100 ma per series tube.

R7,R8,R16,R19,R21,R22,R23: Wire-wound or other temperature stable type. Use equal wattage per ohm in each arm of reference divider.

R19,R21,R23: ±1% limits; R7,R8: ±2% limits; R16,R22: ±5% limits; R9,R11,R12,R18,R20: ±10% limits; R1,R2,R3,R4,R5,R6,R10,R13,R14,R15,R17: ±20% limits. (Note 3)

C1: ±10% limits; all other C: ±20% limits.

NOTES:

1. Ground one side of the regulated output to obtain the desired polarity. For negative outputs, the input voltage must be ungrounded. Positive input must not be grounded.

2. Screen supply should be fused for 20 ma per series tube to prevent damage to the screen if the input voltage is off while the screen supply is on. If an unregulated screen supply is used, maximum ripple should be 1.0 volt rms.

3. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified above. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.

PC 5 DC REGULATOR ±300 VOLTS: 0.1% REGULATION

1. APPLICATION

This circuit has been designed for use in applications requiring superior regulation and long time stability. The factors affecting output voltage stability with respect to temperature and time are the characteristics of the glow-discharge reference tube, the input-stage cathode-balance, and the reference-voltage divider.

2. DESIGN CONSIDERATIONS

2.1 *Definition of Terms:* See PC 1, Section 2.1.

2.2 *Series Tube:* A 6098 pentode-connected series tube was chosen for use with this circuit because it requires less control grid voltage variation to compensate for a given change in load current or line voltage as compared with a low-mu triode, and thereby allows considerable simplification of the associated control circuitry. This advantage more than makes up for the added complexity and increased power consumption of the screen-voltage supply.

In the operation of the pentode-connected 6098 series tube, under conditions of zero control-grid bias and 150v difference of potential between the screen and cathode, a maximum load current of 100ma will flow when the plate-cathode voltage is 35v. Under these conditions the screen will draw 12.5ma.

The separate screen supply will in general be regulated for negative output and unregulated for positive output, because there is usually a regulated 150v positive supply available in any unit using a negative 300v supply; however, a regulated, floating, 150v supply, or a regulated 450v supply is usually not present. The improvement in operation using regulated screen voltage is insufficient to warrant the addition of a regulated supply for that purpose alone. In the usual case, the screen current will not flow through the regulator load, and therefore the maximum current per series tube will be 100ma. This value is arrived at by allowing for maximum screen current consumption and 10% cathode current derating of the 6098.

2.3 *Amplifier Circuit:* The regulator amplifier has two cascaded twin-triode stages (i. e., the plates of the input stage feed the grids of the output stage). The input stage, V5, is a balanced differential amplifier, while the output stage, V3, is a cathode-coupled differential amplifier. [1] A change in the dc output voltage, E_o, attenuated approximately by the ratio R23/(R23+R21), appears at the grid of V5B. The gas tube, V4, keeps the voltage at the grid of V5A approximately constant. The effect of initial velocity and contact potential changes are reduced by a common cathode resistor, R19.

The balanced output of V5 is fed to the grids of V3. A single-ended output is taken from the plate of V3A and used to drive the control grids of V1 and V2.

Filter R17, C2 attenuates noise generated by gas tube V4 before it reaches the grid of V5A.

Neglecting R22, the voltage change seen at the grid of V5B for slow changes in E_o is R23/(R21+R23) of the change in E_o. For more rapid changes in E_o, R21 is bypassed by C3 and the change seen at the grid of V5B is therefore equal to the full change in E_o. Since the voltage at the grid of V5A is held constant by V4, the differential voltage seen by the grids of V5 for rapid changes in output voltage is equal to the total change in output voltage.

A series RC circuit (R9, C1) is connected between the plate and grid of V3A. This circuit provides negative feedback which reduces the gain of the output stage, thus decreasing the overall loop gain, with a resulting increase in the output impedance of the regulator at frequencies higher than 500cps. However, in the vicinity of 50kc, the feedback network produces a phase shift which prevents the regulator from becoming unstable and oscillating.

The output capacitor, C4, acts as a low output impedance at frequencies above 60kc where the gain of the amplifier is too low to be effective. It also acts to decrease the signal fed to the amplifier so that phase shift present in the loop at these high frequencies cannnot cause oscillation.

The cumulative effect of R9, C1, C3, and C4 is to produce an output impedance which decreases in magnitude from zero frequency to about 200cps

[1] George E. Valley, Jr. and Henry Wallman, ed., *Vacuum Tube Amplifiers, Rad. Lab. Series*, vol. 18, McGraw-Hill, 1948, p. 441.

due to C3, increases in magnitude from 200cps to about 50kc, then is restricted from increasing in magnitude between 50kc and 70kc by R9, C1, and decreases in magnitude between 70kc and 150kc due to C4. At about 150kc, C4 is series resonant. Above this frequency the impedance is determined by lead inductance.

The plates of the output amplifier tube, V3, are fed from a divider across the separate screen supply. The screen supply is used because even when unregulated, it varies less than the input voltage, while the divider further reduces this variation and allows optimum setting of the plate supply voltage.

2.4 *Measured Performance:* Impedance was measured in the same manner as described in section 2.5 of PC 1. Measurements taken with both regulated and unregulated screen supplies showed negligible differences. Typical results for full, half, and quarter maximum load currents are shown as solid lines in figure 5–1. All three of these curves were taken with a 4μf capacitor across the supply output. A fourth curve, shown dotted, was taken with a load of 175ma and an output capacitor of 8μf, to show the effect of increasing the output capacity. The value of 175ma was chosen to set the curve off from the 200ma curve discussed previously. The impedance is less than 1 ohm under all the conditions shown in figure 5–1, and the lack of sharp peaks in the characteristic indicates stability against oscillation.

A typical curve showing output voltage as a function of series tube plate-cathode voltage, when input voltage only is varied and screen and heater voltages are held constant, is shown by the solid line of figure 5–2. The variation of output voltage as a function of plate-cathode voltage when both screen and input voltage are varied is shown by the broken line of figure 5–2, while the variation of output voltage as a function of plate-cathode voltage when screen, input, and heater supplies are simultaneously varied is shown by the dotted line of figure 5–2. These latter two measurements were taken by connecting first the screen and input, and then the screen, input, and heater supplies to the output of a variable transformer. The relation between AC line, screen, and plate-cathode voltages is shown in figure 5–3 (page 5-5). The nominal line voltage was taken as 115v and variations were ±10% about this value. Heater voltage as a function of plate-cathode voltage is not shown, as it is an essentially

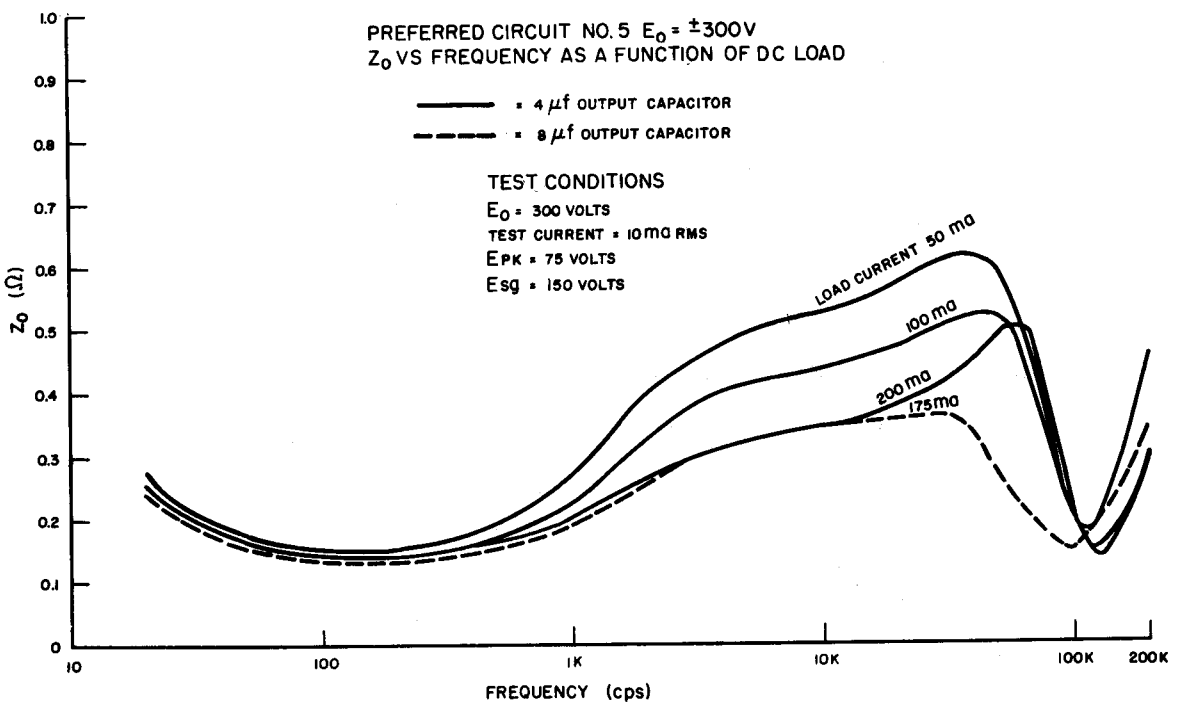


Fig 5–1

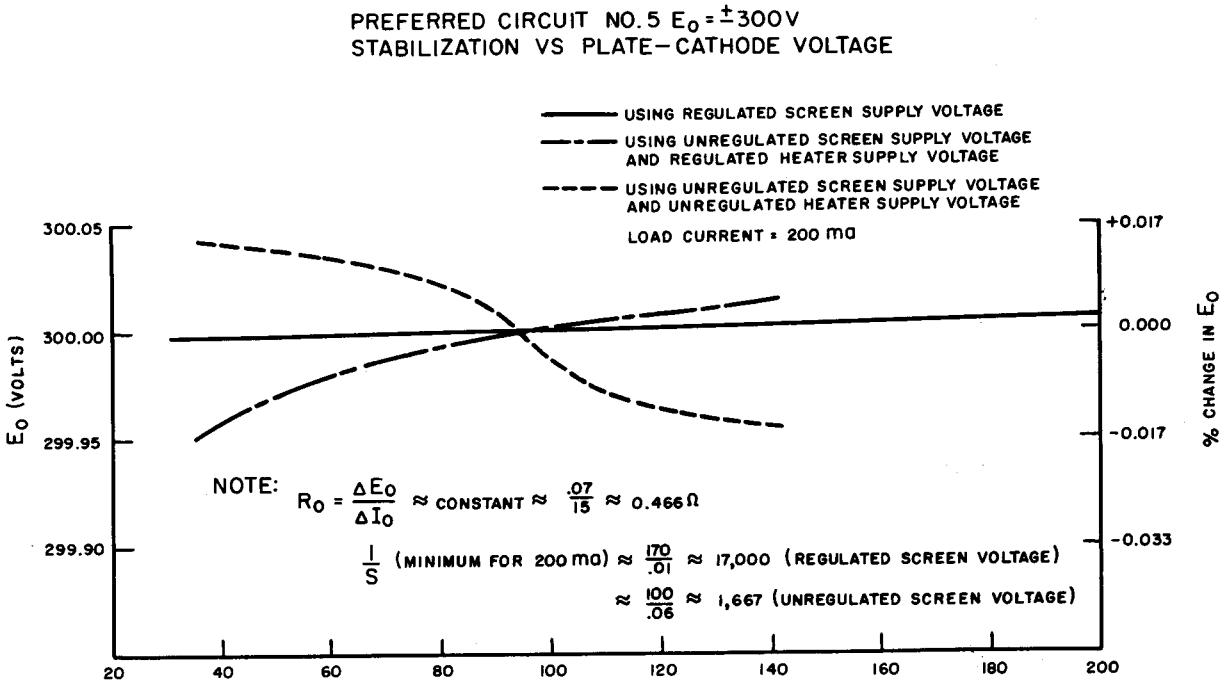


Fig 5-2

linear function of line voltage, and in general, restrictions in performance specifications are on the line rather than heater voltage.

The over-all conclusion to be drawn from the curves shown is that heater voltage variation is the prime offender in changing output voltage in PC 5. However, adding the effect of change in load current (which is 0.07v for a reduction in load current from full to quarter load), to the worst over-all variation shown, the change in output is less than 0.1% or 0.3v.

The measured dc resistance was approximately 0.47Ω. An input voltage ripple of 10v together with a screen-supply ripple of 1 volt results in an output ripple of less than 1 millivolt.

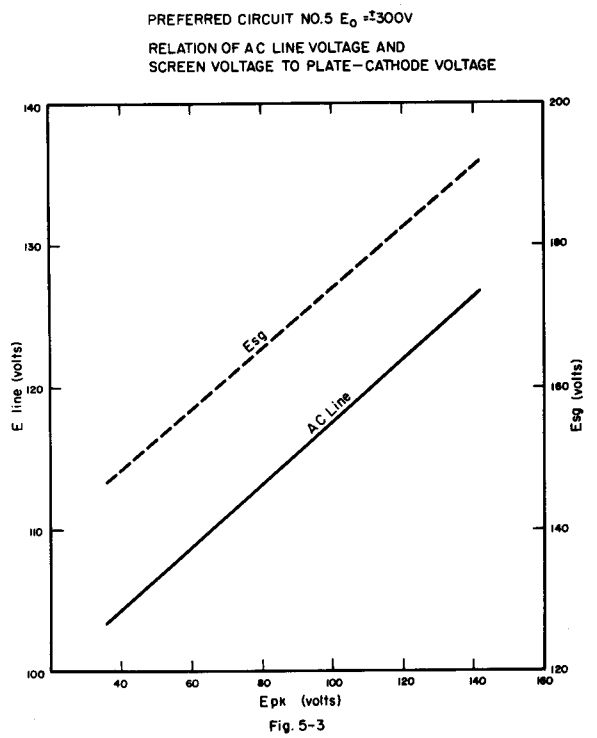


Fig. 5-3

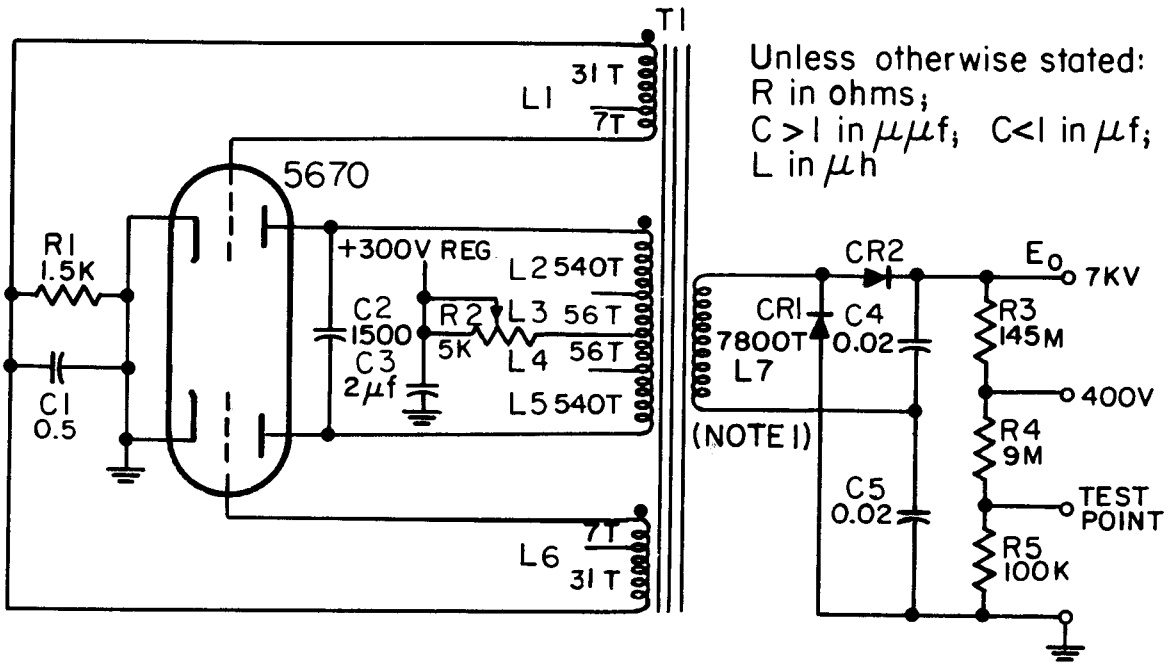
NBS PREFERRED CIRCUIT NO. 6

7 KV CRT POWER SUPPLY

475971 O - 59 - 2

NBS PREFERRED CIRCUIT NO. 6

7 KV CRT POWER SUPPLY



Components:

CR1 and CR2: Six 1N588 silicon diodes connected in series.

T1: See figure 6–1.

All R: ±10% limits. (Note 2)

All C: ±20% limits.

Operating Characteristics:

Input voltage, E_i: 300 volts dc ±1%.

Output voltage, E_o: 7 kv dc.

Ripple (peak to peak): 10 volts at 100 μa. (See figure 6–2)
14 volts at 200 μa.

Operating frequency: ≈450 cps.

Power requirements:

Maximum input power: 18 ma at 300 volts for E_o=7 kv, I_o=200 μa.

NOTES:

1. Lead from inner end of secondary should be connected to the junction of C4 and C5 to keep the maximum voltage stress between the feedback and secondary windings to $E_o/2$.

2. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified above. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.

PC 6 7 KV CRT POWER SUPPLY

1. APPLICATION

PC 6 has been designed to provide the high-voltage source for the screen grid and final anode of 5- to 12-inch cathode ray tubes.

2. DESIGN CONSIDERATIONS

2.1 *Circuit Choice:* A twin-triode tuned-plate oscillator with a high LC ratio was chosen for its general operating efficiency and its ability to continue operating with one triode section under many conditions of failure on the part of the other triode section. In addition, fewer resistors and capacitors are required for this circuit than for a single pentode performing the same function. (See Notes to the Preferred Circuits Manual, section 14.)

Further, it has been found that a sealed unit containing a universal transformer-rectifier filter can be designed for use in either a vacuum tube or transistor dc-to-dc converter. This design is a potential contribution toward minimization of the logistic problem, since a single replacement unit could be produced for use with either type of circuit.

2.2 *Tube Choice:* The 5670 twin triode was chosen because it is a military preferred tube type which satisfies the circuit requirements and appears frequently in associated circuits. Higher μ tubes have too high a plate resistance and somewhat lower plate dissipation; lower μ tubes require a greater number of feedback turns and do not have sufficiently low plate resistance to compensate for the increased grid drive at the power levels required for this circuit.

2.3 *High-Voltage Transformer:* The core of the high-voltage transformer (fig. 6–1) is made of nickel-iron U laminations. This material has a square-loop hysteresis curve and a high permeability which permits a minimum of primary turns for a given input voltage and flux density. For winding ease, the U lamination has advantages over the wound toroidal construction. Also, the toroidal construction is difficult because of the insulation requirements of the high-voltage winding. This insulation is more readily applied if layer-winding techniques are employed.

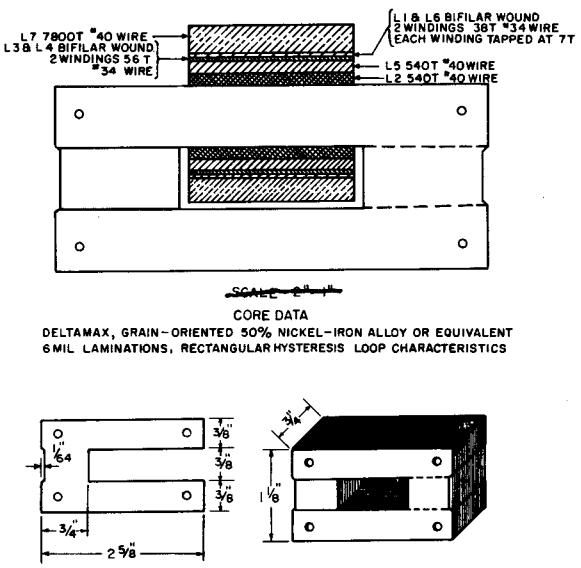


Figure 6–1—Construction details of high-voltage transformer

The transformer is so designed that it may be used either for tube or transistor operated supplies. The tube unit operates from a 300-volt supply, whereas the transistor unit will operate from a 25-volt supply. A voltage of 25 volts was chosen as the one most likely to become a standard regulated voltage for transistor use. The next higher voltage likely to become standard is 50 volts, and this is too high to provide any safety margin, even for transistors with 100-volt peak inverse rating.

No attempt has been made to optimize the size and weight of the transformer shown in figure 6–1. The choice of number of turns and physical core size was a compromise between ease of construction, size, and weight, as opposed to power efficiency. If advanced construction techniques make possible a better transformer design, then the improved transformer may be substituted without any circuit changes being required in PC 6.

The primary is wound in two sections. The inner section contains the major portion of the primary and is layer wound. The second section contains the portion of the primary designed for use with transistors and is bifilar wound to reduce overshoots caused by leakage

inductance. The energy stored in the leakage inductance tends to dissipate via the off transistor, unless this energy can be closely coupled to a dissipative path through the transistor that is conducting. Bifilar winding provides this close coupling. The problem of leakage-induced reverse emf is not as great in the case of tube oscillators, and the mitigating effect of the bifilar coupling is not as complete since the greater portion of the primary is not bifilar wound. The technique of using bifilar windings in one section of the primary does decrease overshoots, however, and creates but a nominal insulation problem. Complete bifilar winding would create a greater insulation problem because of the larger difference in potential between the end turns. In the bifilar portion of the primary, larger wire is used for carrying the greater current in the lower voltage transistor case.

2.4 *Test Point:* To allow measurement of the dc output voltage without special equipment, such as high-voltage probes, etc., a tap is provided on the high-voltage bleeder for connecting a microammeter between the test point and ground. The resistance of the microammeter will be very small with respect to the 100,000-ohm portion of the bleeder resistor; therefore, such connection is physically equivalent to inserting the microammeter in series with the 154 MΩ bleeder. Since the 154 MΩ bleeder will not be made up of precision resistors, the case containing transformer, rectifier, filter, and bleeder must have the number of microamperes corresponding to 7 kv printed on it. This calibration would take place in final test, and therefore the inscription on the case does not unduly complicate unit production.

2.5 *Screen Grid Voltage:* A second tap on the high-voltage bleeder provides 400 volts for the screen grid of the cathode-ray tube. Alternatively, the screen grid may be fed from the regulated +300-volt supply.

2.6 *Theory of Operation:* The oscillator operates in a switching rather than in a sinusoidal mode. Vecchiacci [1] has explained the operation of a single-ended oscillator of this type and has shown that such operation depends on the LC ratio in the plate circuit being much greater than R^2, where R is the resistance in series with the plate supply (this includes plate resistance of the tube when biased on). Preferred Circuit 6 differs from the single-ended circuit described by Vecchiacci in that it is connected in push pull and makes use of the saturating characteristics of the square-loop core to initiate tube saturation and to determine the operating frequency.

The operation of PC 6 is similar to that of the common transistor dc to dc converter. The transformer as specified, with a two section primary and a tapped feedback winding, can be used in a transistorized high-voltage supply. No change need be made in the rectifier filter or the output taps.

2.7 *Operation With One Triode Section Inoperative:* Under some conditions of failure of one triode section, PC 6 will continue to operate but with reduced output voltage. These failure conditions are deteriorated cathode and other effects tending to decrease transconductance or disconnect tube elements. Failure during a mission will cause increased indicator tube deflection, thus bringing the failure to the attention of the operator. The operator can usually bring the voltage up to normal by adjusting the variable resistor R2 in the oscillator place circuit, if time allows, or he can continue to operate with somewhat decreased effectiveness if failure of a triode section occurs at a critical moment.

2.8 *Regulation:* In general, the regulation of the supply (see fig. 6–2) will be sufficient for most uses with no additional circuitry. Should reduction of output resistance be desirable, regulators can be added in series with the dc supply. For reduction of output ripple and output impetance, regulators can be added between the negative terminal of the high voltage and ground. The output voltage stability can be improved by the use of a regulator in the plate circuit of the oscillator, but such a regulator becomes rather complex

[1] F. Vecchiacci, (in English) "Oscillations in the Circuit of a Strongly Damped Triode," Proc. IRE, Vol. 13, No. 5, May 1931 (an incomplete translation); (in Italian) "Sul Funzionamento Oscillatoria Dei Circuiti," Nuovo Ciempo, 1930, p. 172.

if stability better than the approximately ±1% available from PC 6 is desired.

3. MEASURED PERFORMANCE

An oscillator type high-voltage power supply such as PC 6 has a bleeder resistor connected across the output as an integral part of the circuit. This resistor is usually encapsulated, along with the output filter capacitors and associated parts.

3.1 *Output Characteristics as a Function of Load Current:* Electromagnetic cathode-ray tube final-anode currents, in general, average less than 100 μa. The curves for PC 6 (figs. 6–2, 6–3, and 6–4) are plotted considerably beyond this point to demonstrate operating characteristics at extended current ranges.

The relationship between output voltage and current is shown in figure 6–2. The change in output voltage for a change in load current of 100 μa is less than 5%.

The effect of changing tube parameters is shown in figure 6–3. It will be noted that the tubes used include types 2C51 and 6J6 in addition to the preferred type 5670. The 5670's available were so closely matched that no significant data were provided. The data obtained from the seventeen 5670's tried would have given one thick line. As a consequence, tubes of other types were chosen to determine the effect of changing tube parameters. The 2C51 is essentially a 6J6 with separate cathode leads, while the 5670 is the military preferred version of the 2C51.

For the initial curve of figure 6–3, tube 2C51 No. 2 was used; the variable resistor R2 in the +300-volt supply lead was set to the value necessary for an output voltage of 7000 volts with zero load current, and then output voltage versus load current was plotted. For the other curves, except the broken-line curve, the several tubes indicated were substituted without changing the resistor R2. For the broken-line curve, the tube 6J6 No. 2 was left in the socket, R2 adjusted for an output of 7 kv at zero load current, and the curve re-run. This particular tube was chosen because its output differed most from the initial voltage output. From this curve we see that the tube parameters have at most a second order effect on the output voltage versus load current characteristic.

Figure 6–3 indicates the μ to be the controlling factor in the output voltage versus tube parameter relationship. One would expect this since the tube operates in a switching mode;

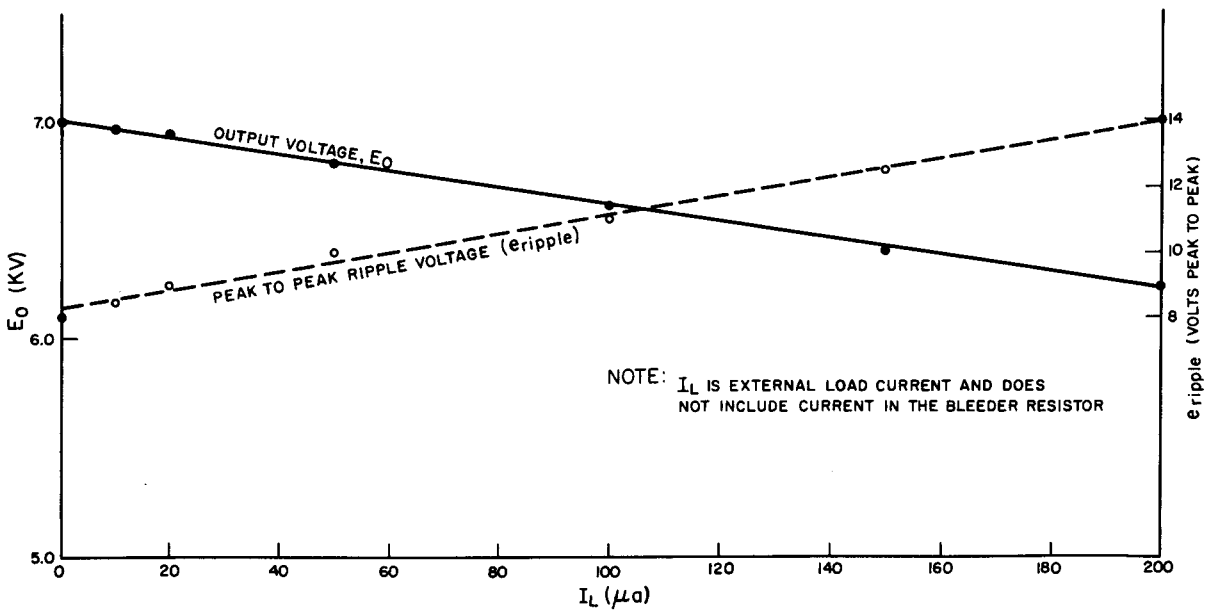


Figure 6–2—Characteristics of PC 6 with both halves of twin triode operative

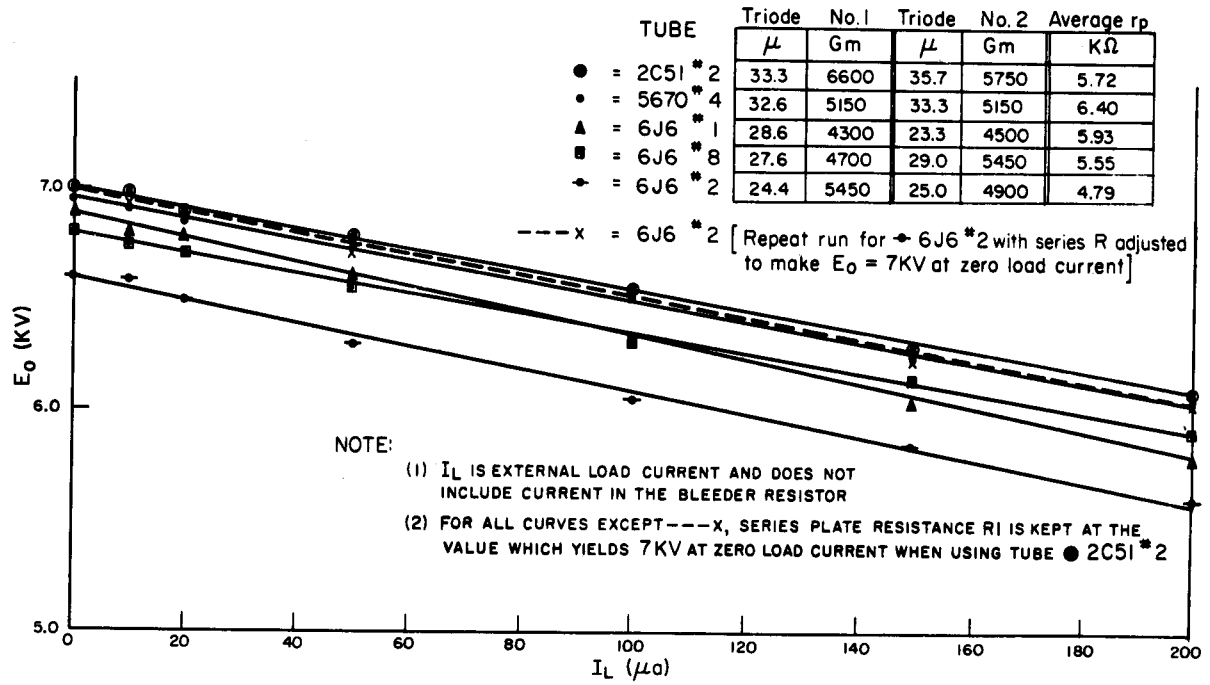


Figure 6–3—Variation of output voltage as a function of tube parameters

therefore, when the μ is higher, the positive grid drive to the on triode is greater, and the forward resistance of the on triode is less. The minimum μ for the 5670WA, according to MIL–E–1/247, is 26. The curve for tube 6J6 No. 2, which has an average μ of about 24.7, illustrates the lower limit of performance. The maximum value of μ under MIL–E–1/247 is 44. The highest average value of μ available for test was 34.5. This is significantly less than the maximum value, 44, of the tube specification. From an extrapolation of tube output versus μ of the tubes tested, it was determined that a tube with a μ of 44 would yield an output of 7150 volts. The rate of change of output voltage as a function of μ for a given output load increases as μ decreases. This nonlinearity may be attributed to two effects, both of which result from increasing the effective grid drive: (1) the nonlinear change of the forward resistance of the triode when in the on position, and (2) the small reduction of total circuit resistance, $R_{transformer}+R2+R_p$, caused by the reduction of the on-tube forward resistance, R_p. Increasing the μ of the tube effectively provides a greater positive grid drive which tends to decrease the series resistance of the tube when in the on condition. However, increasing the effective series drive to the on-tube grid also tends to decrease the grid input resistance and thus to load the source of grid drive; this loading, in turn, somewhat negates part of the effectiveness of the increased effective grid drive. Further, since R2 and $R_{transformer}$ remain constant, the relative effect of decreasing the plate resistance of the triode lessens. Thus a tube with a μ near the upper limit will increase the output voltage by approximately 2% when inserted in the socket prior to readjustment of the series resistor R2.

Figure 6–4 shows the operating characteristics of the supply with one triode section of the twin triode inoperative. The data were obtained by first adjusting the circuit, with both triode sections operating, to have an output voltage of 7 kv when working into an open circuit. (These were also the initial conditions used for obtaining the curves of figure 6–2.) The plate lead to one of the triode sections was

then disconnected and the test re-run. The data, therefore, represent the results obtained when one of the triode sections becomes inoperative due to causes such as reduced emission, open cathode, open plate, etc.

3.2 *Output Characteristics as a Function of Heater Voltage:* Tests made to determine the effect of heater voltage variation show no measurable change in output over the range of 6.3 volts ±10%.

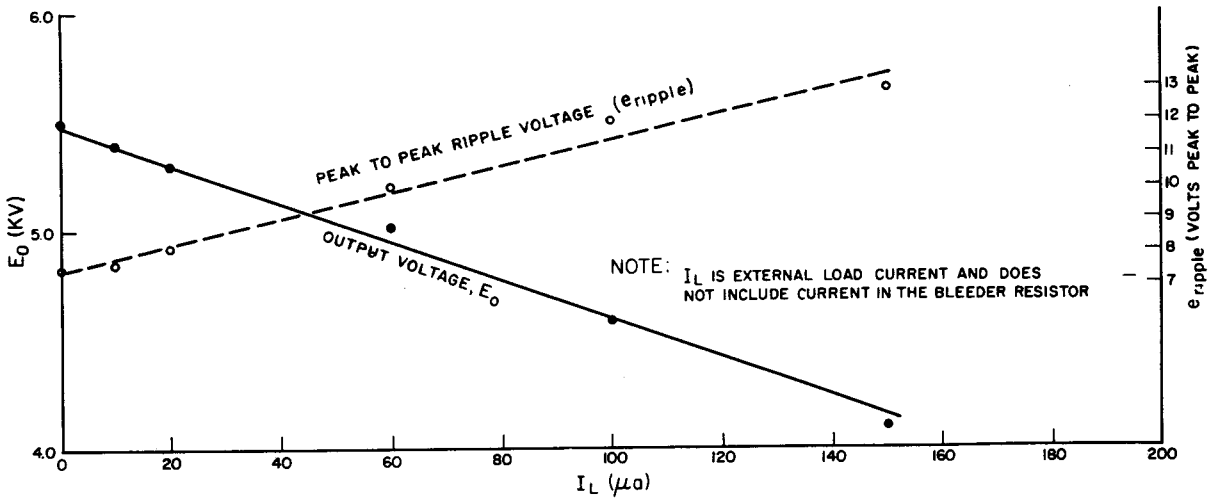
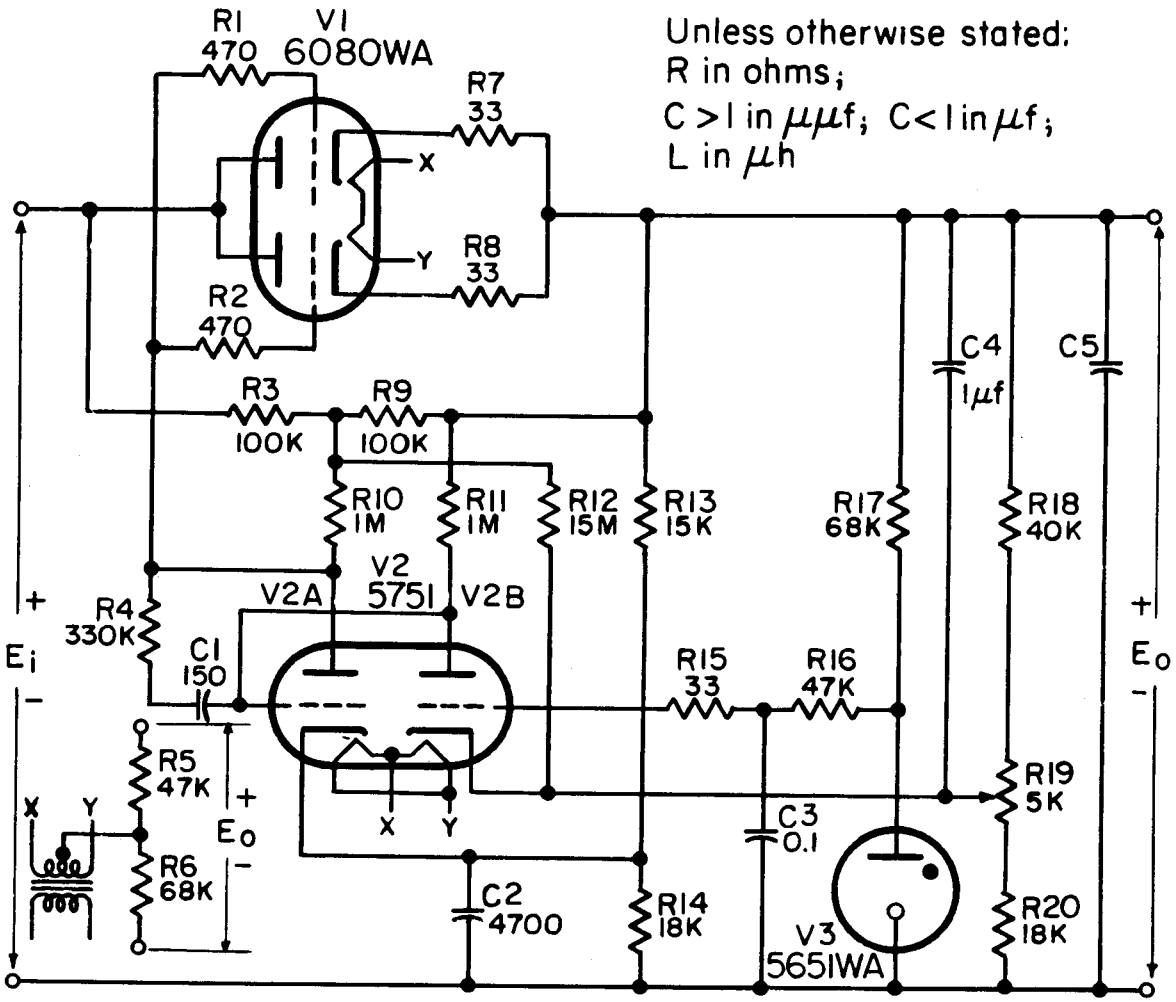


Figure 6–4—Characteristics of PC 6 with one half of twin triode inoperative

NBS PREFERRED CIRCUIT NO. 7
DC REGULATOR FOR PLUS OR MINUS 250 VOLTS: 1% REGULATION

NBS PREFERRED CIRCUIT NO. 7

DC REGULATOR ±250 VOLTS: 1% REGULATION



(For specifications, see next page.)

Components:

C5 (minimum): 4 μf.

R18,R19,R20: Wire-wound or other temperature stable type; use equal watts per ohm in each arm of the divider.

R18,R20: ±1% limits; R7,R8,R13,R14,R19: ±5% limits; R4: ±10% limits; all other R: ±20% limits. (Note 1)

All C: ±20% limits.

Operating characteristics:

Input voltage, E_i:

Minimum ~~300~~ volts dc. 300V

Maximum 400 volts dc at 10 ma minimum load per triode section; 430 volts dc at 25 ma minimum load per triode section.

Output voltage, E_o: ±250 volts dc. (Note 2)

Output current:

Minimum 10 ma per triode section.

Maximum 125 ma for single 6080WA triode section; 100 ma per triode section when two or more sections are paralleled.

Output resistance, R_o: ≈0.33Ω.

Output impedance, Z_o: <2Ω from dc to 100 kc. (See fig. 7-3.)

Stabilization ratio, S: <0.002.

Ripple gain at 120 cps: ≈1000.

NOTES:

1. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified above. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.

2. Ground one side of the regulated output to obtain the desired polarity. For negative output the input voltage must be ungrounded. positive input Terminal must not be grounded.

PC 7 DC REGULATOR ±250 VOLTS: 1% REGULATION

1. APPLICATION

PC 7 is intended for use with an unregulated dc power source to provide ripple reduction, low output impedance, and stability against changes in input voltage and output load. The circuit was chosen to meet the many needs for a low impedance supply with a self-contained reference source which will provide 1% regulation. Regulation is used here to mean the constancy of the output voltage with line voltage and load changes; it does not include output voltage changes which are caused by aging of components or by changes in the environment in which the circuit operates. The limits placed on the component values on page 7–3 are those necessary to achieve 1% regulation in spite of combined line voltage and load changes within the range specified. The 250 volts is set initially by means of potentiometer R19.

The stability of the circuit with time and with changes in environment is a function of the components within the circuit, principally the stability of the reference voltage provided by the gas tube, V3, and of the components in the divider which supplies the cathode of the input stage of the amplifier, V2B. The user must choose components for these circuits that will meet his stability requirements under the environmental and aging conditions that are expected in his application.

2. DESIGN CONSIDERATIONS

The circuit configuration, tube complement, and most component values of PC 7 are the same as those of PC 3A, the ±300 volt dc regulator. Changes in six resistor values were required to obtain the lower output voltage and to recenter the operating range of the dc amplifier, V2.

2.1 *Series Tube:* The 6080WA and equivalents were chosen because of their low static plate resistance and ±300 volt heater to cathode voltage rating. Cathode resistors are included to obtain self-bias which tends to equalize the plate currents when triode sections are connected in parallel. The grid resistors are parasitic oscillation suppressors.

2.2 *Amplifier Circuit:* The 5751 and electrical equivalents were chosen for the amplifier because of their recurrence in equipment design and their generally satisfactory performance. The plate feed for the output section is taken from a voltage divider across the series tube to decrease the plate swing required of the output section of the amplifier tube, V2A.

At conditions of low input voltage and high load current, the series tube requires very little negative bias; hence its grid voltage will practically equal the cathode voltage. This would be impossible to accomplish if the output section of the amplifier tube, V2A, were fed from the regulated output. One alternative is to return the plate load resistor of V2A to the unregulated supply. With this arrangement, low series tube biases are easily obtained. At conditions of high input voltage and low load current, however, the series tube must offer a high resistance and hence requires a high negative bias. Since the need for higher bias is accompanied by an increase in the plate supply voltage of V2A, a large plate voltage swing is required. With this arrangement it is difficult to design the amplifier, V2A, with a reasonable plate load resistance and at the same time prevent driving its grid positive under high input voltage, low load current conditions.

The use of the divider across the series tube is a compromise between the better linearity of operation obtained at low input voltage and high load current when the unregulated input potential is used as the plate supply for the final amplifier, V2A, and the better gain and lower plate swing required under normal operating conditions when the regulated output voltage is used.

The circuit is very sensitive to changes in the sampling divider, R18, R19, and R20. Resistors whose wattage ratings are very conservative should be employed, and to insure that one resistor will not change in value relatively more than another, the wattages should be in the same ratio as the power dissipation. This

factor is one of the most critical aspects of regulator stability. The range of adjustment required in potentiometer R19 is determined by the tolerances of the components in the reference circuit, principally the operating voltage of the reference tube, V3. This range is limited to the minimum which will permit setting the output voltage to 250 volts in the event that all tolerances add in the direction which causes maximum deviation. Even though this requires 1% limits on the fixed resistors of the divider, it facilitates initial adjustment of the circuit and lessens the possibility of gross misadjustment. Capacitor C4 increases the loop gain at audio frequencies by coupling directly from the regulator output to the input of the comparing circuit.

The feedback network R4, C1 provides frequency selective negative feedback across the output stage of the regulator amplifier. This decreases the regulator high frequency output impedance at the cost of increased mid-frequency impedance. Resistor R12 decreases output resistance and increases stabilization by feeding a portion of the input voltage change to the regulator-amplifier cathode.

2.3 *Reference Circuit:* Although complete comparison data are not available, the 5651WA and electrical equivalents appear to be the most stable glow discharge devices available. The 5651WA is fed from the regulated output. The choice of current is a compromise between higher noise level at low currents and shortened life at high currents. The bypass capacitor and resistor network R16, C3 is designed to attenuate the transient noise spikes characteristic of glow discharge tubes. R15 is a parasitic oscillation suppressor.

3. PERFORMANCE

This section includes a definition of regulator circuit performance terms and information on the test methods used to obtain the performance characteristics.

3.1 *Definition of terms:*

(a) Stabilization Ratio—S: The ratio of the change in output voltage to the change in input voltage with constant load current. The inverse ratio, $1/S$, is also used.

(b) DC Output Resistance—R_o: The ratio of the change in output voltage to the change in output current with the input voltage held constant.

(c) Output Impedance—Z_o: The ratio of the ac components of output voltage and current when the load is varied sinusoidally with the input voltage held constant.

(d) Ripple Gain—e_i/e_o (120 cps): The ratio of the ac components of input voltage to output voltage at the ripple frequency. The frequency of 120 cps is selected as the lowest frequency usually encountered.

3.2 *Methods of Measurement:* The test supply used for measurements on the dc regulator is shown in figure 7–1 accompanied by a curve showing its output impedance as a function of frequency. It is a simulated unregulated supply formed by adding series resistance and shunt capacitance to a standard laboratory regulated supply. This was done to prevent power source ripple from masking the output impedance measurements. Figure 7–2 shows the test set-up for deriving the impedance curves.[1,2] For ripple gain measurements, 120 cycle ripple may be inserted between the 10 μf capacitor and ground.

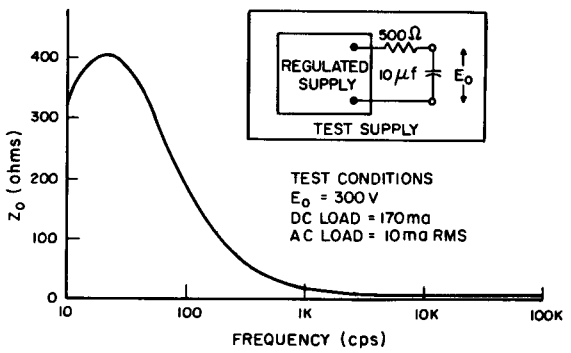


Figure 7–1.—Output impedance of test supply. The peak in the vicinity of 20 cps is caused by the resonance of the LC filter in the regulated supply

[1] J. H. Hersey, "Dynamic Impedance of Regulated Power Supplies," Bell Lab. Rec., vol. 27, June 1949, p. 216.

[2] "Standards on Television: Methods of Measurement of Electronically Regulated Power Supplies, 1950," Proc. IRE, vol. 39, Jan. 1951, p. 29. See par. 3.5.2 and fig. 3.

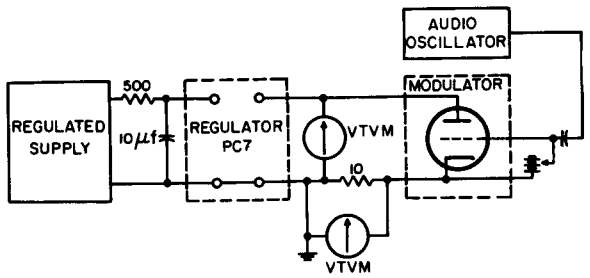


Figure 7–2.—Test circuit for measuring output impedance of a voltage regulator

3.3 *Measured Performance:* In figure 7–3, typical impedance curves of the combined regulator and supply are shown as a function of load current. Since reduction of impedance is a function of the series tube transconductance, and transconductance is a function of tube current, the increase of effective impedance with decrease in load current is expected.

Typical curves showing output voltage as a function of input voltage are given in figure 7–4. The solid lines show the relationship when design center parameters are used in the circuit. The dotted lines show the relationship under minimum performance conditions resulting from the use of low mu series and amplifier tubes, and resistor values chosen within their allowable limits to give poor performance. Circuit performance could conceivably be poorer than that shown by the dotted lines; however, the chance of each parameter changing in such a direction as to cause poorer operation is very small.

The dc resistance of the regulator was measured to be approximately 0.33Ω. This remains essentially constant even under poor operating conditions, as may be verified by the constant distance between the curves of figure 7–4. An input voltage ripple of 10v results in an output ripple of less than 10mv.

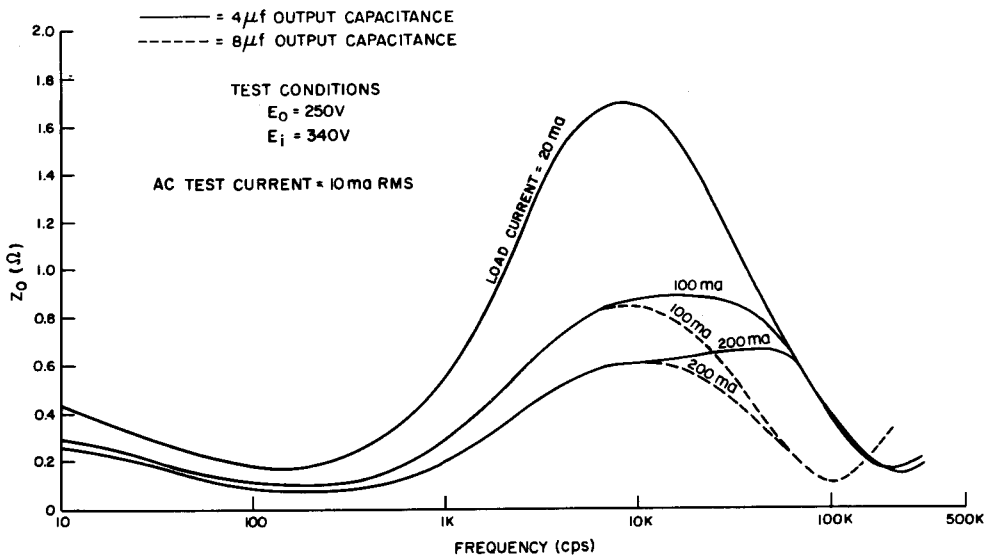


Figure 7–3.—Output impedance as a function of frequency and dc load

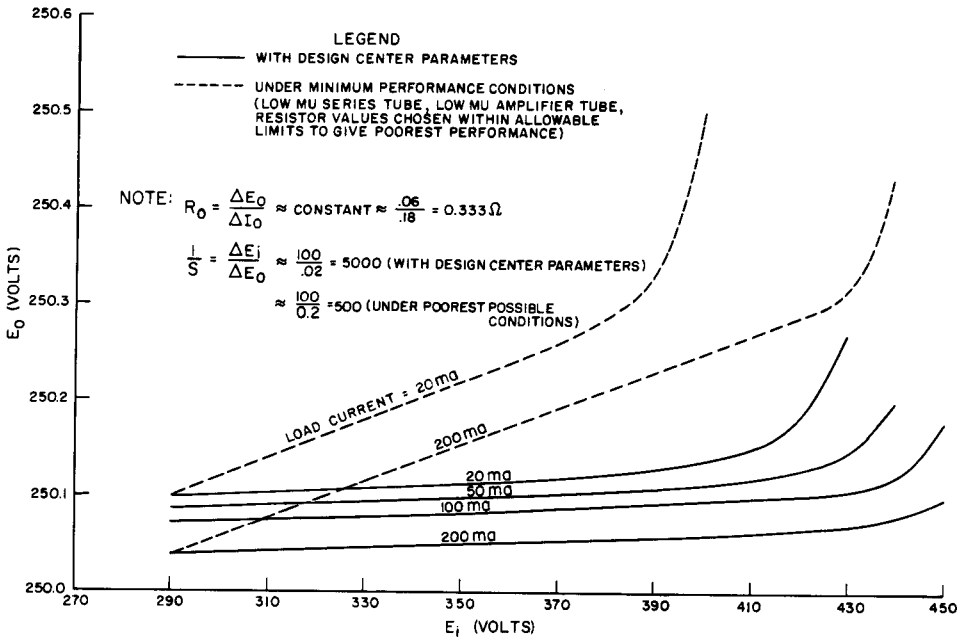


Figure 7–4.—Output voltage versus input voltage as a function of load current

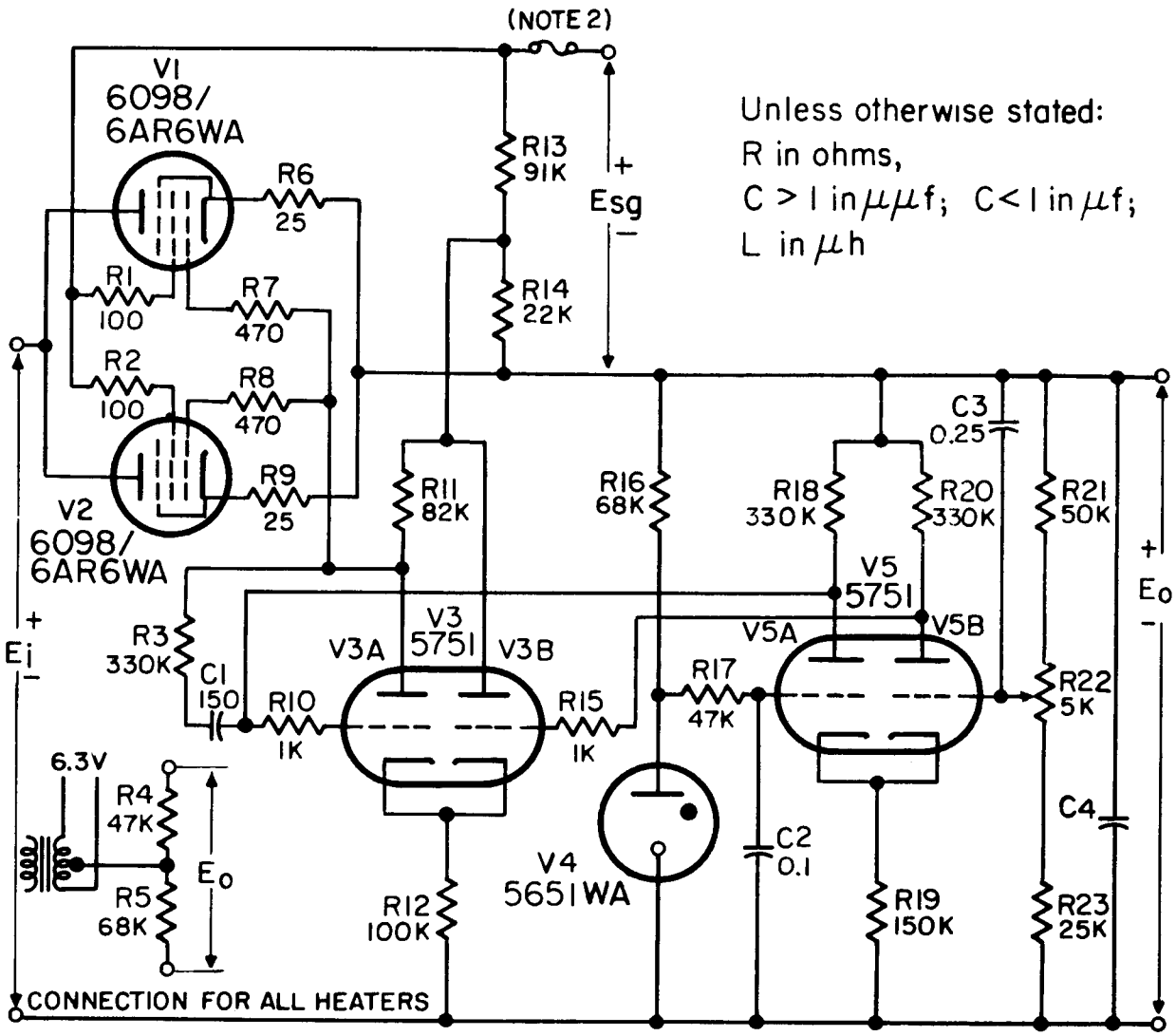
NBS PREFERRED CIRCUIT NO. 8

DC REGULATOR FOR PLUS OR MINUS 250 VOLTS: 0.1% REGULATION

475971 O - 59 - 3

NBS PREFERRED CIRCUIT NO. 8

DC REGULATOR ±250 VOLTS: 0.1% REGULATION



(For specifications, see next page)

Components:

C4 (minimum): 4 μf

R6,R9,R16,R19,R21,R22,R23: Wire-wound or other temperature stable type. Use equal watts per ohm in each arm of the reference divider.

R19,R21,R23: $\pm 1\%$ limits; R6 R9: $\pm 2\%$ limits; R16,R22: $\pm 5\%$ limits; R3,R11,R12,R13, R14,R18,R20: $\pm 10\%$ limits; all other R: $\pm 20\%$ limits. (Note 1.)

C1: $\pm 10\%$ limits; all other C: $\pm 20\%$ limits.

Operating characteristics:

Input voltage, E_i: Minimum 290 volts dc.

Screen voltage, E_{s_g}: Minimum 150 volts dc. (Note 2.)
Maximum 200 volts dc.

Output voltage, E_o: ± 250 volts dc. (Note 3)

Output current: Minimum 10 ma per series tube.
Maximum 100 ma per series tube.

Output resistance, R_o: $\approx 0.22\Omega$.

Output impedance, Z_o: $<1\Omega$ from dc to 100 kc. (See figure 8–1.)

Stabilization ratio, S: <0.0013.

Ripple gain at 120 cps: $>10{,}000$.

NOTES:

1. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified above. Thus, the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.

2. The screen voltage is measured with respect to the 250 volt regulated output. The screen supply must be capable of delivering 12.5 ma per series tube and should be fused at 20 ma per series tube to prevent damage to the screen if the input voltage is off while the screen supply is on. If an unregulated supply is used, maximum permissible ripple is 1 volt rms.

3. Ground one side of the regulated output to obtain the desired polarity. For negative outputs the input voltage must be ungrounded. The positive input terminal must not be grounded

PC 8 DC REGULATOR ±250 VOLTS: 0.1% REGULATION

1. APPLICATION

PC 8 is designed for use in applications requiring better regulation and stability than can be obtained from PC 7. Regulation is used here to mean the constancy of the output voltage with line voltage and load changes; it does not include output voltage changes which are caused by aging of components or by changes in the environment in which the circuit operates. The limits placed on the component values on page 8-3 are those necessary to achieve 0.1% regulation in spite of combined line voltage and load changes within the range specified.

The stability of the circuit with time and with changes in environment is a function of the components within the reference and comparison circuits. The user must choose components that are stable enough to meet his requirements under the environmental and aging conditions that are expected in his application.

2. DESIGN CONSIDERATIONS

The circuit configuration, tube complement, and most component values of PC 8 are the same as those of PC 5, the ±300 volt dc regulator. Changes in six resistor values were required to obtain the lower output voltage and to recenter the operating range of the amplifier stages.

2.1 *Series Tube:* A pentode-connected 6098/6AR6WA* was chosen as the series tube for this circuit because, compared with a low-mu triode, it requires less control grid voltage variation to compensate for a given change in load current or line voltage, and thereby allows considerable simplification in the amplifier circuit. This advantage more than makes up for the added complexity and increased power consumption of the screen-voltage supply.

The improvement in operation obtained by use of a regulated screen voltage is insufficient to warrant the addition of a regulated supply for that purpose alone. If an unregulated screen supply is used, its voltage with respect to the regulated 250 volts must remain within the 150 to 200 volt range specified, and its maximum ripple should be one volt rms. For a positive 250-volt supply, a floating screen supply may be used if a supply voltage of 400 to 450 volts with respect to ground is not available. A maximum screen current of 12.5 ma per series tube is required to assure proper operation when the series tube is passing maximum load current.

2.2 *Amplifier Circuit:* The regulator amplifier consists of a balanced differential amplifier input stage, V5, cascaded with a cathode-coupled differential amplifer, V3, used as the output stage.[1] Changes in the regulated output voltage, E_o, appear at one of the grids of the input stage, while the voltage at the other grid is held approximately constant by the gas tube, V4. The effects of changes in the initial velocity and in contact potential are reduced by the common cathode resistor, R19. The filter R17,C2 attenuates noise generated by the gas tube before it reaches the grid of V5A.

The balanced output of V5 is fed to the grids of V3, and the single-ended output, taken from the plate of V3A, is used to drive the control grids of the series tubes, V1 and V2. The plates of the output stage, V3, are fed from the separate screen supply because, even when it is unregulated, the screen supply voltage varies less than either the input voltage or the plate-cathode voltage of the series tube. A divider is used to obtain optimum voltage for the plate supply.

Neglecting R22, the voltage change seen at the grid of V5B for slow changes in E_o is R23/(R21+R23) of the change in E_o. For more rapid changes in E_o, R21 is bypassed by C3 and the change seen at the grid of V5B is therefore equal to the full change in E_o. Since the voltage at the grid of V5A is held constant by V4, the differential voltage seen by the grids of V5 for rapid changes in output voltage is equal to the total change in output voltage.

Potentiometer R22 is required to adjust the output voltage to 250 volts. It is needed prin-

*The 6098/6AR6WA appears in MIL-STD-200D, Navy Supplement-1A, 15 September, 1958.

[1] George E. Valley, Jr., and Henry Wallman, ed., *Vacuum Tube Amplifiers, Rad. Lab. Series*, vol. 18, McGraw-Hill, N. Y., N. Y., 1948, p. 441.

cipally because of the range of operating voltages permitted in the reference tube, V4; some additional range is required to cover the tolerances of the other components in the reference and comparison circuits. One percent limits are placed on the fixed resistors in the divider and on the cathode resistor of the input stage, and the range of the adjustment of R22 is deliberately limited to permit easy adjustment of the output voltage to within 0.1 percent of 250 volts.

A series RC circuit (R3, C1) is connected between the plate and grid of V3A. This circuit provides negative feedback which reduces the gain of the output stage, thus decreasing the over-all loop gain, with a resulting increase in the output impedance of the regulator at frequencies higher than 500 cps. In the vicinity of 50 KC, however, the feedback network produces a phase shift which prevents the regulator from becoming unstable and oscillating.

The output capacitor, C4, acts as a low output impedance at frequencies above 60 KC where the gain of the amplifier is too low to be effective. It also acts to decrease the signal fed to the amplifier so that phase shift present in the loop at these high frequencies cannot cause oscillation.

3. PERFORMANCE

For a definition of performance terms and information on the test methods used to obtain the measured performance, see PC 7, sections 3.1 and 3.2.

Typical impedance curves for the regulator are shown as a function of load current in figure 8–1. Measurements taken with both regulated and unregulated screen supplies showed negligible differences. The data for these curves were taken using 90 volts from series tube plate to cathode and 150 volts from screen to cathode, with one exception. Since high screen voltages cause an increase in impedance at low load currents, data were taken using 200 volts from screen to cathode at a load current of 20 ma to obtain the maximum impedance curve. The impedance is less than 1 ohm under all the conditions shown in the figure, and the lack of sharp peaks in the characteristic indicates stability against oscillation.

Typical curves showing output voltage as a function of input voltage, load current, and line voltage are given in figure 8–2. As indicated by the solid lines, the output voltage does not change more than 0.05 volts (0.02%) in spite of load changes from 200 to 20 ma and input voltage changes from 290 to 470 volts, if the screen and heater supplies are regulated. The dotted lines show the performance when unregulated screen and heater supply voltages are used. For these measurements a $\pm 10\%$ change in line voltage is simulated by varying input, screen, and heater voltages $\pm 10\%$. The center values, indicated by the plotted point, P, on each curve, are chosen to obtain operation near the limits specified for the circuit. Under these conditions, a change in load is accompanied by both a change in input voltage due to the resistance of the unregulated supply and a change in screen voltage because of the changing screen current requirements. Using a 500Ω supply for the input and a 1300Ω unregulated supply for the screen, the regulation was still better than the 0.1% specified for the circuit.

The dc resistance of the regulator was measured to be approximately 0.22Ω. An input voltage ripple of 1 volt results in an output ripple of less than 1 millivolt.

An input Ripple of 10 v Together with a Screen Supply Ripple of 1.0 v Results in an output Ripple of Less than 1.0 millivolt

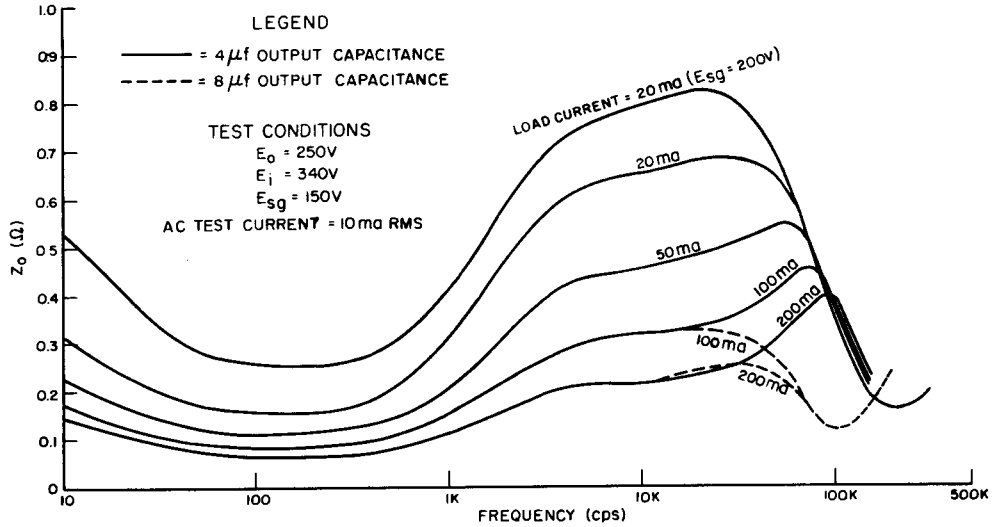


Figure 8-1.—Output impedance as a function of frequency and dc load

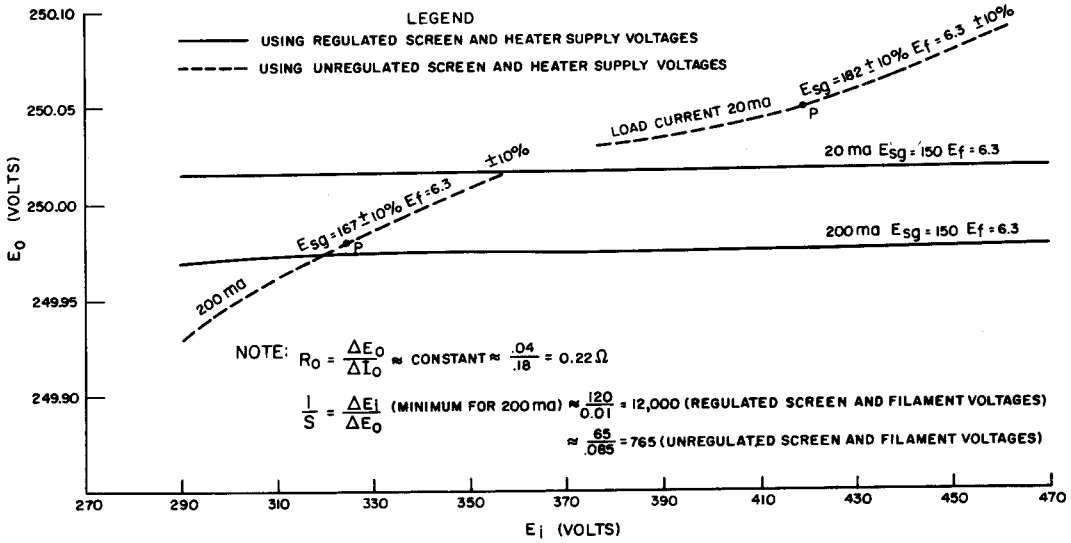
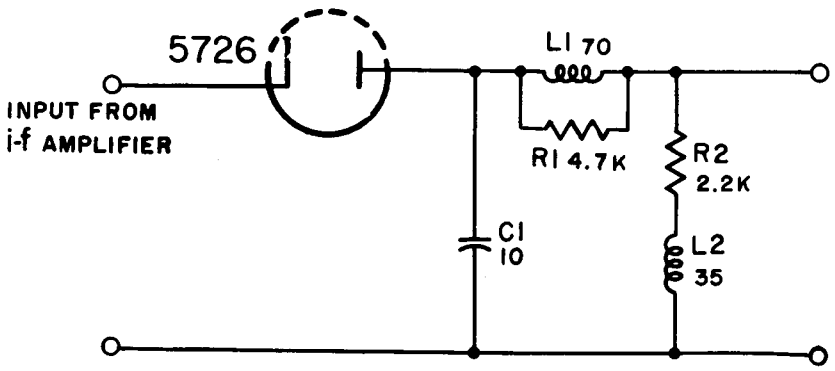


Figure 8-2.—Effects of load variations and screen and heater supply voltage changes on output voltage

NBS PREFERRED CIRCUIT NO. 20
VIDEO DETECTOR

NBS PREFERRED CIRCUIT NO. 20
VIDEO DETECTOR



UNLESS OTHERWISE STATED: R IN OHMS; C > 1 IN $\mu\mu$f, C < IN μf; L IN μh

This circuit is used to demodulate pulsed i-f signals.
Typical associated circuit is limiter, PC 21.
Video signal data:

	Input	*Output*
Waveform	i-f pulses 20–70mc.	Rectified negative pulses.
Operating level		0.6v nominal.

Fall Time: 0.07μsec.
R1,R2: $\pm$10% limits. All C: $\pm$10% limits.

NOTES:

1. The shunt capacity of the following stage is assumed to be about 14$\mu\mu$f.
2. L1 wound to be self-resonant at i-f frequency.

PC 20 VIDEO DETECTOR

1. APPLICATION

The function of this circuit is to demodulate intermediate-frequency amplified signals. It is located at the output of the last i-f stage.

2. DESIGN CONSIDERATIONS

Figure 20–1 shows the operating characteristic of the detector. Design details are individually discussed. The input is noise plus signals. The diode is connected for an output of negative pulses.

The 0.6v nominal operating level results in a 1 volt output from the cathode follower, PC 22. The cathode follower is driven by a 5654 limiter which requires a negative input signal. The limiter is driven in turn by the detector. The range of detector output is given by the curve where the linear range extends from about 0.2v to over 4v. Limiting is obtained with between −2 and −3v input.

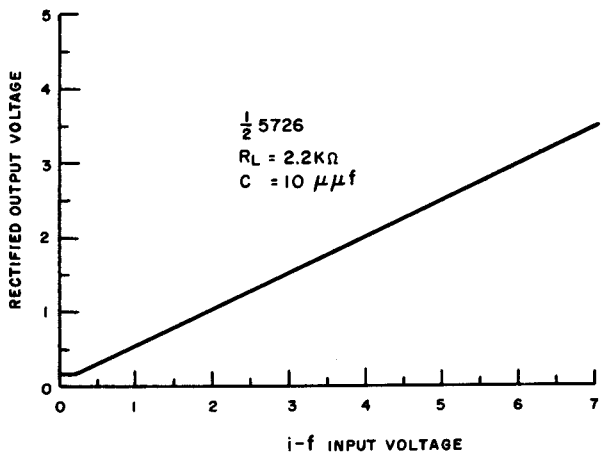


Fig. 20–1 DETECTOR CHARACTERISTIC

The fall time with compensating circuit is 0.066μsec. [1] [2] Without compensation the fall time is 0.136μsec. Allowance is made for FTC circuit capacity. Approximate capacities are

	$\mu\mu$f
5726 and wiring	4
5654 input	5
wiring	5
FTC relay	4
i–f capacitor, C1	10
	28

Fall time = $2.2\,RC = 2.2 \times 2.2 \times 10^{3} \times 28 \times 10^{-12} = 0.136\mu$sec.

If the compensation shown is used, the advantage over the uncompensated circuit is 2.06. The resulting fall time is 0.066μsec with 3% overshoot. The compensating circuit calculation is

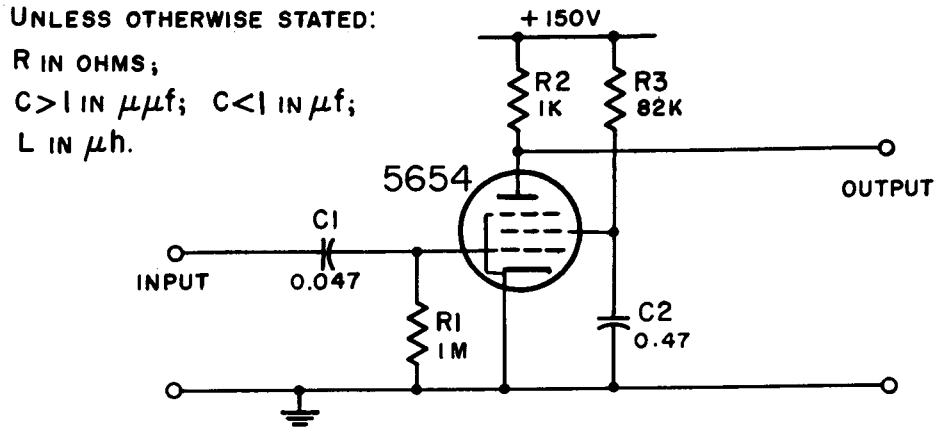
Input and output capacities = 14$\mu\mu$f each.
R2 = 2.2KΩ.
R1 = 2 × R2 = 4.4KΩ.
L1 = $(R)^2$ C.
L1 = $(2{,}200)^2 \times 14 \times 10^{-12} = 68\mu h \approx 70\mu h$.
L2 = L1/2 = 35μh.

[1] S. N. Van Voorhis, ed., *Microwave Receivers, Rad. Lab. Series*, vol. 23, McGraw-Hill, 1948, p. 192.

[2] George E. Valley, Jr. and Henry Wallman, ed., *Vacuum Tube Amplifiers, Rad. Lab. Series*, vol. 18, McGraw-Hill, 1948, p. 76.

NBS PREFERRED CIRCUIT NO. 21
VIDEO LIMITER

NBS PREFERRED CIRCUIT NO. 21
VIDEO LIMITER



This circuit is used to amplify and limit low level video signals. This limiter is usually located between the video detector and the low level cathode follower, PC 22.

Video signal data: [1]

	Input	*Output*
Waveform	Negative pulse	Positive pulse.
Operating level	0.6v	2.2v.
Limiting level		4.2v.

Rise time: 0.035μsec. [2]

Droop: 3.5% for 500μsec pulse. [3]

Tolerance: The variation of limiting level is ±30% for the MIL specification limits of tubes and ±5% resistors.

R2,R3: ±5%; R1: ±20% limits. All C: ±20% limits.

NOTES:

1. The operating levels are selected to permit cathode follower output to be 1 volt operating and 2v limiting.

2. This assumes that the total average capacity is 16μμf including output, wiring, and cathode follower input capacity.

3. For C1 = 0.01μf, C2 = 0.1μf, droop = 3.5% for 100μsec pulse.

PC 21 VIDEO LIMITER

1. APPLICATION

This circuit is used to amplify and limit low level video signals. This limiter is usually located between the video detector and the low level cathode follower, PC 22.

2. DESIGN CONSIDERATIONS

The main characteristics desired in a video limiter are linear amplification, a definite limiting level, small variation with different tubes, fast rise time, and little droop. These characteristics are discussed as applied to this limiter. This circuit is suitable for only low duty-cycle signals. The limiting level rises with increasing duty cycle. For constant limit level, a circuit with stabilized screen voltage is necessary.

The operation of this type of limiter depends upon a negative input signal driving the plate current to cutoff. The limiting level is easily measured, being the voltage across the load resistor with no input. The desired limiting level in this circuit is obtained by adjusting the screen resistor. [1]

The operating level should be about one-half of the limiting level. The limiting level is adjusted so that the cathode follower stage immediately following has a 2v output. The limiting level is 4.2v. An operating level of 2.2v results in a cathode follower output of 1 volt. The input to the limiter for this operating level is −0.6v. The linearity of the limiter is shown in figure 21-1.

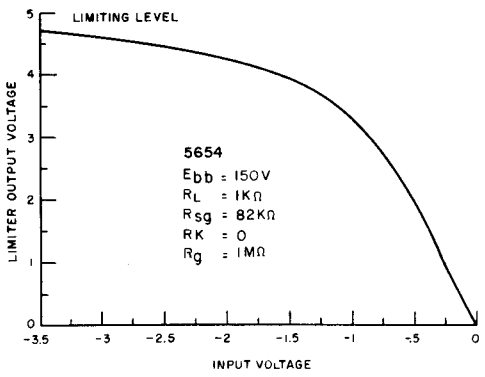


Fig. 21-1 VIDEO LIMITER CHARACTERISTICS

The variation of limiter operation with tube substitution is considerable, as shown by figure 21-2. The limiting level is plotted as a function of g_m. The spread in the points of this curve would be greatly reduced if the plate-to-screen current ratio were plotted instead of g_m; however, this ratio is not a specified characteristic. The MIL limits of the 5654 are from 3500 to 6500μmhos, or 5000μmhos ±30%. Changing of tubes has an appreciable effect because of these wide limits. The screen resistor R3 stabilizes the limiting level by degenerative feedback as opposed to fixed screen voltage. The percentage variation of limit level is ±22% for the MIL range of tubes. Since the tubes available were in the lower half of the g_m range, the data were extrapolated for the upper half. The graph shows the limiting level is higher than 4.2v. Since resistor selection is confined to 20% step values, the nearest value for R3 is 82KΩ,

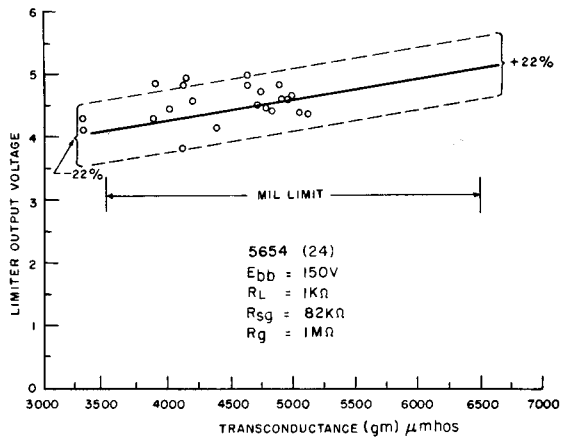


Fig. 21-2 VARIATION LIMITING LEVEL WITH TRANSCONDUCTANCE

resulting in a limit level of 4.6v. The 4.2v level is the input to the cathode follower for 2v output.

Rise time was computed for the limiter using the relation

$$t_r = 2.2RC$$

R is the plate load resistor (1KΩ) and C is the total capacity including the 5654 plate, 5670 input, socket, and wiring capacities.

[1] George E. Valley, Jr. and Henry Wallman, ed., *Vacuum Tube Amplifiers, Rad. Lab. Series*, vol. 18, McGraw-Hill, 1948, p. 86.

The output capacity of 5654 is 3.2$\mu\mu$f, maximum.

The input capacity of 5670 is for 2 sections:

$$C_{in} = C_{gp} + \frac{C_{gk}}{1 + g_m R_L}$$

C'_{gp} = 1.6$\mu\mu$f maximum 1 section

C'_{gk} = 2.7$\mu\mu$f maximum 1 section

$$C_{in} = (2 \times 1.6) + \frac{2 \times 2.7}{1 + (10{,}000 \times 10^{-6} \times 100)}$$

$$C_{in} = 3.2 + 2.7 = 5.9\mu\mu f$$

Total capacity:

	$\mu\mu$f
5654 output	3.25
5670, 2 sections	5.9
Sockets	2.0
Wiring	5.0
	16.15

Therefore

$$t_r = 2.2 \times 10^3 \times 16.15 \times 10^{-12}$$

$$t_r = 0.035\mu sec$$

Droop is a function of plate-to-grid coupling circuits and screen decoupling circuits. For small values of droop, the over-all value of droop can be obtained by taking the sum of values for individual circuits.

Input coupling: Element values 0.05μf, 1MΩ.
$RC = 10^6 \times 0.05 \times 10^{-6} =$ 50,000μsec.

For a 500μsec pulse: Droop = 500/50,000 = 1%.

Screen circuit: Element values: 0.5μf, 40KΩ (equivalent screen resistance).
$RC = 40 \times 10^3 \times 0.5 \times 10^{-6}$ = 20,000μsec.

$$\text{Droop} = \frac{500}{20{,}000} = 2.5\%.$$

Total droop = 3.5%.

For values of C1 = 0.1μf and C2 = 0.1μf, the results are 3.5% droop for a 100μsec pulse.

For variation of the plate resistor, the change is directly proportional to the variation of the resistance, e. g., $\pm$5%. For variation of screen resistor the change is $\pm$3% for a $\pm$5% resistor.

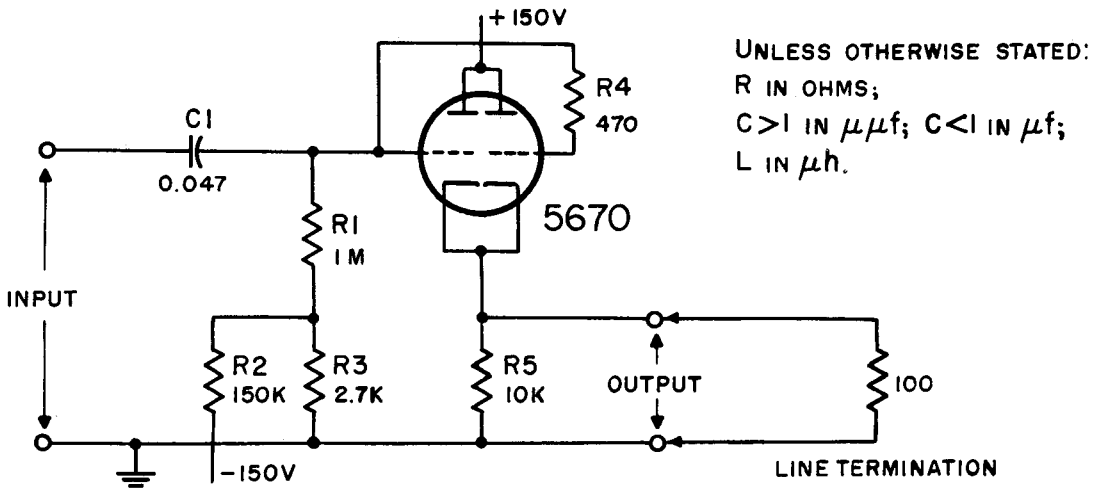
The total tolerance is

	Percent
Tube variation	$\pm$22
Plate resistor	5
Screen resistor	3
	$\pm$30

The limit level variation due to voltage variation is not included in the tolerance. The limit level changes $\pm$7% with a change of $\pm$10% in filament voltage. When the plate supply voltage is changed $\pm$5%, the limit level changes $\pm$6%.

NBS PREFERRED CIRCUIT NO. 22
LOW-LEVEL CATHODE FOLLOWER

NBS PREFERRED CIRCUIT NO. 22
LOW-LEVEL CATHODE FOLLOWER



This circuit is used to match a low-level video source, such as the limiter PC 21, to a low impedance line.
Video signal data: [1]

	Input	*Output*
Waveform	Positive pulses	Positive pulses.
Operating level	2.2v	1.0v.
Maximum output level	4.2v	2.0v.

Droop: 1% for 500μsec pulse. [2]

Tolerance: The variation of maximum output level is ±12% for MIL specification limits of tubes and ±5% resistors.

R2,R3: ±10%; R1,R4,R5: ±20% limits. All C: ±10% limits.

NOTES:

1. Levels are selected for use with limiter PC 21.
2. For C1 = 0.01μf, droop = 1% for 100μsec pulse.

PC 22 LOW-LEVEL CATHODE FOLLOWER

1. APPLICATION

The purpose of this circuit is to match the output of a low-level video stage to a low-impedance transmission line.

2. DESIGN CONSIDERATIONS

A positive input signal gives a positive output pulse.

The design is based on a normal operating level of 1 volt and a maximum level of 2v. The 2v level results from full limiting operation of the preceding limiter stage. The 2v level approaches the grid-current region of the tube and comes near the maximum that can be obtained with this type of tube.

The gain is about 0.5.

$$G = \frac{g_m R_L}{(g_m R_L + 1)}$$

$$G = \frac{10{,}000 \times 100 \times 10^{-6}}{10{,}000 \times 100 \times 10^{-6} + 1} = 0.5$$

The cathode-follower characteristic is given in figure 22–1 which shows an average for 24 tubes covering a transconductance range of 5000 to 6000μmhos. The MIL range is 5500μmhos $\pm 18\%$.

The output impedance of the cathode follower is 100Ω.

$$Z_o = \frac{1}{g_m} = 100\Omega$$

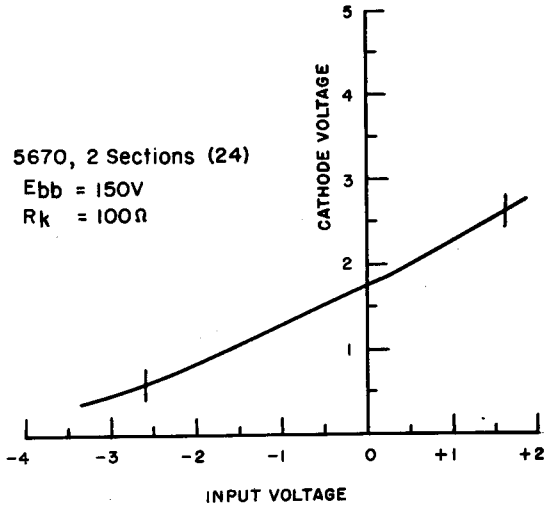


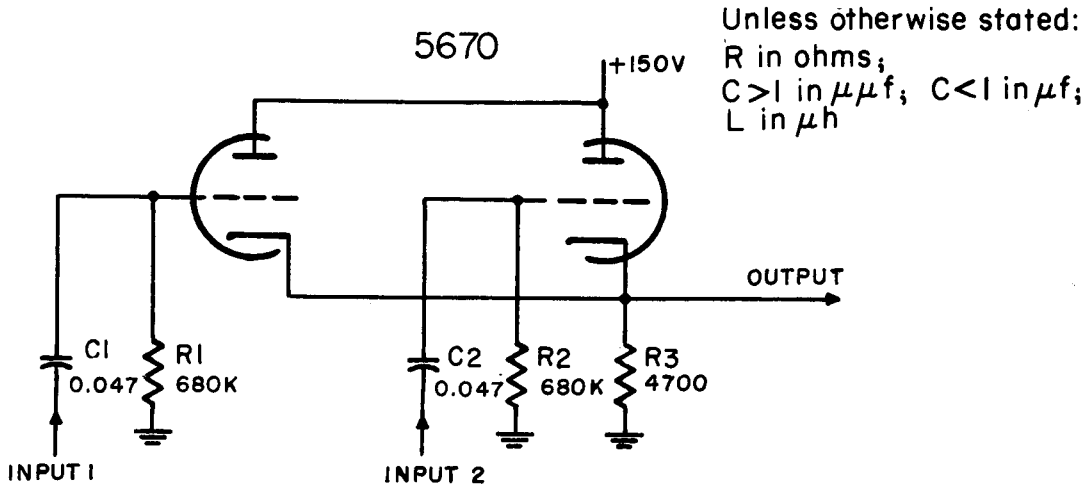
Fig. 22–1 CATHODE FOLLOWER CHARACTERISTIC

The droop is a function of the input coupling circuit (see PC 21). The droop is 1% for a 500μsec pulse.

The gain variation due to tube and resistor variations allowable by MIL specifications is $\pm 2\%$. The average g_m of one section of the 5670 is 5500μmhos. The variation of output level due to permissible variation of tubes alone is $\pm 9\%$. The variation due to cathode resistors alone is $\pm 2.5\%$ for 5% resistors. Therefore the total variation is $\pm 11.5\%$.

NBS PREFERRED CIRCUIT NO. 23
VIDEO MIXER: COMMON-CATHODE TYPE

NBS PREFERRED CIRCUIT NO. 23
VIDEO MIXER: COMMON-CATHODE TYPE



A video mixer is used to combine various forms of information such as radar video and range markers.

Inputs 1 and 2: Positive.
Gain: (as a cathode follower) 0.75.
Output: Positive.
Additive factor:[1] 20% for 4v inputs.
Rise time: 0.05μsec (with 50μμf output capacity).
Output Impedance: 500Ω.
Droop: 2% for 500μsec pulse. For input, RC time constants are noted above.

Two additional 2C51 sections may be paralleled with little change in operating characteristics, thus providing four inputs.

R3: ±10%; R1,R2: ±20% limits. All C: ±10% limits.

NOTE:

1. Additive factor in % = $100 \dfrac{\text{Output for inputs in coincidence} - \text{Output for highest input.}}{\text{Output for lowest input}}$.

PC 23 VIDEO MIXER: COMMON-CATHODE TYPE

1. APPLICATION

The primary function of this mixer is to combine various video signals and pulses. The common-cathode video mixer offers the feature of nonadditive mixing. Assume, for example, that a radar target pulse is time-coincident with a range marker. If the mixer combined the two pieces of information in an algebraic manner, the resultant signal could cause overloading in the video chain and "blooming" of the target blip at the indicator. To avoid this, the mixer should combine time-coincident inputs so that only the input with higher level appears at the output. This type of combination is nonadditive mixing.

This nonadditive feature of the common-cathode mixer is obtained by cross-biasing at the cathode by coincident positive input signals. In the strict sense, some adding is always present in the described circuit. The extent of this adding is primarily a function of the cathode resistor and the signal level. The amount of adding that is tolerable is determined by the type of information to be combined and the composition of the video chain.

TABLE *23-1—Video Mixer: Common Cathode Type*
2C51
E_{bb} = +150v

Output (for either input)	Output (for inputs in coincidence)	Input 1	Input 2
Volts	*Volts*	*Volts*	*Volts*
Cathode Resistor—4700Ω			
0.2	0.35	0.38	0.45
1.0	1.5	1.6	1.8
3.0	3.6	4.1	4.0
10.0	11.0	14.0	13.0
Cathode Resistor—470Ω			
0.2	0.37	0.48	0.49
1.0	1.5	2.0	1.9
3.0	3.9	4.9	4.9
10.0	12.0	16.0	14.0
Cathode Resistor—150Ω			
0.2	0.38	0.59	0.62
1.0	1.0	2.5	2.4
3.0	4.3	8.0	6.0

NOTE: The voltage levels of inputs 1 and 2 were chosen to produce identical output levels. Any discrepancy between the input levels can be attributed either to tube unbalance or the effect produced by unequal duty cycle. Input 1 was a 180μsec pulse, input 2 a 10μsec pulse.

2. DESIGN CONSIDERATIONS

Table 23-1 is a tabulation of operating data comparing the performance of PC 23 with that obtainable with different values of cathode resistance. The input levels in each case were adjusted in steps, keeping the output range unchanged. Input 1 was a 180μsec positive pulse; input 2, a 10μsec positive pulse. Both pulses were at 400pps. The choice of two widely different pulse lengths shows the effect of duty cycle. Negative signals can be combined by common-cathode mixers only at very low levels since cutoff is quickly reached.

Figure 23-1 displays the gain characteristic and linearity of the circuit for the three values of

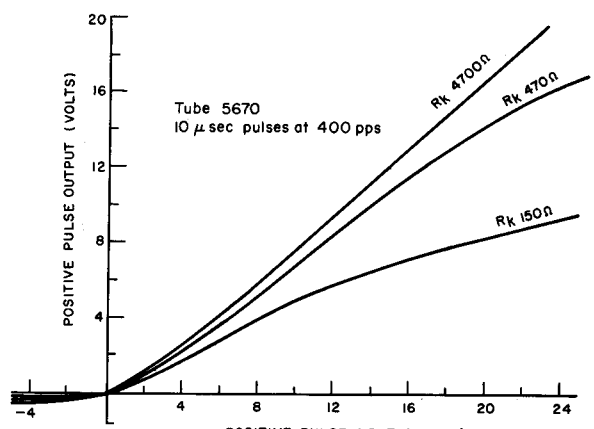


Fig. 23-1 COMMON-CATHODE MIXER

cathode resistance. This figure shows that the selected value of 4700Ω for the cathode resistance offers the widest range of linearity. This 4700Ω value is the effective value of cathode load resistance, provided the cable connection across the resistor is short and not terminated. If the mixer is required to drive a long low-impedance cable, it is necessary to terminate the cable in a low value of resistance approaching the cable impedance. This resistance lowers the effective value of the cathode load resistance and limits the output of the mixer.

The operating characteristics with 100Ω shunting the original 4700Ω would be somewhat similar to the data for 150Ω shown in table 23–1 and figure 23–1. The additive factor increases for lower values of cathode resistance, since the gain of the stage drops and there is less cross-biasing of the combined signals at the cathode. It is highly desirable to insert an additional cathode follower stage if the line impedance is low and a low value of additive function is required.

Table 23–2 is a tabulation of data for four 5670 sections in parallel for application where more than two inputs are to be combined. Comparing this data with the information in table 23–1, it appears that the circuit operation remains essentially the same. Paralleling additional cathode sections in order to provide for more inputs should cause an increase in output capacitance. The rise-time figure for short duration pulses does not suffer in proportion. An over-all increase of transconductance by the additional sections seems to offset the rise in capacitance by lowering the input impedance.

TABLE *23–2—Video Mixer: Common Cathode Type*

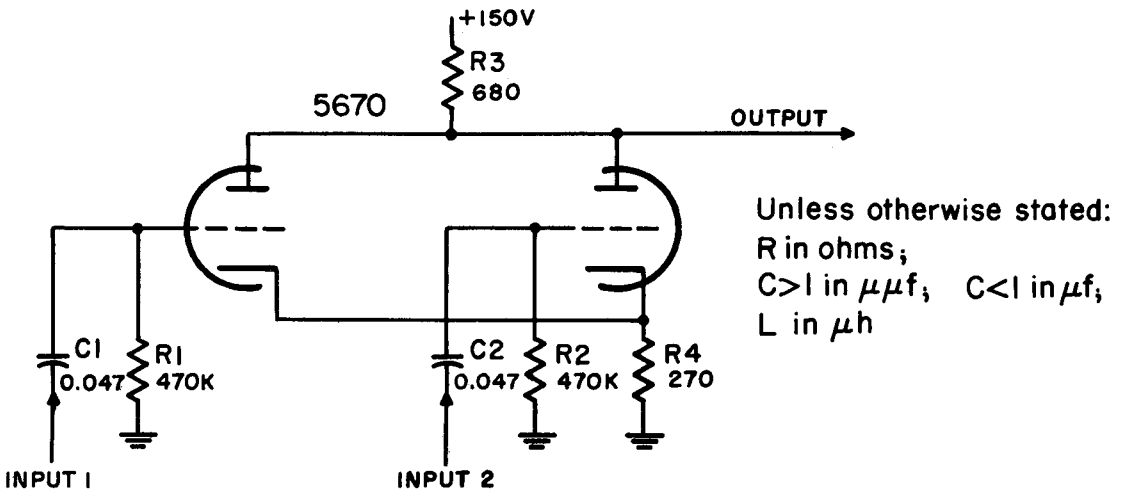
2C51—Four Sections With Common Cathode
E_{bb} = +150v

Output (for either input)	Output (for inputs in coincidence)	Input 1	Input 2
Volts	*Volts*	*Volts*	*Volts*
Cathode Resistor—4700Ω			
0.2	0.36	0.66	0.58
1.0	1.4	2.0	1.8
3.0	3.6	4.8	4.2
10.0	11.0	12.0	12.0
Cathode Resistor—470Ω			
0.2	0.37	0.80	0.79
1.0	1.5	2.2	2.2
3.0	4.0	5.6	5.5
10.0	12.0	47.0	15.0
Cathode Resistor—150Ω			
0.2	0.37	1.0	0.98
1.0	1.7	3.7	3.5
3.0	4.3	47.0	7.8

NOTE: Refer to note on table 23–1.

NBS PREFERRED CIRCUIT NO. 24
VIDEO MIXER: COMMON-PLATE TYPE

NBS PREFERRED CIRCUIT NO. 24
VIDEO MIXER: COMMON-PLATE TYPE



A video mixer is used to combine various forms of information such as radar video and range markers.

Video data	*Input* 1	*Input* 2	*Output (for either input)*	*Output (for inputs in coincidence)*
Polarity	Positive	Positive	Negative	Negative.
Level	3.5v	3.5v	4.0v	6.2v.

Gain: approximately 1.

Additive factor:[1] 55% at level given above.

Droop: 2% for 500μsec pulse for given input RC constants.

Rise time: approximately 0.03μsec (with 15μμf at load).

Two additional 2C51 sections may be paralleled with little change in operating characteristic, thus providing four inputs. This requires changing the cathode resistor R4 to 100Ω.

R3,R4: ±10%; R1,R2: ±20% limits. All C: ±10% limits.

NOTE:

1. See PC 23 for additive factor equation.

PC 24 VIDEO MIXER: COMMON-PLATE TYPE

1. APPLICATION

The primary function of a video mixer is to combine various video signals and pulses.

2. DESIGN CONSIDERATIONS

There are two significant differences between the operation of PC 23 and PC 24. The common-cathode circuit, PC 23, has a positive output for positive input; the common-plate mixer, PC 24, inverts the phase and delivers a negative output. The other consideration is the additive factor. Signals that appear in time coincidence at the input tend to combine in an additive manner in the case of the common-plate mixer. Consequently this type cannot prevent overloading of subsequent video amplifiers by coincident signals. Overloading can only be avoided by means of limiting action in a following stage. The limiting level can be set for the highest level of one input. Any further addition of signal will then result in clipping.

PC 24 has a gain of 1. A higher gain can be achieved with a common-plate mixer, with certain limitations. The primary function of a mixer is to combine signals in a proper manner and to preserve the rise-time fidelity of short-duration pulses. The gain was of secondary importance in the selection of the preferred circuit. This circuit requires no high-frequency compensation in the form of a plate inductance or cathode bypass capacitor. A rise-time of 0.01μsec has been achieved by the use of a low value plate load, permitting duplication of the circuit without the computation of tailored inductors or capacitors. Furthermore, the highly degenerative cathode resistor offers good gain-stability with tube aging. The Miller effect input capacitance is kept to a minimum as a result of the low gain.

As noted on the circuit sheet, four inputs can be mixed by paralleling two additional tube sections. If the value of plate load and cathode resistance is not changed, paralleling halves the gain. By substitution of a cathode resistance value of 100Ω, the gain can be brought back to unity. No deterioration of rise time was noted due to additional parallel tube sections.

The 5670 tube was chosen over another possible type, the 5814A, for several reasons. Statistics point out the reliability of the 5670, both in an electrical and mechanical sense. Second, it has been determined experimentally that under comparable conditions of operation, as in common-plate mixers, the 5814A draws almost twice as much plate current as the 5670. It was felt that the lower heat dissipation of the latter would contribute significantly to longer tube life in this circuit.

Figure 24-1 is a plot of output versus input voltage for the common-plate mixer, PC 24. Note the small output that can be attained from negative input pulses.

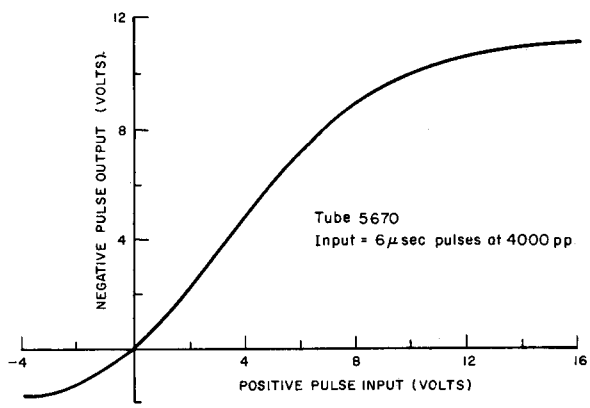
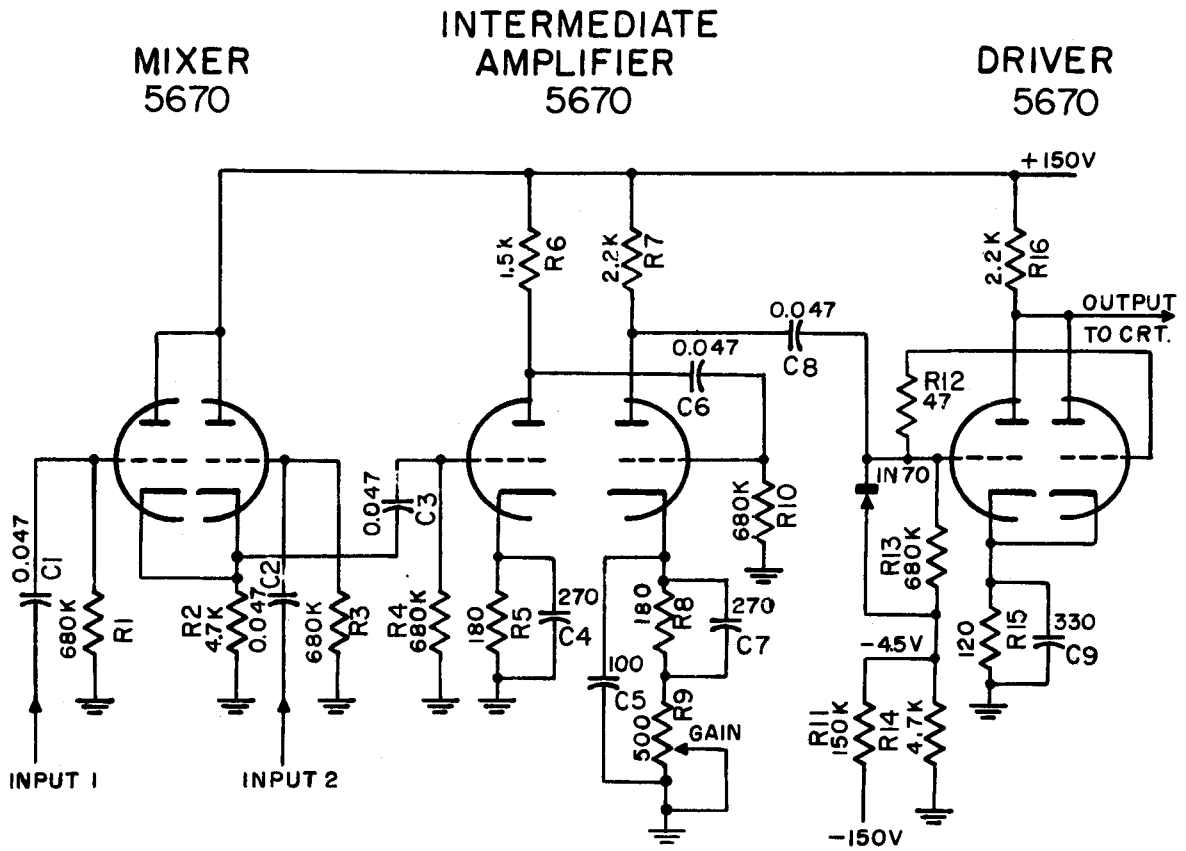


Fig. 24-1 COMMON-PLATE MIXER

NBS PREFERRED CIRCUIT NO. 25
VIDEO AMPLIFIER CHAIN

NBS PREFERRED CIRCUIT NO. 25
VIDEO AMPLIFIER CHAIN



Unless otherwise stated: R in ohms; C > 1 in $\mu\mu$f; C < 1 in μf; L in μh

Gain: 60v output for 1 volt input.
Maximum input amplitude: 1 volt.
Polarity: Input — Positive.
Output — Negative.
Rise Time: 0.10μsec maximum (over-all) with approximately 15$\mu\mu$f output capacity.
Droop: 10% for 800μsec pulse (over-all).
Gain of Mixer: 0.65.
Gain of Intermediate amplifier: 15.
Gain of Driver: 5.9.
Gain control range: 4.1.
Total supply current: 26ma.
Grid and cathode resistors 20%: all others 10% limits.
All C: 20% limits.

PC 25 VIDEO AMPLIFIER CHAIN

1. APPLICATION

This preferred video chain circuit has been developed for use in a radar display system. The function of the video chain is to mix the radar video with marker pulses and amplify the combined signals to a level sufficient to intensity-modulate the cathode ray indicator. This circuit is not intended for a specific application. Rather, it will serve as a convenient guide in planning the video section of a display system. The circuit includes principles that allow for ease of manufacture and give high reliability in operation. The component types and values have been selected to make the circuit suitable for either mechanized production or conventional construction.

2. DESIGN CONSIDERATIONS

A large number of existing radar video circuits were examined. This examination showed that great liberties were afforded the designer in the choice of tube types, component values, and circuitry. Often as many as 10 different circuit designs perform the same function. The video chain circuits examined extend from the video mixer to the cathode ray tube driver amplifier. The circuits were divided into individual stages for the purpose of tabulating the data of stages performing the same function. This procedure led to a restriction of operating voltages, tube types, and circuit parameters. These restrictions in turn formed the basis of the preferred video chain.

Considerations concerning design and circuit performance are discussed below. For a more detailed discussion, refer to Preferred Circuits 23, 26, and 27.

2.1 *Supply Voltage*: An examination of equipment in current use showed the multiplicity of positive and negative voltages. An analysis of existing circuits indicated that these voltages could be limited to 300 and 150v, positive and negative. In this preferred circuit, the choice of the positive 150v supply was made as being generally sufficient for signal swings under 100v.

2.2 *Video Mixer:* The common cathode mixer is the same as that chosen for PC 23. The advantages of this circuit are:

(*a*) Good gain stability due to cathode degeneration.

(*b*) Favorable additive factor for time-coincident input signals.

(*c*) Ideal polarity considerations.

(*d*) Low output impedance (500Ω).

(*e*) Possibility of paralleling sections.

(*f*) Excellent rise-time (< 0.05μsec).

The less-than-unity gain of the stage is a negligible disadvantage. For a 1 volt input, the output is approximately 0.65v.

2.3 *Video Amplifier:* This stage represents a departure from conventional video circuitry. The two major features are the use of triodes and the lack of inductive plate peaking. These features will be taken up individually.

(*a*) Triodes versus pentodes: A dual triode envelope is used as a two stage amplifier in the selected video amplifier. The transconductance of triodes has been improved sufficiently in the last few years so that they compare favorably with pentodes. Triodes also have lower output capacity.

The greatest obstacle to overcome in the use of triodes is the adverse increase of input capacity caused by the Miller effect. The low-impedance output of the common cathode mixer reduces the effect of the increase of input capacity of the first video amplifier. This effect is balanced in the second amplifier section by cathode peaking, discussed below.

(*b*) Capacitive cathode peaking versus inductive plate peaking: The technique of cathode peaking is neither widely suggested nor employed. The situation making its application possible in this video chain is the method of biasing the two video amplifier stages. Cathode biasing was chosen because it is simpler than fixed grid-bias. Grid-bias is usually taken from a resistive divider across a source of high negative voltage. This method requires more components than the single cathode resistor. The disadvantage of loss of gain associated with self-bias is balanced by the improvement in stability resulting from cathode degeneration.

The next problem is the effect of high-frequency compensation on rise time. Table 25–1 contains two sets of figures showing the relative improvement of gain/rise-time ratio using cathode peaking. Although cathode compensation increases gain/rise-time ratio compared to the unbypassed

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TABLE 25–1—*Performance of Shunt-Peaked Circuit at Plate*[1]

m	Gain/rise-time ratio	Overshoot (percent)
0	1.0	0
0.25	1.4	0
0.41	1.7	3.1
0.50	1.9	6.7
0.60	2.1	11.4

$m = \frac{L}{R^2C}$. L = compensating inductance. R = load resistance. C = output capacity.

Performance of Cathode Compensation

P	Gain/rise-time ratio	Overshoot (percent)
0	1.0	0
0.5	1.2	0
1	2.0	0
1.5	2.2	2
2	2.9	14

$P = R_kC_k/R_lC$. R_k = cathode resistor. C_k = compensation capacitor. R_l = load resistance. C = output capacity.

[1] George E. Valley, Jr. and Henry Wallman, ed., *Vacuum Tube Amplifiers, Rad. Lab. Series*, vol. 18, McGraw-Hill, 1948, pp. 74, 91.

cathode resistor, it does not improve the ratio compared to a grounded or completely bypassed cathode.

The introduction of a small low-tolerance capacitor at the cathode is simpler than adding an inductor at a higher impedance plate load. Precise duplication of the circuit becomes much simpler. The complete absence of inductors makes the system attractive for mechanized production.

2.4 *Video Driver:* The paralleled triode driver stage completes the video chain. Triodes were selected because of their low output capacity and high transconductance. With no input signal, the driver operates at 0.5ma plate current.

The clamp diode at the grid may be eliminated for short pulse-duration, low duty-cycle operation. The diode is needed in the case of a high duty-cycle signal, however, to clamp the bottom level of the signal at −4.5v.

2.5 *Summary:* Below is a summary of the operating characteristics of the complete video chain:

(*a*) A positive 1 volt pulse at either input produces a 60v negative pulse at the output.

(*b*) The over-all rise-time is 0.1μsec.

(*c*) Droop is approximately 10% for an 800μsec pulse.

Figure 25–1 is a plot of the over-all gain characteristic of the video chain.

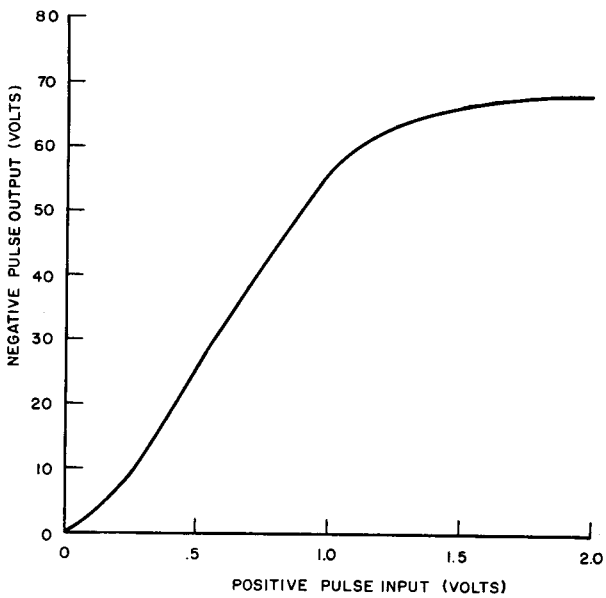
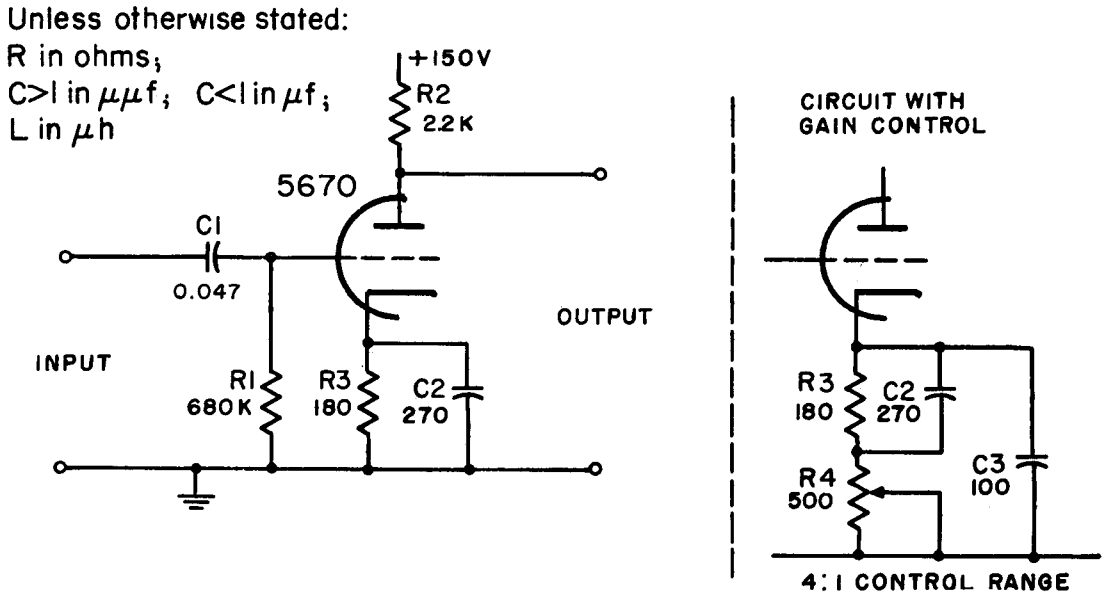


Fig. 25–1 GAIN CURVE OF CHAIN

NBS PREFERRED CIRCUIT NO. 26
INTERMEDIATE VIDEO AMPLIFIER

NBS PREFERRED CIRCUIT NO. 26
INTERMEDIATE VIDEO AMPLIFIER



This circuit is used to amplify intermediate level video signals and to invert signal polarity. It is used as a part of video chain, PC 25.

Input waveform: Video pulses of either polarity.

Operation:

R2	2.2KΩ	1.5KΩ.
Gain	5.5	3.5.
Rise time [1]	0.046μsec	0.032μsec.
Input, maximum volts	−2.3, +2.2	−3.5, +3.0.
Output, maximum volts	±16	±12.
Input capacity	11μμf	8μμf.

Tolerance: The variation in gain is ±10% for MIL specification limits of tubes and ±5% resistors.

Droop: 1.5% for 500μsec pulse. [2]

R2,R3: ±10%; R1: ±20% limits. C: ±20% limits.

NOTES:

1. Total output capacity, 19μμf.
2. For C1 = 0.01μf; R1 = 680KΩ, droop 1.5% for 100μsec pulse.

PC 26 INTERMEDIATE VIDEO AMPLIFIER

1. APPLICATION

This circuit is used to amplify and invert intermediate-level video signals such as the output of a mixer or cathode follower. The circuits may be connected in cascade to obtain greater gain or to regain the original polarity.

2. DESIGN CONSIDERATIONS

The intermediate video amplifier is designed to amplify a 1-volt signal to the level required by a video driver amplifier. Two values of plate load resistors are given, permitting a limited selection of rise time and gain. The gain of the amplifier is 5.5 for a 2.2KΩ plate resistor and 3.7 for a 1.5KΩ resistor. The gain curve in figure 26-1 shows the

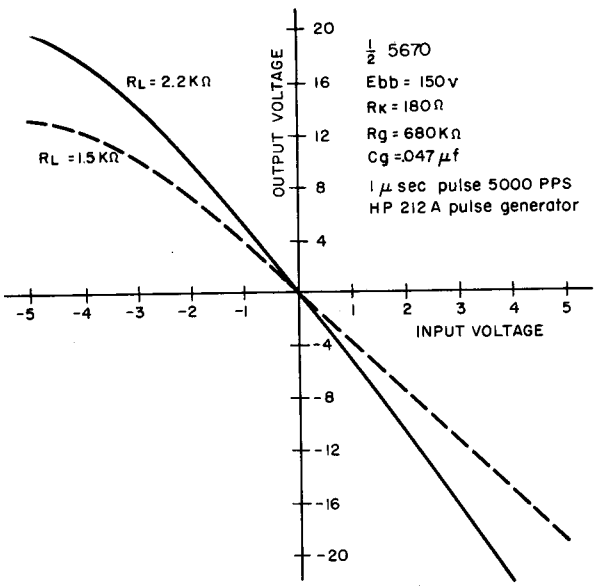


FIG. 26-1 OUTPUT CHARACTERISTIC: INTERMEDIATE VIDEO AMPLIFIER

limiting of the output voltage with negative inputs. The MIL limits of 5670 transconductance are from 4500 to 6500μmhos. The variation of gain with different tubes is shown in figure 26-2. Extrapolating the data to these limits, the variation of gain is about ±10%. When the plate and cathode resistors are changed ±5%, the electrode potentials do not vary more than ±1.5%. The change in gain with ±10% change in supply voltage is less than 1%. With a ±33% voltage change, the gain changes ±7%.

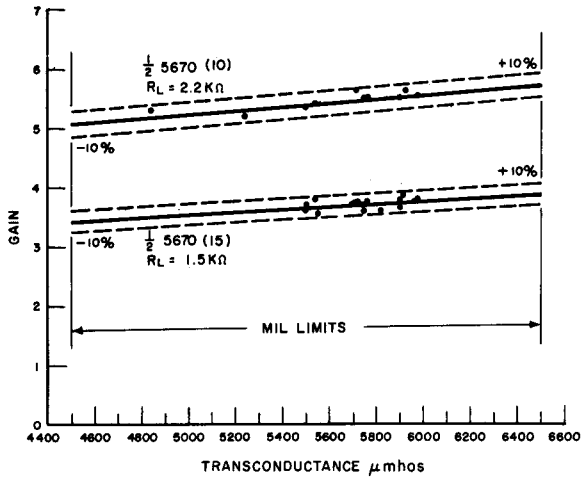


Fig. 26-2 VARIATION OF GAIN WITH TRANSCONDUCTANCE

The rise time for the circuit using a 2.2KΩ plate resistor is 0.046μsec.

The total output capacity is

	μμf
Plate capacity	1
Wiring	7
Following input	11
	19

Using the relation

$$\text{Rise time, } t_r = 2.2RC$$

then

$$t_r = 2.2 \times 2200 \times 19 \times 10^{-12}$$
$$t_r = 0.092\mu\text{sec}$$

With cathode high-frequency compensation, an improvement factor of about 2 is attained (see PC 25, Sec. 2.3). The resulting rise time is 0.046μsec. The rise time is 0.032μsec when a 1.5KΩ is used.

Because of the Miller effect, the input capacity of the triode amplifier is appreciable. The input capacity for this amplifier is computed using the formula

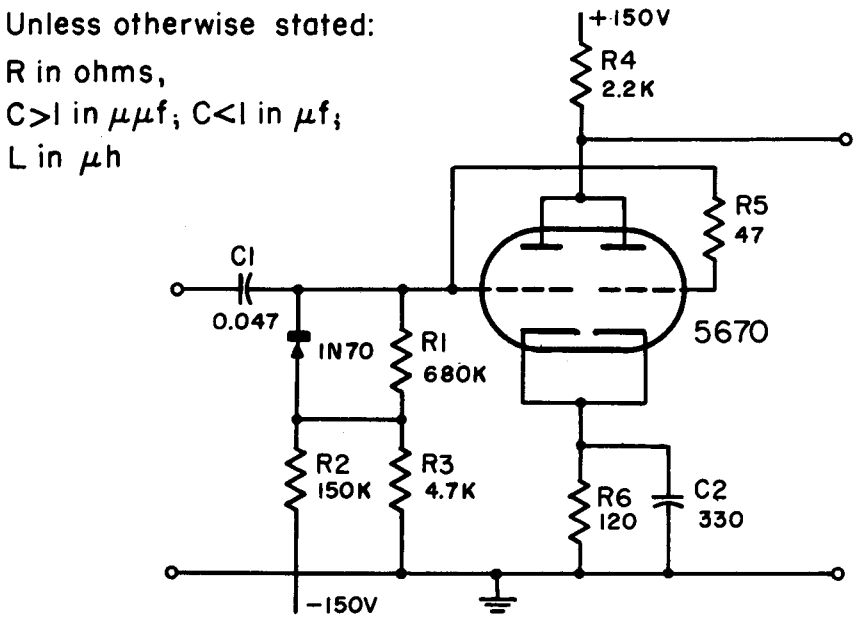
$$C \text{ input} = C_{gk} + (1 + \text{Gain}) C_{gp}$$
$$= 2.2 + (1 + 5.5)\ 1.3\mu\mu\text{f}$$
$$= 11\mu\mu\text{f}$$

The input capacity for the amplifier with a gain of 3.7 is 8μμf.

The droop is a function of the input coupling circuit (see PC 21, Sec. 2). The droop is 1.5% for a 500μsec pulse.

NBS PREFERRED CIRCUIT NO. 27
TRIODE VIDEO DRIVER AMPLIFIER

NBS PREFERRED CIRCUIT NO. 27
TRIODE VIDEO DRIVER AMPLIFIER



This video amplifier is used to drive the cathode of a CRT indicator. It is used as a part of video chain PC 25.

Input waveform	Positive pulses.
Input voltage	2.0 to 9.5v.
Voltage gain	4.8 at 5v input.
Input capacity	19.4μμf.
Rise time [1]	0.05μsec.
Maximum output voltage	60v.

Tolerance: The variation in gain is ±10% for MIL specification limits of tubes.

Droop: [2] 4% for 500μsec pulse.

R2,R3,R4: ±10%; R1,R5,R6: ±20% limits. C: ±20% limits.

NOTES:

1. Total output capacity, 20μμf.
2. For C1 = 0.01μf; R1 = 680KΩ, droop is 4% for 100μsec pulse.

PC 27 VIDEO DRIVER: TRIODE

1. APPLICATION

The purpose of the driver stage is to amplify radar or other video signals to the level necessary for intensity-modulation of the cathode ray tube indicator. This driver is used as part of the video chain, PC 25.

2. DESIGN CONSIDERATIONS

Intensification of a cathode ray indicator can be accomplished by either a positive signal at the grid or a negative signal at the cathode. The latter arrangement has been chosen in the design of this preferred circuit. A negative output from a video driver can be achieved with a considerably lower steady-state plate current and a lower plate load resistor. The circuit with positive output, in comparison, must draw enough steady-state plate current in order that the plate swing may start at a point below the plate supply level. In the interest of plate dissipation, the plate load resistor must be kept high in value if the plate swing requirements are to be met. This consideration increases the problem of high-frequency compensation.

As in the case of PC 26, the preferred driver stage has a plate load without inductive compensation. Cathode bias resistance is used for gain stabilization and is bypassed with a small capacitor for high-frequency compensation. The use of triodes eliminates the droop problem associated with screen supplies. Figure 27-1 shows the gain characteristic of the stage. The average gain is 4.8.

The effectiveness of the gain stabilization resulting from cathode degeneration is illustrated in the relatively low variation of gain with transconductance (fig. 27-2). The MIL limits of transconductance are 4500 and 6500μmhos. Paralleling the triode sections increases the limits to a theoretical 9000 and 13,000μmhos. The data are extrapolated to MIL limits to obtain the gain tolerance of $\pm 10\%$.

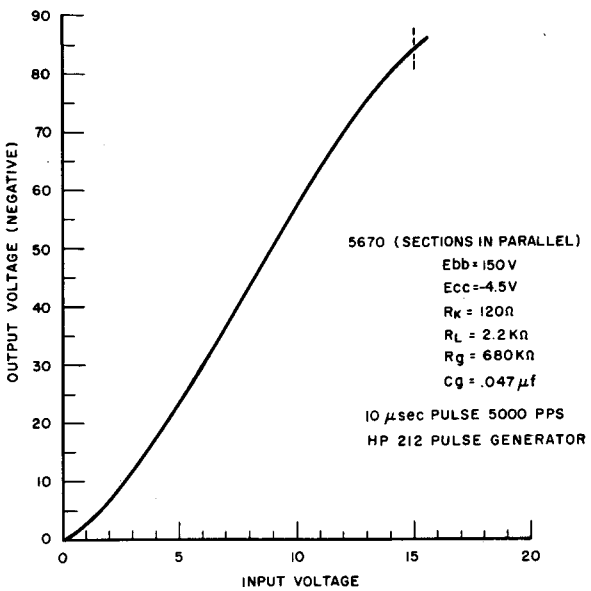


Fig. 27-1 OUTPUT CHARACTERISTIC: 5670 VIDEO DRIVER

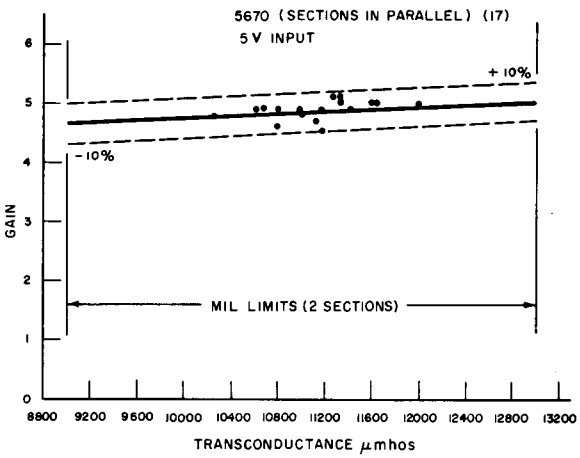


Fig. 27-2 VARIATION OF GAIN WITH TRANSCONDUCTANCE

The rise time for the driver using a 2.2KΩ plate resistor is 0.050μsec.

The total output capacity is

	$\mu\mu$f
Plate capacity	2
Wiring	13
Cathode CRT	5
	20

Using the relation

$$\text{Rise time, } t_r = 2.2\ RC$$

then

$$t_r = 2.2 \times 2200 \times 20 \times 10^{-12}$$
$$t_r = 0.097\mu\text{sec}$$

An improvement factor of about 2 is attained with

cathode high-frequency compensation (see PC 25, Sec. 2.3). The resulting rise time is about 0.05μsec.

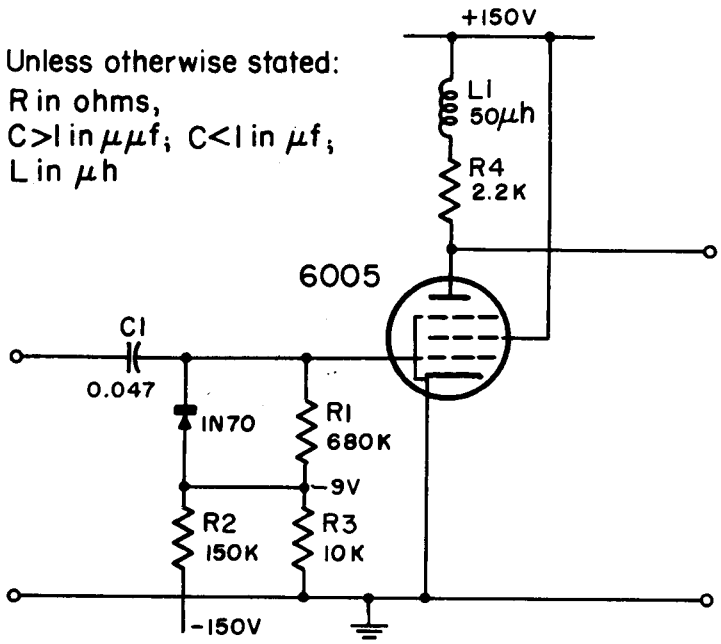
Because of the Miller effect, the input capacity of the triode amplifier is appreciable. The input capacity for this amplifier with sections in parallel is computed using the formula

$$\begin{aligned} C \text{ input} &= C_{gk} + (1 + \text{Gain})\, C_{gp} \\ &= 2 \times 2.2 + (1 + 4.8)\, 2 \times 1.3 \mu\mu\text{f} \\ &= 19.4 \mu\mu\text{f} \end{aligned}$$

The droop is a function of the input coupling circuit (see PC 21, Sec. 2). Without the 1N70 diode restorer the droop is 1.5% for a 500μsec pulse.

NBS PREFERRED CIRCUIT NO. 28
BEAM POWER VIDEO DRIVER AMPLIFIER

NBS PREFERRED CIRCUIT NO. 28
BEAM POWER VIDEO DRIVER AMPLIFIER



This video amplifier is used to drive the cathode of a CRT indicator.

Input waveform	Positive pulses.
Input voltage	1 to 9v.
Voltage gain	7.
Input capacity	12.6μμf.
Rise time	0.07μsec. [1]
Maximum output voltage	70v.

Tolerance: The variation in gain is ±17% for MIL specification limits of tubes.

Droop: 4% for 500μsec pulse. [2]

R2,R3,R4: ±10%; R1: ±20% limits. C: ±20% limits.

NOTES:

1. Total output capacity 25.5μμf.
2. For C1 = 0.01μf; R1 = 680KΩ, droop is 4% for 100μsec pulse.

PC 28 BEAM POWER VIDEO DRIVER AMPLIFIER

1. APPLICATION

The purpose of the driver stage is to amplify radar or other video signals to the level necessary for intensity-modulation of the cathode ray tube indicator.

2. DESIGN CONSIDERATIONS

The beam power video driver is widely used in search radars. A discussion of the general requirements for a video driver is given in PC 27, Section 2. PC 28 is designed for those applications where the input capacity of PC 27 is too high. Some of this advantage is lost in the output side where its capacity is 7.5$\mu\mu$f compared to 2.6$\mu\mu$f for triodes in parallel. The linearity of this circuit is more uniform throughout the operating range than in the triode circuit, PC 27.

In the beam power circuit, high-frequency shunt

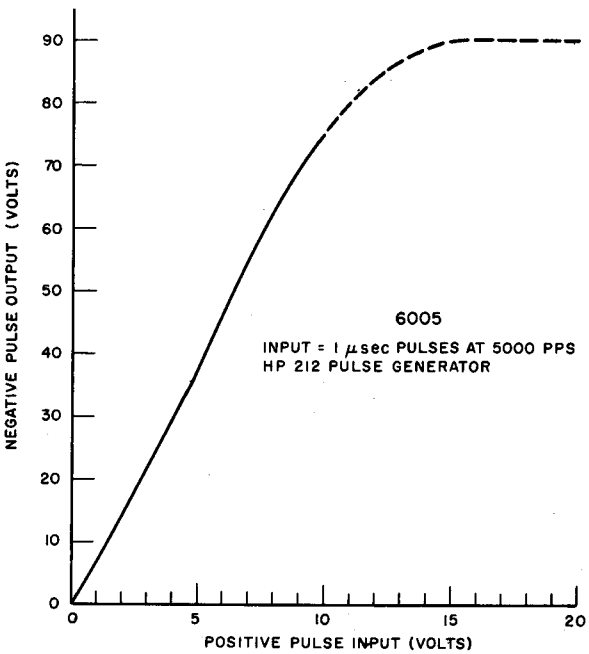


Fig. 28-1 OUTPUT CHARACTERISTIC: 6005 VIDEO DRIVER

ompensation is used in the plate circuit. Figure 8–1 shows the gain characteristic of the video driver. The average gain is 7.

The rise-time for the driver using a 2.2KΩ plate resistor and shunt compensation is 0.07μsec. The total output capacity is

	$\mu\mu$f
Plate capacity	7.5
Wiring	13.0
Cathode CRT	5.0
	25.5

Using the relation

Rise time, $t_r = 2.2RC$

then

$$t_r = 2.2 \times 2200 \times 25.5 \times 10^{-12}$$
$$t_r = 0.12\mu\text{sec}$$

With shunt compensation [1] using a parameter ratio $m = .41$, an improvement factor of 1.7 is attainable with 3% overshoot. The resulting rise time is 0.07μsec.

The value of shunt inductance is computed using the relation

$$L = mR^2C$$
$$L = 0.41 \times 2200^2 \times 25.5 \times 10^{-12}$$
$$L = 50\mu\text{h}$$

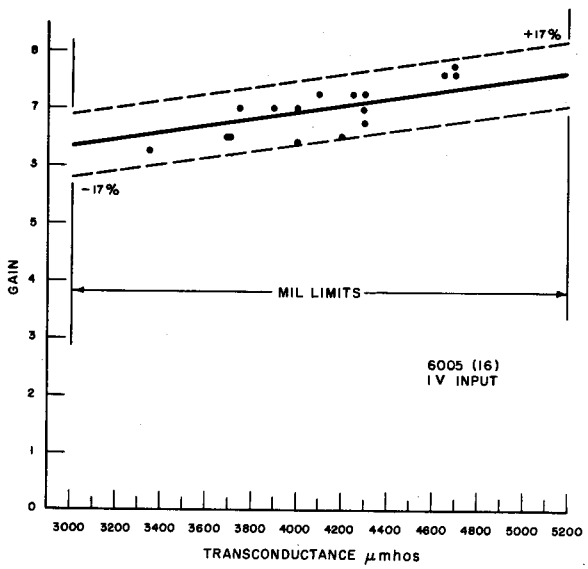


Fig. 28-2 VARIATION OF GAIN WITH TRANSCONDUCTANCE

[1] George E. Valley, Jr. and Henry Wallman, ed., *Vacuum Tube Amplifiers, Rad. Lab. Series*, vol. 18, McGraw-Hill, 1948, p. 73.

Because of the Miller effect, the input capacity is increased about 4$\mu\mu$f. The total input capacity is computed using the relation

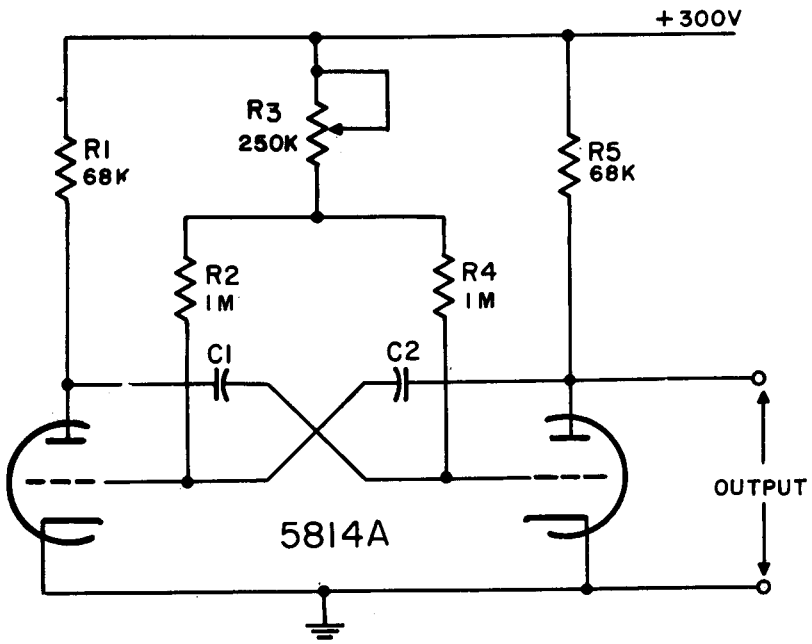
$$C \text{ input} = C_{gk} + (1 + \text{Gain})\, C_{gp}$$
$$= 8.3 + (1+7)(0.54)$$
$$= 12.6\mu\mu\text{f}$$

Droop is a function of the input coupling circuit (see PC 21, Sec. 2). Without the 1N70 diode restorer the droop is 1.5% for a 500μsec pulse.

The absence of gain-stabilizing resistors in the cathode and screen circuits is reflected in the variation of gain with transconductance. The 6005/6AQ5W MIL range is from 3000 to 5200μmhos. Figure 28–2 shows the gain variation for 16 tubes. Extrapolating the data to the MIL limits gives a gain tolerance figure of $\pm$17%.

NBS PREFERRED CIRCUIT NO. 40
PRF MULTIVIBRATOR

NBS PREFERRED CIRCUIT NO. 40
PRF MULTIVIBRATOR



Unless otherwise stated: R in ohms; C>1 in $\mu\mu$f; C<1 in μf; L in μh

Formula: $C1 = C2 = \frac{0.79}{f}$ $(10^6 \mu\mu f)$

where f= pulse-repetition frequency in pulses per second. Potentiometer will compensate for values of C which differ from computed values by not more than 5%.

Output: 260v (not including negative overshoot).

Fall time: 10–90% value (not including negative overshoot): 0.4μsec.

Frequency stability: 0.5% change in frequency for 10% change in B+. Frequency drift primarily proportional to drift in values of C1,C2,R2, and R4.

R2,R4: ±1%; R1,R5: ±5%; R3: ±20% limits. C1,C2: ±2%. limits.

NOTES:

1. Use negative-going waveform for accurate timing.
2. To minimize effect of varying load impedance on frequency stability, use differentiated output into cathode follower.

PC 40 PRF MULTIVIBRATOR: ASTABLE, PLATE-TO-GRID COUPLED

1. APPLICATION

This circuit is used as a moderately stable repetition-rate generator. It is an astable, plate-to-grid coupled multivibrator. The multivibrator has the advantage of greater frequency stability than the blocking oscillator and greater economy of components than the Wien bridge oscillator. One disadvantage of the multivibrator is that the output impedance for positive pulses is essentially equal to the plate-load resistance. This resistance must be relatively high for good frequency stability.

2. DESIGN CONSIDERATIONS

The recommended design uses a 5814A twin triode or electrical equivalents with relatively high plate resistors (68KΩ). This value of resistance will slow the transition to some extent, but frequency stability is more important. A differentiated output into a cathode follower is recommended, since a load on the multivibrator will impair the frequency stability. The negative-going waveform is generated at a much lower impedance than the positive-going waveform; therefore, the cathode follower should be zero-biased (grid resistor returned to the cathode) so that only the fast negative-going pulse will be obtained from the cathode follower output.

The speed of the transition, as in all multivibrators, depends to some extent upon the capacitance between tube elements. Except for the basic consideration of keeping leads as short as possible to minimize stray capacities, no special precautions need be observed in the construction of this circuit. Potentiometer, R3, should be readjusted each time the multivibrator tube is changed, since changing the multivibrator tube may cause a 3% change in repetition frequency.

The period of a symmetrical, astable multivibrator with grid resistors returned to a positive voltage may be determined approximately from the equation [1]

$$T = 2RC \ln \frac{E_g + E_i}{E_g + E_c}$$

where T = period in seconds.
R = value of either grid resistor in ohms.
C = value of either cross-coupling capacitor in farads.
E_g = voltage to which grid resistors are returned.
E_i = voltage drop across either plate resistor when tube is conducting (at zero grid bias).
E_c = absolute value of grid cutoff voltage with B+ on plate.

This equation is not exact because it does not take into consideration the effect of tube capacities and the overshoots that appear immediately after the transition. It also ignores as negligible compared to R the parallel combination of the plate resistance and load resistor of the "on" tube, which are in series with the grid resistance during the discharge of C. Although a more elaborate expression may be written to include the effects of tube capacities and tube and plate load resistances, there is no simple formula which will account for the overshoots. Therefore, the empirical formula given in figure 40-2 was derived for the value of cross-coupling capacitance as a function of the repetition frequency with all parameters fixed.

The frequency stability of a multivibrator may be improved by making the timing waveform on the grid of the cutoff tube very large and as steep as possible at the time that this voltage is approaching the cutoff voltage. In this circuit a large timing waveform is obtained by using a high resistance in the plate circuit, since the full voltage drop across this resistor is applied to the opposite grid as the timing waveform. This waveform is made steeper as it passes through the cutoff region of the tube by returning the grid resistor to a positive voltage instead of ground. The exponentially-rising voltage on the grid will then be further from its final value as it passes through cutoff. The optimum value of positive voltage, E_g, to which the grid resistor should be returned is such that the relationship $E_g + E_c = (E_g + E_i)/\epsilon$ is satisfied. [2] The notation in this equation is the same as previously given, with ϵ the natural

[1] Britton Chance, ed., *Electronic Time Measurements*, *Rad. Lab. Series*, vol. 20, McGraw-Hill, 1949, p. 80.
[2] Britton Chance, ed., *Waveforms*, *Rad. Lab. Series*, vol., 19, McGraw-Hill, 1949, pp. 177–179, 190–194.

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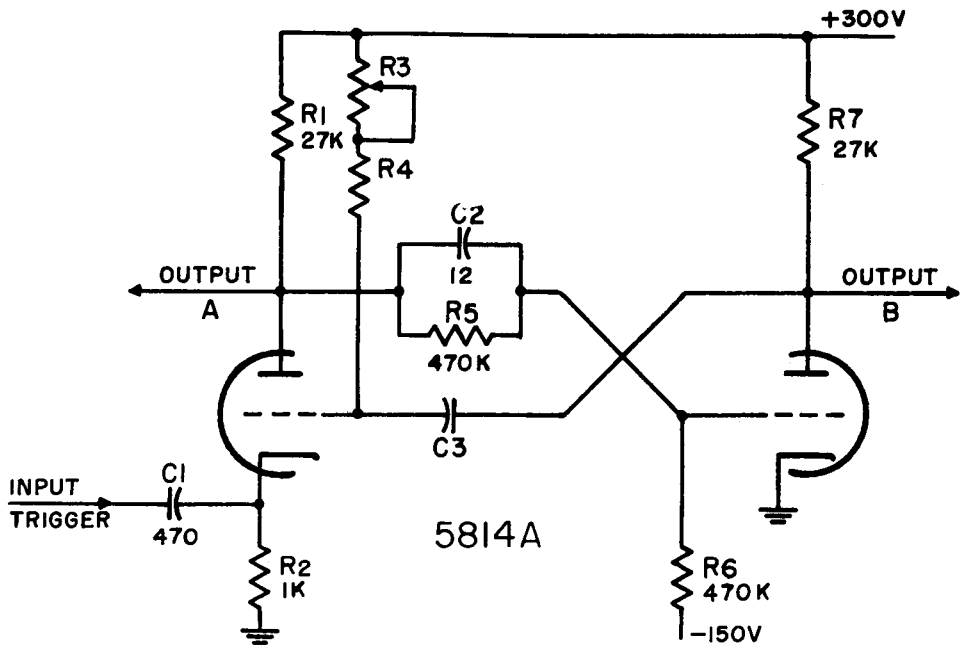
logarithm base. The value of this voltage is not critical. The grid resistors are returned to B+ in most applications.

Pentodes have an advantage over triodes for multivibrators since the voltage drop across the "on" tube can be held to closer limits by operating the pentodes in the knee region. This results in better frequency stability than with triodes using the same value of plate load resistors. The relative improvement becomes smaller, however, as the value of the resistors is increased. In addition, if pentodes are operated in the knee region of the curves, the multivibrator may sometimes fail to oscillate. [3]

[3] William A. Edson, *Vacuum Tube Oscillators*, John Wiley & Sons, Inc., 1953, pp. 281–293.

NBS PREFERRED CIRCUIT NO. 41
MAIN GATE MULTIVIBRATOR: MONOSTABLE

NBS PREFERRED CIRCUIT NO. 41
MAIN GATE MULTIVIBRATOR: MONOSTABLE



Unless otherwise stated: R in ohms; C>1 in $\mu\mu$f; C<1 in μf; L in μh

This circuit is used to provide a positive or negative gate pulse in response to a positive input trigger.

Self timing — requires no shut-off pulse.

Gate duration: Maximum 2500μsec. Minimum 30μsec.
Maximum duty cycle 0.85.

PRF: 200 to 2000pps.

Input: 25v peak.

Outputs: [1] A. Positive 210v peak. Rise time: 2μsec. Decay time: 1μsec.
B. Negative 210v peak. Rise time: 0.7μsec. Decay time: 10μsec.

Component values: (R3+R4) must be between 550KΩ and 3MΩ. For (R3+R4) = 2MΩ, gate duration in μsec = value of C3 in $\mu\mu$f. R3 = 1/5(R3+R4) for ease of adjustment.

R3,R4, and C3 must be of stability commensurate with application.

All C: $\pm$10% limits. All R: $\pm$10% limits.

Stability: For a 5% change in plate supply voltage, the duration will change 0.8%. For a 10% change in heater voltage, the pulse duration will change 0.5%.

NOTE:

1. Rise and decay times obtained with probe of 15$\mu\mu$f.

PC 41 MAIN GATE MULTIVIBRATOR: MONOSTABLE

1. APPLICATION

The primary function of this preferred circuit in radar equipment is to establish the period during which the main display sweep is presented. Invariably the unblanking gate for the cathode ray tube is obtained from this circuit. It may also provide the gate for initiating and shutting off the distance-mark generator. This circuit can be used when a positive or negative rectangular gate of long duration is needed.

The multivibrator would normally be triggered from a source of positive short-duration pulses, such as PC 48, and having a repetition-rate between 200 to 2000pps. It can be used at repetition rates from zero to a maximum determined by the gate length and recharging time.

2. DESIGN CONSIDERATIONS

In certain applications it is desirable to have the range-sweep lengths determined by the duration of the main gate. A monostable multivibrator was chosen for this function. The circuit produces rectangular gates of both polarities upon receipt of a trigger pulse. The length of the gate is primarily determined by R3, R4, and C3. In an application where different ranges are required, these elements are switched in value for each duration position. It is desirable that the sum of R3 and R4 not exceed 3MΩ. For a range-gate of 2500μsec, (R3+R4) could be made 2MΩ and value of 25μμf for C3 would provide the gate length.

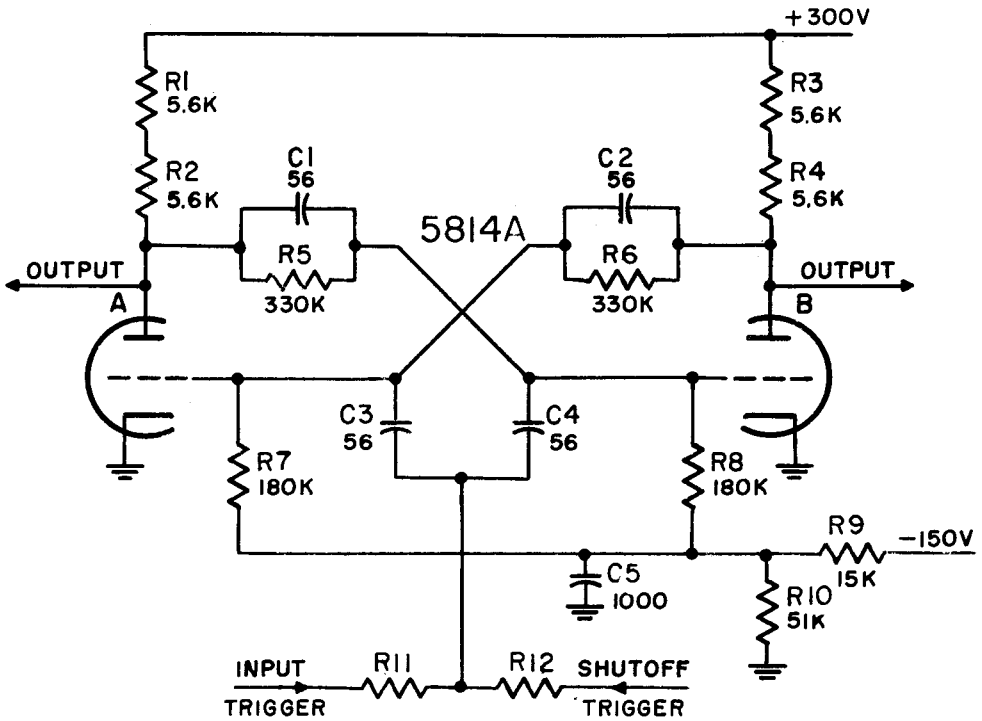
In some instances this circuit may supply output gates to as many as four branches. Unless precautions are taken, the steepness of the waveforms can be adversely affected by shunt capacities of the associated circuits or by grid-current demands. The rise and decay times given will hold only if the total shunt capacity at either plate does not exceed 15μμf. A much greater shunting capacity can be tolerated by taking the output at some point divided down on the plate-load resistors, but at the sacrifice of amplitude. The positive output at "A" should not be coupled to a circuit that demands grid current, since the multivibrator may fail. A cathode follower or buffer should be used to couple the positive output to such a circuit.

The rise time in the negative direction, output at "B", is inherently much faster than the positive. An improvement in the positive rise time at "A" can be realized by lowering the value of C2. The negative excursion, however, will be inversely affected. The decay time at output "B" is directly related to the value of C3. The stated figure of 10μsec is for a value of 100μμf for C3.

For applications where the gate length is determined by a shutoff pulse from the sweep circuit, the monostable circuit is not recommended for reasons stated in PC 42. PC 42, utilizing a bistable multivibrator, is recommended for these applications. Although many radar systems employ a monostable circuit with a shutoff pulse, examination will show that the basic nature of the monostable circuit does not lend itself to stable premature recycling by a shutoff pulse.

NBS PREFERRED CIRCUIT NO. 42
MAIN GATE MULTIVIBRATOR: BISTABLE

NBS PREFERRED CIRCUIT NO. 42
MAIN GATE MULTIVIBRATOR: BISTABLE



Unless otherwise stated: R in ohms; C > 1 in $\mu\mu$f; C < 1 in μf; L in μh

This circuit provides a positive or negative gate in response to an input trigger pulse, and the gate is terminated by a shut-off pulse.

Input: >25v peak, either polarity, 1μsec duration.

Shutoff pulse: >25v peak, either polarity, duration not critical.

Output A or B: 180v peak, rectangular gate of either polarity.

	Negative Gate	*Positive Gate*
Rise time [1]	0.7μsec	2.5μsec
Decay time	2.5μsec	0.7μsec

Gate duration: Determined by timing trigger and shutoff pulse time interval.

R9 and R10: $\pm$5%; all other R: $\pm$10% limits. All C: $\pm$10% limits.

NOTES:

1. Rise and decay times obtained with 15$\mu\mu$f probe.
2. R11 and R12 are part of the input circuit, 5KΩ to 50KΩ.

PC 42 MAIN GATE MULTIVIBRATOR: BISTABLE

1. APPLICATION

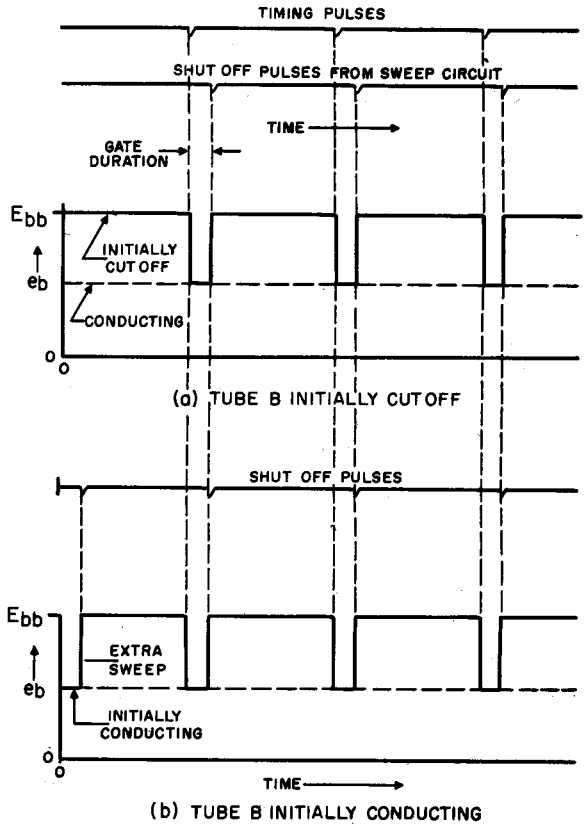
The main-gate multivibrator generates the gates during which the display is presented. The applications for this circuit are similar to PC 41, Main-Gate Multivibrator: Monostable. The major difference is the need for a shutoff pulse to return the circuit to the initial state.

2. DESIGN CONSIDERATIONS

In some radar applications it is desirable to have the gate length controlled by the display circuit. In such cases the sweep circuit provides a shutoff pulse for the purpose of recycling the bistable multivibrator. The monostable multivibrator can also be used with a shutoff pulse to terminate operation before the end of its normal cycle. However, the required shutoff pulse amplitude does not remain constant over the duration of the cycle because the varying range and/or repetition rates which occur in radar sets cause the shutoff pulse to occur at different points on the exponential rise of the grid voltage of the cutoff tube. For this reason, shutoff pulse operation is not as reliable as with the bistable MV. The bistable MV circuit is basically suited for this purpose.

As noted in the data sheet, rectangular gates of either polarity are available at plates A and B. This can be seen from the symmetry of the bistable circuit, since, when the circuit is turned on, a particular tube such as B can be either in the cutoff or conducting state. In the sweep application mentioned above, a question arises as to the state of the tube from which the sweep gate is taken. In other words, how is the desired gate polarity established?

To illustrate, a graph of the operation is shown in figure 42-1. Briefly, assume the sweep circuit is operated with a negative gate and at the termination of the sweep a shutoff pulse is produced which is fed back to the bistable MV. If tube B is initially cut off (fig. 42-1a), the timing pulse will initiate the negative gate. In the event tube B is initially conducting (fig. 42-1b), no sweep will be generated by the first timing pulse. However, the multivibrator will recycle and proceeds normally with the second timing pulse. If the gate polarity required for the sweep circuit is positive, a positive gate is obtained in a manner



ESTABLISHING GATE POLARITY

Fig. 42-1

similar to that for the negative gate, except that the shutoff pulse occurs only when the gate is positive.

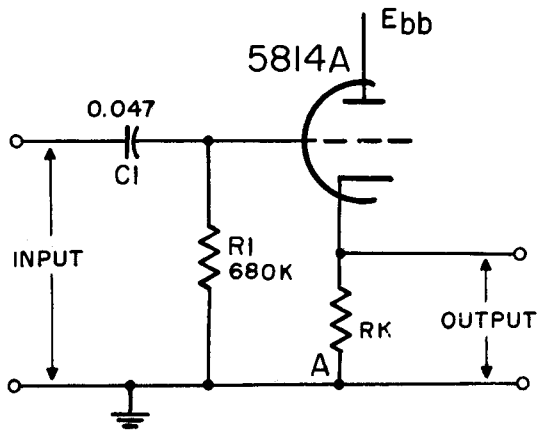
The input trigger can be of either polarity with the negative preferred. The shutoff pulse can be of either polarity also, but its duration is not critical since a fast decay time of the gate is not usually desired. The gates are formed by combinations of positive and negative transitions. The negative-going transition is inherently faster than the positive. The negative transition time is 0.7μsec and the positive is 2.5μsec.

As in PC 41, precautions should be taken when connecting associated circuits to the outputs. The rise and decay times given on the data sheet hold only if the total shunt capacity added does not exceed 15$\mu\mu$f. By dividing down on the plate resistor, a greater shunting capacity can be tolerated with a proportional loss of amplitude.

NBS PREFERRED CIRCUIT NO. 43
PULSE CATHODE FOLLOWER

NBS PREFERRED CIRCUIT NO. 43
PULSE CATHODE FOLLOWER

Unless otherwise stated;
R in ohms;
C>1 in $\mu\mu$f; C<1 in μf;
L in μh



This cathode follower is used to isolate critical circuits from loading effects by virtue of its high impedance input and low impedance output characteristics.

For R_K (Ω)	10K	10K	22K (−150v) [1]
E_{bb} (v)	150	300	300
Gain	0.87	0.87	0.9
Input limits (v)	0 to 70	0 to 170	−100 to 180
Output limits (v)	0 to 61	0 to 148	−90 to 162
Output impedance [2] (Ω)	300	420	300 [3]
Rise time (μsec)	0.02	0.02	0.02
Fall time [4] (μsec)	0.2	0.15	0.05

Input capacity: 2.5$\mu\mu$f. [5]
Droop: 1.5% for 500μsec pulse. [6]
R1: ±20% limits. C1: ±10% limits.

NOTES:

1. −150v connected at point A of R_K.
2. For 20v pulse.
3. 1400Ω for −20v pulse.
4. For 20v pulse and 15$\mu\mu$f added.
5. Excluding wiring.
6. For C1 = 0.01μf; droop 1.5% for 100μsec pulse.

PC 43 PULSE CATHODE FOLLOWER

1. APPLICATION

The cathode follower is used to isolate critical circuits from loading effects by virtue of its high input impedance. Circuit variations are given to accommodate a range of positive and negative input voltages. PC 22, Low-Level Cathode Follower, may be used when a circuit is to be matched to a low impedance line.

2. DESIGN CONSIDERATIONS

This cathode follower is characterized by a low input capacity and a fast rise time response which is in the order of 0.01 to 0.03μsec. However, the follower increases the transition time of negative-going edges of pulses, such as the fall time of a positive pulse or the rise time of a negative pulse (see fig. 43-5). The follower is also characterized by a low output impedance.

The output impedances listed on the data sheet were obtained by adjusting the load so as to reduce the output voltage to one-half the no-load value. Thus, in the case of a 20v signal, the output impedance is measured by the value of a load resistor (connected through a capacitor) which reduces the voltage to 10v. The effective output impedance for large signals depends upon pulse polarity. In the circuit using a -150v supply connected to a 22KΩ cathode resistor, the effective impedance is 300Ω for a positive pulse and 1400Ω for a negative pulse.

The rise time depends mostly upon the tube transconductance and associated electrode and added capacities. In most radar applications a rise time of 0.02 or 0.03μsec is adequate. With the 5814A tube and 30$\mu\mu$f added capacity, the rise time is of this order. [1]

In order to accommodate a range of input voltages, several circuit variations are given. The operating level limits indicate the region in which the grid begins to draw current. Another limiting condition is the heater-cathode breakdown voltage, which is $\pm$200v for the 5814WA. The cathode follower characteristic curves are shown in figures 43-1 and 43-2. The plate current can be determined by dividing the cathode voltage by the cathode resistance. When the cathode resistor is returned to -150v, the difference between the cathode voltage and -150v must be used.

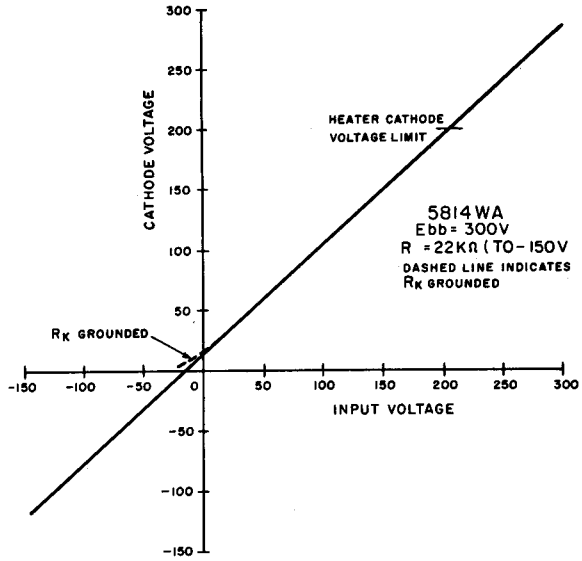


Fig. 43-1 CATHODE FOLLOWER CHARACTERISTIC FOR R_K = 22KΩ

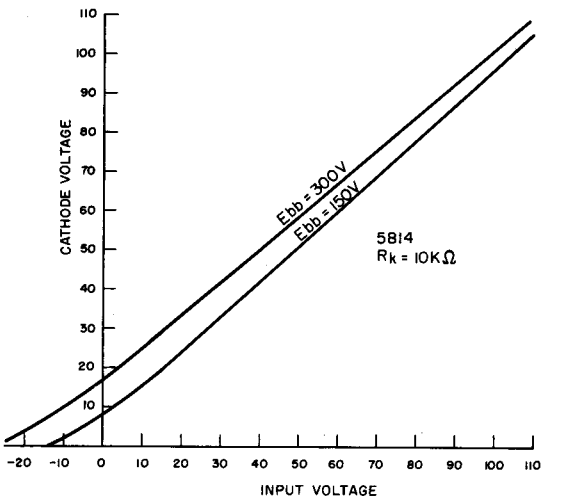


Fig. 43-2 CATHODE FOLLOWER CHARACTERISTIC FOR R_K = 10KΩ

The transition time for negative-going edges of a pulse is a function of amplitude, whereas positive-going edges are not markedly affected by amplitude. This is because of the difference in transconductance during the rise and fall of the pulse. The cathode resistor and associated

[1] M. B. Kline, "Cathode Follower Bandwidth," *Electronics*, June, 1949.

capacities are being driven by a source impedance, $1/g_m$. During the fall, the tube is nearer cutoff, therefore the transconductance is low and the pulse fall time is determined largely by the cathode resistor, associated capacity, and the

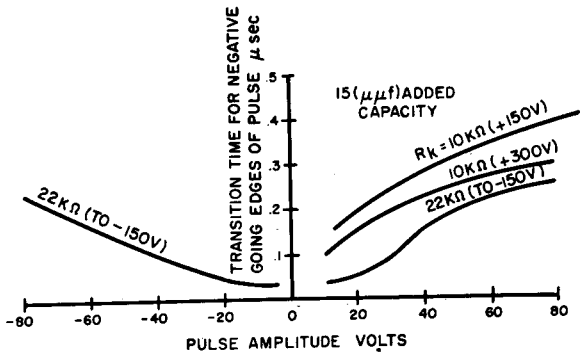


Fig. 43-3 VARIATION OF PULSE TRANSITION TIME WITH PULSE AMPLITUDE

amplitude of the pulse.[2] Figure 43-3 shows the deterioration of transition time as a function of amplitude for different circuit connections. The effect of using a negative supply connected to the cathode resistor is to improve the negative transition-time for positive and negative pulses. This is a result of the tube drawing higher plate current (higher g_m) in the quiescent state as compared to tubes operated with the resistor grounded. A similar result can be attained by connecting the grid-resistor return end to a divided cathode resistor.

The effect of added output capacity on the negative transition time is shown in figure 43-4. Here also the effect is more noticeable on the negative transition time; the positive transition time will also suffer, but is less noticeable. The curves show that the output capacity should be kept at a minimum if fast negative transition times are desired.

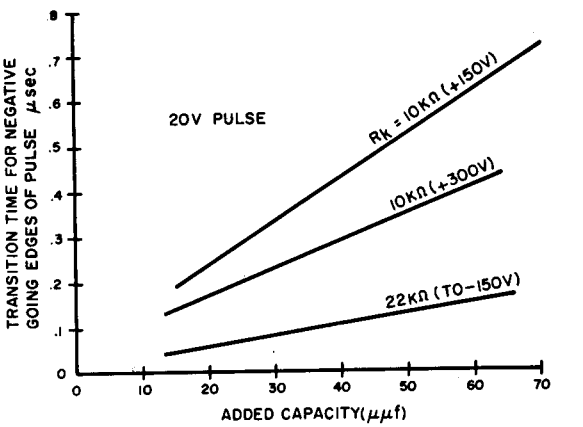
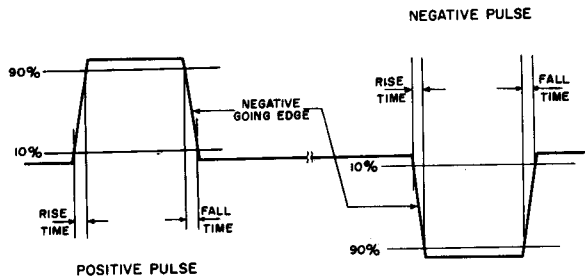
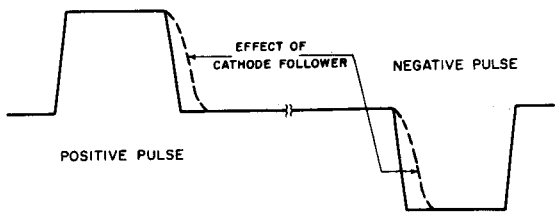


Fig. 43-4 VARIATION OF PULSE TRANSITION TIME WITH ADDED OUTPUT CAPACITY



(a) PULSE TRANSITION TIME DEFINITIONS



(b) EFFECT OF CATHODE FOLLOWER ON TRANSITION TIME

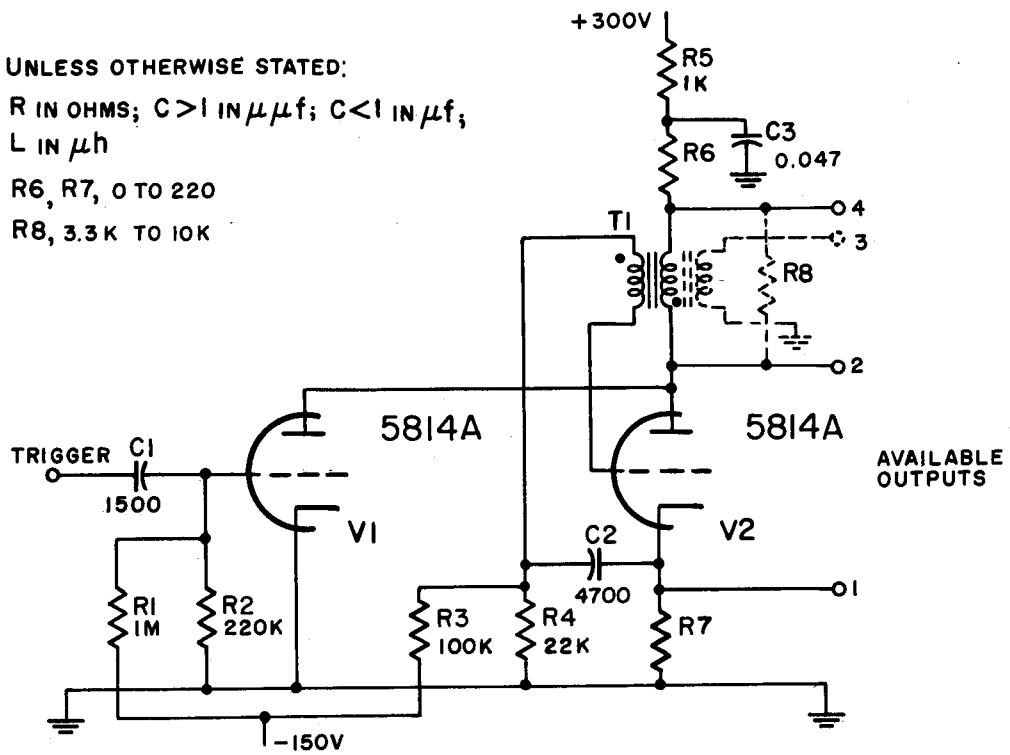
Fig. 43-5 EFFECT OF CATHODE FOLLOWER ON NEGATIVE GOING EDGES OF PULSES

The droop is a function of the input coupling circuit (see PC 21, Sec. 2). The droop is 1.5% for a 500μsec pulse. When high duty cycle signals are encountered it will be necessary to clamp the input to avoid the negative biasing effect when the grounded cathode resistor connection is used. When direct coupling is used the problem of droop is eliminated.

[2] William C. Elmore and Matthew Sands, *Electronics*, McGraw-Hill, 1949, p. 57.

NBS PREFERRED CIRCUIT NO. 46
PARALLEL-TRIGGERED BLOCKING OSCILLATOR

NBS PREFERRED CIRCUIT NO. 46
PARALLEL-TRIGGERED BLOCKING OSCILLATOR



R6 and R7 may be determined from the desired output voltage by assuming peak pulse current is 250ma. R8 used if required to prevent ringing; may be supplemented by a diode to eliminate overshoot.

Input:

PRF: 200 to 2000pps.

Trigger amplitude: 30v minimum

Output:

Pulse width: 0.1 to 5.0μsec
Rise time: 0.05 to 0.5μsec
} Determined by transformer T1.

Terminal	1	2	3	4
Polarity	Positive	Negative	Either	Negative
Amplitude [1]	0 to 50v	120 to 180v	120 to 180v	0 to 50v
Impedance	≈ R7	Z_o of T1	Z_o of T1	≈ R6
Maximum load C [2]	500μμf	10μμf	10μμf	500μμf

R3,R4: ±10%; R1,R2,R5,R6,R7,R8: ±20% limits. All C: ±20% limits.

NOTES:

1. Open circuit amplitudes are specified.
2. Shunt capacitance above the maximum specified will affect the wave shape of the blocking oscillator.

PC 46 PARALLEL-TRIGGERED BLOCKING OSCILLATOR

1. APPLICATION

Triggered blocking oscillators are used to produce nearly rectangular pulses of large amplitude with a minimum of components. A frequent application is to produce synchronizing pulses for modulators and indicators. The parallel-triggered blocking oscillator has less effect on the trigger source than the series-triggered type; however, there may be more delay between the trigger pulse and the blocking oscillator output. PC 46 is designed to furnish pulses between 0.1 and 5μsec wide at rates of 200 to 2000pps.

2. DESIGN CONSIDERATIONS

PC 46 employs a 5814A dual triode or its commercial prototype. One triode is used as a trigger amplifier and the other as the blocking oscillator.

The primary purpose of the trigger amplifier is to prevent the blocking oscillator from reacting on the trigger source. Except for the very narrow pulse widths (1μsec or less), an incidental advantage is the sharpening of the trigger pulse by amplification.

The minimum trigger requirements at the input to the circuit are an amplitude of 30v and a rate of rise of at least 100v per microsecond. The delay between the start of the trigger pulse and the start of the cathode output of the blocking oscillator under these conditions is between 0.25 and 0.35μsec. With an input amplitude of 50v, the delay is between 0.15 and 0.25μsec. Further increase in trigger amplitude produces little further decrease in delay.

The width of the trigger is not critical. The triggers are amplified by V1 and appear in differentiated form in the transformer outputs due to the action of the transformer itself. The positive pip at the leading edge of the trigger starts the blocking oscillator. The negative pip at the trailing edge appears in the transformer outputs, but its amplitude is negligible compared to the blocking oscillator pulse. A grid bias of 27v is obtained by a voltage divider from a negative 150v supply. C2 bypasses the bias supply directly to the cathode to remove the cathode resistor from the grid current path. This eliminates the degenerative effect of the cathode resistor which would otherwise cause changes in pulse width with changes in cathode load.

A compromise must be made in the choice of values for the resistor and bypass capacitor in the bias divider. The time constant, R4, C2, must permit the capacitor to discharge to the bias voltage before the succeeding trigger arrives or the blocking oscillator will not trigger reliably. With this limitation, C2 should be as high a capacitance as possible to minimize the voltage change during the pulse and permit the transformer to determine the pulse width. R4 may be as low as power dissipation considerations will permit. The values chosen permit recovery of the grid bias within the 500μsec period of the highest PRF for which the circuit is designed. Faster recovery times are accommodated by PC 47.

All the common pulse outputs of the blocking oscillator are shown in the circuit diagram. The output amplitudes specified will vary with different tubes and transformers.

The output amplitude at the plate and across the third transformer winding is between 40 and 60% of the supply voltage. The two waveforms are the same except for the spike on the plate output. The third winding is used when positive polarity or isolation from ground is required. A damping resistor (R8) is usually necessary with high "Q" transformers to prevent the circuit from squegging or, in extreme cases, oscillating. If the overshoot is objectionable, a diode may be used.

The characteristic impedance of blocking oscillator transformers is generally less than 1000Ω. Therefore resistive loads much higher than 1000Ω will not affect outputs 2 and 3. Shunt capacitance across any of the transformer windings will affect all the outputs, since the transformer largely determines the pulse characteristics. As shunt capacitance across a transformer winding increases, blocking oscillator performance is affected as follows:

(*a*) The time delay between the start of the trigger and the start of the blocking oscillator pulse increases.

(*b*) The trigger amplitude required at the input to the trigger amplifier increases.

(*c*) The rise time of the blocking oscillator pulse increases and the amplitude decreases.

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Outputs 1 and 4 across R6 and R7 are identical except for polarity. The maximum value recommended for either of these resistors is 220Ω because of the effect on the other outputs. As R6 increases, the blocking oscillator pulse width and the amplitude of the transformer outputs increase slightly. R7 has the same effect on pulse width, but it decreases the transformer output amplitudes. In all these cases the measurement with 220Ω in the circuit is about 10% different from the same measurement when the resistance is zero. The effects of load resistance and shunt capacitance on these outputs can be judged by the shunting effect on R6 or R7.

have the emission capabilities of the 5814A. There was more variation in performance between 12AT7's than between 5814's. Pentodes were rejected because they increase circuit complexity without appreciably improving the performance.

The selection of transformer T1 must be governed by the pulse characteristics required. Most manufacturers of pulse transformers will furnish them to specification if given the circuit and the desired waveform. A number of manufacturers have stock transformers available. The circuit was checked using ten stock transformer types made by two different manufacturers. In all cases the circuit performed within the limits

TABLE 46–1—*Performance of Parallel-triggered Blocking Oscillator*

Test conditions:	E_{bb}, E_{ff} normal	$E_{bb}-10\%$	$E_{ff}-10\%$
E_{bb}	300v	270v	300v.
E_{ff}	6.3v	6.3v	5.6v.
Trigger amplitude	30v	30v	30v.
Rise time	0.08μsec	0.08μsec	0.08μsec.
Delay	0.17μsec	0.22μsec	0.17μsec.
Plate output:			
Pulse width	1.4μsec	1.5μsec	1.35μsec.
Amplitude	200v	185v	190v.
Rise time	0.1μsec	0.1μsec	0.1μsec.
Cathode output ($R_7=100\Omega$):			
Pulse width	1.3μsec	1.4μsec	1.3μsec.
Amplitude	29v	26v	17v.
Rise time	0.1μsec	0.1μsec	0.1μsec.

Table 46–1 gives the performance of this circuit using a typical tube and transformer. The effects of a 10% decrease in supply voltages are also shown. The changes caused by a 10% increase in supply voltages are slightly smaller in magnitude and opposite in sense. With a well regulated power supply all these effects are negligible except the decrease in cathode signal amplitude with the decrease in filament voltage. This effect can be minimized by returning C2 to ground if the 10% decrease in pulse width can be tolerated.

The 5814A was selected over other MIL approved twin triodes because of its peak power capabilities. Slightly higher pulse amplitudes were obtainable with the 12AT7. However, no emission test is required of the 12AT7 by MIL–E–1B, and reliability reports [1] indicate its cathode does not

specified for PC 46 and within the manufacturer's specifications except for pulse width. The widths in some cases varied 50% from the value specified by the manufacturer. This can be expected unless the tube type and grid circuit capacitance are specified by the transformer manufacturer.

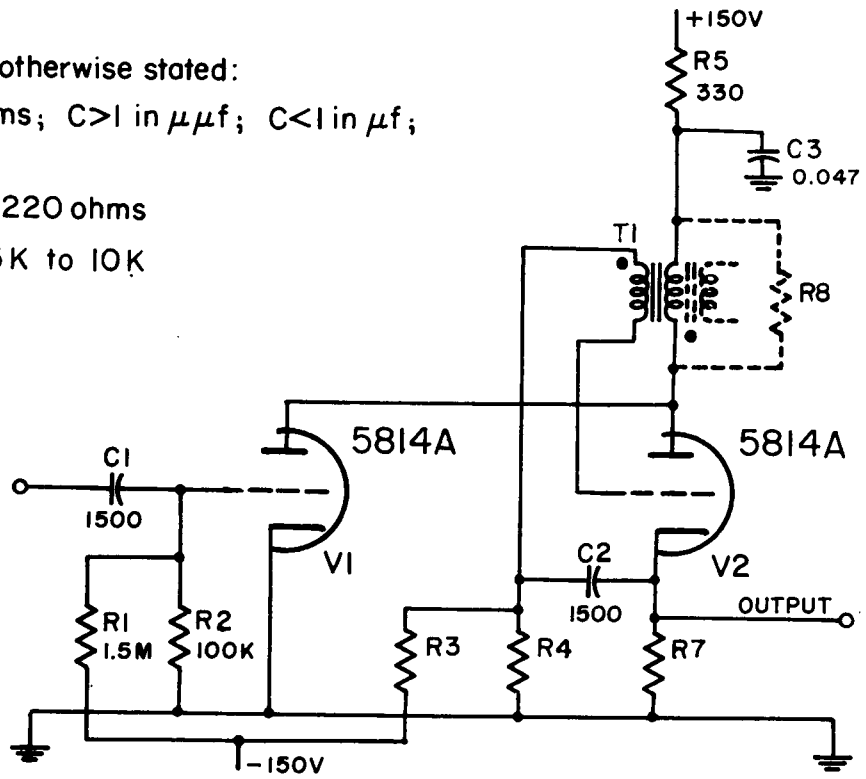
Unity turns-ratio between plate and grid will approximately match the grid and plate impedance of a 5814A in the positive grid region. This ratio results in best over-all performance of the circuit. A two to one step-down between plate and grid will produce higher amplitude voltage pulses (outputs 2 and 3) and will widen the pulses at all outputs. Stepping up the grid voltage will increase the current pulse amplitude (outputs 1 and 4).

[1] Aeronautical Radio, Inc., *General Report No. 1, Investigation of Electron Tube Reliability in Military Applications*, Jan. 4, 1954, p. 55.

NBS PREFERRED CIRCUIT NO. 47
TRIGGERED BLOCKING OSCILLATOR FOR FAST RECOVERY

NBS PREFERRED CIRCUIT NO. 47
TRIGGERED BLOCKING OSCILLATOR FOR FAST RECOVERY

Unless otherwise stated:
R in ohms; C>1 in $\mu\mu$f; C<1 in μf;
L in μh
R7, 0–220 ohms
R8, 3.3K to 10K



Pulse spacing μsec	R3	R4
12 to 60	47KΩ	4.7KΩ
60 to 500	100KΩ	10KΩ

R8 used if required to prevent ringing.
R7 may be determined by assuming peak pulse current is 200ma.

Input:
Maximum duty factor 0.05.
Trigger amplitude 30v.

Output:
Pulse width 0.1 to 2μsec
Rise time [1] 0.05 to 0.25μsec
} Determined by transformer T1.
Amplitude [1] 0 to 40v.
Impedance≈ R7.

Delay (start of trigger to start of output): 0.15 to 0.25μsec.
R3,R4: ±10%; R1,R2,R5,R6,R7,R8: ±20% limits. All C: ±20% limits.
NOTE:
1. Open circuit amplitude and rise time are specified.

PC 47 TRIGGERED BLOCKING OSCILLATOR FOR FAST RECOVERY

1. APPLICATION

PC 47 is a triggered blocking oscillator designed to respond to trigger pulses which are separated by only a few microseconds. Applications for this circuit occur in distance-mark generators and in circuits where antenna position information must be relayed to a remote indicator.

2. DESIGN CONSIDERATIONS

PC 47 is similar to PC 46. The circuit has been modified slightly to permit the blocking oscillator to be triggered by pulses separated as little as 12μsec.

The time constant in the blocking oscillator grid circuit has been reduced. The limiting values for C2, R3, and R4 are discussed in PC 46. The minimum value for C2 is 1500$\mu\mu$f if the transformer is to retain control over the pulse width.

The plate voltage has been reduced from 300 to 150v. This has two advantages. Reduction of the peak current through the tube permits use of a higher duty factor. It also reduces the bias required to keep the blocking oscillator cut off. This permits reducing R4 (to reduce the grid circuit time constant) without drawing excessive current from the bias supply. The values of R1, R2, and R3 have also been changed because of the change in bias voltages.

The reduction in plate supply voltage also reduces the amplitude of the outputs. This is not a disadvantage in most applications of this circuit. If higher amplitudes are required, a 300v plate supply may be used if the bias is increased and duty factor decreased accordingly.

Although the cathode output is the only one shown, any of the outputs shown in PC 46 may be used if required. Except for polarity, the output obtainable from a series resistor in the plate circuit is the same as the cathode output using the same resistance. The amplitude of the output at the plate or third winding of the transformer will be between 75 and 125v depending on the transformer used.

The remarks in PC 46 concerning tube type, transformer, and the effects of load and power supply changes also apply to PC 47.

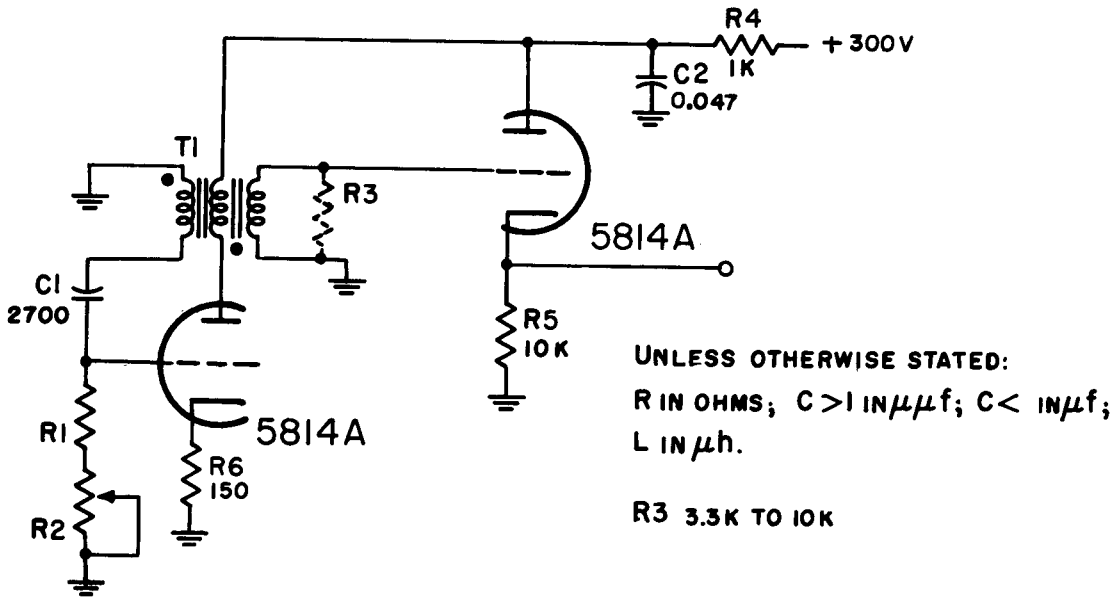
The performance of this circuit using a typical tube and transformer is shown in table 47-1.

TABLE 47-1—*Performance of PC 47*

Trigger amplitude	30v.
Rise time	0.2μsec.
Cathode output (R_7=100Ω):	
Pulse width	1.2μsec.
Amplitude	20v.
Rise time	0.25μsec.
Delay between 10% amplitude points on trigger and output waveforms	0.2μsec.

NBS PREFERRED CIRCUIT NO. 48A
BLOCKING-OSCILLATOR PRF GENERATOR

NBS PREFERRED CIRCUIT NO. 48A
BLOCKING-OSCILLATOR PRF GENERATOR



C1,R1, and R2 determine the pulse repetition period according to the equation

$$T = (R1+R2)C1 \ln E_i/E_f$$

where E_i = voltage across $(R1+R2)$ at beginning of discharge.
E_f = voltage across $(R1+R2)$ at end of its discharge.

Actual values must be determined experimentally: for a first approximation assume E_i = 150v and E_f = 18v.

PRF: 200 to 2000pps.

Frequency Stability: ±5%.

Output:

Pulse width: 0.1 to 5.0μsec
Rise time: 0.05 to 0.5μsec
} Determined by transformer T1.
Amplitude: 100v
Impedance: ≈ 400Ω.

All R: ±20% limits. All C: ±20% limits.

NOTE: Open circuit amplitudes are specified.

PC 48A BLOCKING-OSCILLATOR PRF GENERATOR

1. APPLICATION

The blocking-oscillator PRF generator is used to generate a repetition rate where stability requirements are low. The output can be used as a trigger without further shaping. The principal disadvantage is the poor frequency stability. The circuit is particularly sensitive to changes in filament voltage; a 10% decrease in filament voltage may change the frequency as much as ±2%. Other factors contribute an additional 1 or 2%.

2. DESIGN CONSIDERATIONS

The period of a free-running blocking oscillator is determined principally by the discharge time constant in the grid circuit, as shown in figure 48-1. However, since C1 partly determines the pulse width as well as the discharge time, the values of C1, R1, and R2 are best determined experimentally.

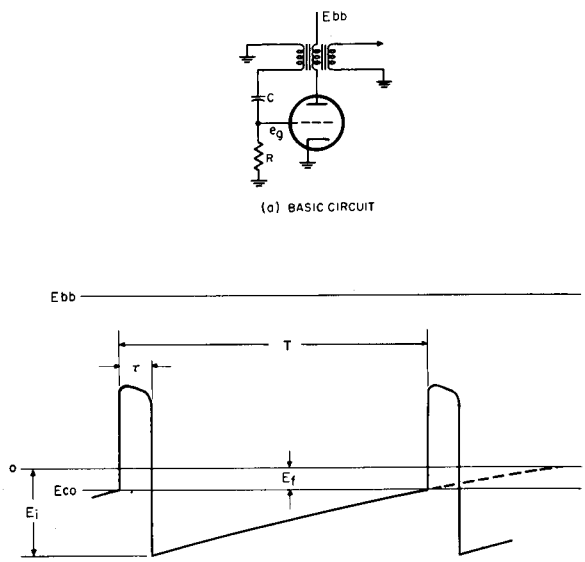


Fig. 48-1 BLOCKING OSCILLATOR

If C1 is so large that its voltage does not change during the pulse, the pulse-width is determined by the transformer alone. As C1 is decreased the charge gained during the pulse causes its voltage to rise. Since the blocking-oscillator grid-voltage is the difference between the capacitor voltage and the voltage across the grid winding of the transformer, a rise of capacitor voltage causes the grid voltage to fall faster than when the action depends on the transformer alone. This shortens the pulse.

The voltage across C1 must be allowed some increase because it becomes the initial voltage from which C1 must discharge during the interval between pulses. Values of C1 between 0.001 and 0.01μf are suitable in most cases. The size of C1 has no effect on the rise time of the pulse and negligible effect on amplitude.

Since R is large compared to the internal grid-cathode resistance of the tube when the grid is positive, it does not affect the charging of C1. The value of R can be chosen solely on the basis of the discharge time constant required for the given period. In using the formula to determine $R=(R1+R2)$, a useful first approximation is to assume $E_i=E_{bb}/2$ and $E_f=E_{bb}/\mu$. R2 must be a sufficient fraction of R to be capable of changing the frequency about 40% to accommodate different tubes.

The main factors affecting the frequency stability of the blocking oscillator are:

(*a*) The stability of R1, R2 and C1: By careful component selection, RC can be kept sufficiently constant with temperature changes to have a negligible effect.

(*b*) Changes in tube parameters: These changes are negligible over the life of any particular tube, but there are enough differences among MIL tubes of the same type to cause frequency changes as high as 20%. A number of circuits that have been suggested to minimize this effect are discussed in section 5.3 of "Notes to the Preferred Circuits Manual."

(*c*) Changes in supply voltages: The magnitude of these changes varies from tube to tube; in general, the effects are small except for a decrease in filament voltage. The PRF changes about ±1.0% with a ±10% change in plate voltage or a 10% increase in filament voltage. A 10% decrease in filament voltage may cause a ±2% change in frequency. In addition, there are random short time frequency changes of a few tenths of a percent.

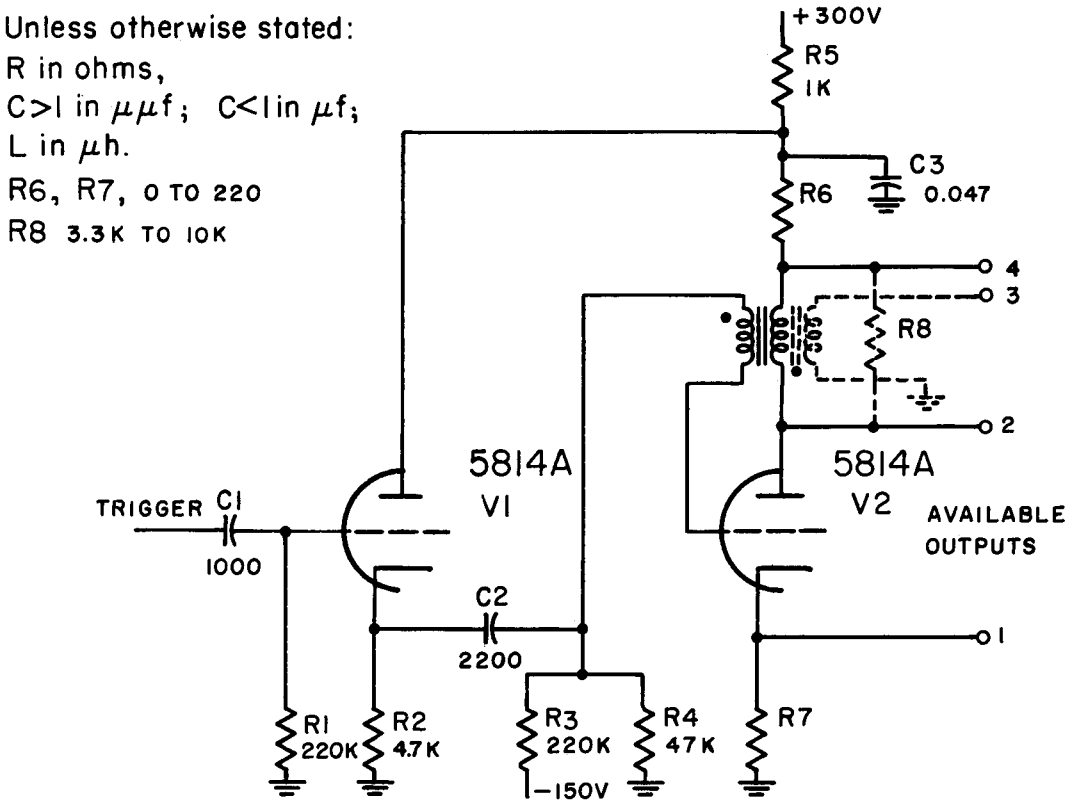
The preferred circuit consists of a free-running blocking oscillator, transformer-coupled to a

cathode follower. The circuit includes a 150Ω cathode resistor to minimize the change in frequency with change in filament voltage.

The cathode follower is included to minimize the effects of the load on the frequency. Its gain with the 10KΩ cathode resistor is about 0.9. The high cathode resistance results in a very long fall time, which is generally not objectionable in synchronizing pulses. If less amplitude is permissible, a reduction in the resistance of R5 will improve the output waveshape (see PC 43).

NBS PREFERRED CIRCUIT NO. 49
SERIES-TRIGGERED BLOCKING OSCILLATOR

NBS PREFERRED CIRCUIT NO. 49
SERIES-TRIGGERED BLOCKING OSCILLATOR



R6 may be determined by assuming peak plate current is 250ma.
R7 may be determined by assuming peak cathode current is 330 ma.
R8 used if required to prevent ringing; may be supplemented by a diode to eliminate overshoot.

Input:

PRF 200 to 2000pps.

Trigger amplitude: 30v to 50v.

Output:

Pulse width: 0.1 to 5.0μsec
Rise time: 0.05 to 0.5μsec
} Determined by transformer T1.

Terminal	1	2	3	4
Polarity	Positive	Negative	Either	Negative
Amplitude [1]	0 to 70v	120 to 180v	120 to 180v	0 to 50v
Impedance	≈R7	Z_o of T1	Z_o of T1	≈ R6
Maximum load C [2]	500μμf	10μμf	10μμf	500μμf

Delay [3] 0.1μsec to 0.2μsec.

R3,R4: ±10%; R1,R2,R5,R6,R7,R8: ±20% limits. All C: ±20% limits.

NOTES:

1. Open circuit amplitudes are specified.
2. Shunt capacitance above the maximum specified will affect the wave shape of the blocking oscillator.
3. Delay measured between start of trigger and start of cathode output.

PC 49 SERIES-TRIGGERED BLOCKING OSCILLATOR

1. APPLICATION

Although the applications are basically the same as for the parallel-triggered type, the series-triggered blocking oscillator will respond to a more slowly rising trigger and requires a low impedance trigger source. There is considerable reaction on the trigger even if a cathode follower is used for triggering.

2. DESIGN CONSIDERATIONS

PC 49 is a series-triggered blocking oscillator employing a 5814A. Except for the method of triggering, the circuit is the same as PC 46. The data on bias and outputs in PC 46 also apply to PC 49. As in PC 46 the 5814A was chosen on the basis of its power and current rating. Any pulse transformer that will furnish the desired pulse characteristics may be used.

One of the triodes is used as a cathode follower to obtain a low impedance and to provide some isolation between blocking oscillator and trigger source. Even with the cathode follower, PC 49 is likely to load the circuit preceding it. Since the effective resistance of the cathode follower output is low compared to R4, the larger part of the blocking oscillator grid current flows through R2 and this current is sufficient to drive the cathode follower grid positive. This will not interfere with the operation of the blocking oscillator, but the effect on the trigger source should be considered. A diode in parallel with R2 with cathode connected to V1's cathode will minimize this effect.

The cathode follower is not essential to the operation of the circuit. C2 may be connected to any low impedance trigger source if the grid current flow during the pulse is not detrimental to trigger operation. If the impedance of the trigger source is a few hundred ohms, the operation will be the same as with the cathode follower. Impedances of several thousand ohms are permissible if decreases in pulse width of 20% are not objectionable.

There are two principal sources of delay in any blocking oscillator circuit: the time required for the blocking oscillator grid voltage to rise to its cutoff value, and the interval between the time the tube conducts and the time that regeneration occurs. The latter is a function of the transformer inductance and tube type and is essentially the same for either a series or parallel trigger. The former depends on the trigger amplitude and rise time, the gain of the trigger amplifier, and the fixed bias on the blocking oscillator.

The series trigger minimizes the delay by eliminating the transformer as a coupling element between the trigger tube and the blocking oscillator grid. This reduction of the delay is partly counteracted because the requirement for a low-impedance trigger source necessitates the use of a cathode follower with resulting loss in trigger amplitude. The parallel trigger compensates for the delay associated with the coupling transformer by providing amplification in the trigger tube. When pulse widths shorter than one microsecond are desired, however, the transformer inductance is only a few tenths of a millihenry and the trigger amplifier gain is near unity. In this case the series trigger results in less delay. The series trigger is also necessary when a slowly rising trigger is used.

As part of the grid return path, C2 partly determines the pulse width and its capacitance should be kept high to realize the rated pulse width from the transformer. As part of the trigger coupling network, the capacitance of C2 should be kept high to minimize the trigger attenuation. A maximum is set by the time constant R4, C2 which must be low enough to permit C2 to discharge to the fixed bias before the following trigger occurs. A longer time constant will cause V2 bias to rise, increasing the delay.

If the interval between trigger pulses is short, the time constant in the grid circuit should be reduced as follows:

Pulse spacing	C2	R3	R4
12 to 60μsec	680μμf	22KΩ	4.7KΩ
60 to 500μsec	2200μμf	47KΩ	10KΩ

The value of 680μμf for C2 will reduce the pulse width about 25%. R5 should be reduced to 330Ω in both cases.

Supply voltage changes have little effect on the operation of the circuit. Filament voltage changes of 10% have negligible effect. Plate voltage changes of 10% result in 10% amplitude changes and a slight change in pulse width. This effect is minimized if both plate and bias supplies change simultaneously.

Table 49–1 (p. 49–4) gives the performance of this circuit.

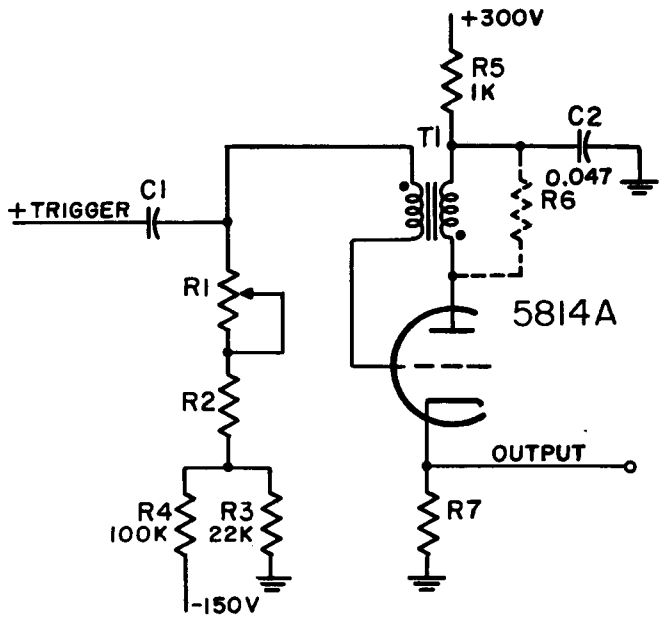
TABLE 49–1
Performance of Series-Triggered Blocking Oscillator

Trigger	
Amplitude	30v.
Rise time	0.07μsec.
Delay	0.1μsec.
Third winding output:	
Pulse width	1.3μsec.
Amplitude	175v.
Rise time	0.16μsec.
Cathode output (R7 = 100Ω):	
Pulse width	1.1μsec.
Amplitude	38v.
Rise time	0.20μsec.

NBS PREFERRED CIRCUIT NO. 50
BLOCKING OSCILLATOR PULSE-FREQUENCY DIVIDER

NBS PREFERRED CIRCUIT NO. 50
BLOCKING OSCILLATOR PULSE-FREQUENCY DIVIDER

R6 3.3K TO 10K (see note 1)
R7 15 TO 220 ohms



Unless otherwise stated:
R in ohms;
C>1 in $\mu\mu$f; C<1 in μf
L in μh

Blocking oscillator PF dividers are used for division of the input pulse frequency by 2, 3, 4 or 5.

Output PF	>300pps	300 to 600pps	>600pps
C1	1500$\mu\mu$f	1000$\mu\mu$f	470$\mu\mu$f

[2] Rg(max.) $\approx$ T/0.7C Rg(min.) $\approx$ T/2.2C
[3] R1 = Rg(max.) − Rg(min.) R2 = Rg(max.) − (R1+18KΩ)

	Input	*Output*
PF	400 to 10,000pps	200 to 2,000pps
Duty cycle		0.05 max.
Pulse amplitude	30v±10%	70v max.
Rise time		0.05 to 0.13μsec
Polarity [4]	Positive	Positive
Pulse width		Determined by T1
Impedance	400 ohms max.	≈R7
Delay [5]		0.1 to 0.25μsec

R3,R4: ±10%; R1,R2,R5,R6,R7: ±20% limits. All C: ±20% limits.

NOTES:

1. The maximum resistance which just prevents ringing should be used so that loading is minimum.
2. Total resistance required in the gird circuit for an output pulse spacing of T microseconds.
3. Use the nearest preferred resistor values.
4. See PC 46 for other possible outputs.
5. Between the 10% points of the input and corresponding output pulses.

PC 50 BLOCKING OSCILLATOR PULSE-FREQUENCY DIVIDER

1. APPLICATION

Blocking oscillator pulse-frequency dividers produce equally spaced pulses at a submultiple of the trigger pulse-frequency. In radar circuits, frequent uses are to divide down from a high to a low pulse-frequency (PF) and to produce distance marks.

2. DESIGN CONSIDERATIONS

PC 50 employs one-half of a 5814A twin triode or its equivalent in a blocking oscillator frequency divider, which can be adjusted to divide by any number between two and five. Division by more than five is possible but not recommended because operation is likely to be unstable. Basically, the circuit is a series-triggered blocking oscillator adjusted so that it fires on the second to the fifth input pulse, depending on the division desired.

The cathode output is shown because it is normally used in this application of blocking oscillators. However, any of the other outputs shown in PC 46 can be used if the precautions noted are observed.

The bias voltage is chosen on the basis of the trigger amplitude, triggering level, stability of count, and range of cutoff voltages, which for a 5814A is -16 to -19v. The bias voltage used is -27v.

The most desirable triggering level in this type of frequency divider is the point on the exponential grid voltage where the discrimination between the desired trigger and those immediately adjacent is maximum. Where this maximum change occurs is explained in Sec. 7.3 of the Notes. The level at which the change occurs depends on the initial voltage across the coupling capacitor (E as shown in fig. 50-1) and the discharge time constant T/R_gC, where R_g is the resistance in the grid circuit, C is the coupling capacitor, and T is the period in μsec between output pulses.

The value of C1 was chosen on the basis of its effect on the initial grid voltage, the trigger amplitude, and the output pulse width. Small values of C1 are required for maximum initial grid voltage, essential for maximum stability at high divisions. Large values of C1 are desirable for minimum attenuation of the trigger amplitude and output pulse width. (See Notes, Sec. 7.3)

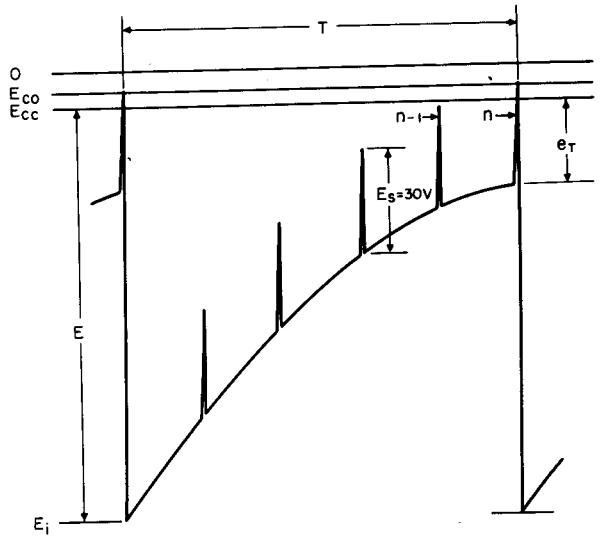


Fig.50-1 VOLTAGE ACROSS C1

A reasonable compromise in the value of C1 is about 500$\mu\mu$f. In this design larger capacitors (up to 1500$\mu\mu$f) are used only where necessary to limit total grid resistance required (for long output pulse spacings).

Since the impedance of the trigger source limits the initial voltage to which the coupling capacitor charges, its value should be less than 400Ω, resulting in a reduction in E of less than 10%.

Theoretically, there is an optimum trigger amplitude for each tube and transformer. To permit triggering with a 30v pulse for tubes within MIL-E-1B specifications and pulse transformers whose capacitor voltage, E, varies over the range 50v to 150v, the grid resistance must be variable between the limits given for R_g(max.) and R_g(min.) on the data sheet.

3. PERFORMANCE

This circuit will operate stably with small simultaneous variations in supply voltages and in trigger amplitude—at least $\pm 10\%$ for plate, bias, and filament supplies and $\pm 10\%$ for trigger amplitude—without readjustment of R1. (Originally, R1 should be adjusted halfway between the position for a division $(n-1)$ and that for a division of $(n+1)$, and will require readjustment only when a tube or component is replaced).

The output pulse amplitude varies $\pm 10\%$ with tubes of MIL specification limits for a given trans-

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former, and for different transformers, varies ±20%. The effects of load resistance and shunt capacitance on these outputs can be judged by the shunting effect on R7.

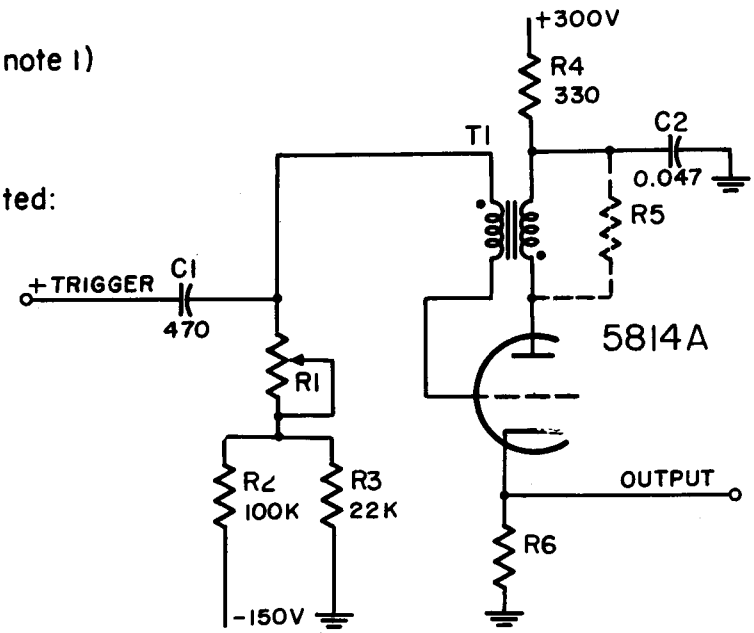
The pulse delay increases with increasing trigger rise time and varies slightly between different transformers for the same trigger rise time (see PC 51).

NBS PREFERRED CIRCUIT NO. 51
BLOCKING OSCILLATOR DISTANCE-MARK DIVIDER

NBS PREFERRED CIRCUIT NO. 51
BLOCKING OSCILLATOR DISTANCE-MARK DIVIDER

R5 3.3K to 10K (See note 1)
R6 0 to 220 ohms

Unless otherwise stated:
R in ohms;
C>1 in $\mu\mu$f;
C<1 in μf.



Input pulse spacing (μsec)	*Division by—*	*Output pulse spacing (μsec)*	*R1 (Ω)*	*T1 output pulse width (μsec)*
12.2 or 15.25	5 or 4	61	250K	0.5
20.33 or 30.5	3 or 2	61	250K	0.5
61	2 and 3	122 and 183	500K	1.0
	4 and 5	~~244~~ 305 and ~~488~~ ~~610~~ 305	~~2.5M~~ 1.0M	~~1.0~~ 1.5
122	2 and 3	~~244~~ 366	1M	1.5
	4 and 5	488 and 610	2.5M	1.5

	Input	*Output*
Duty cycle		0.05 max.
Pulse amplitude	30v $\pm$ 10%	70v max.
Rise time	0.13μsec max.	0.05 to 0.25μsec
Polarity [2]	Positive	Positive
Pulse width		0.5 to 1.5μsec
Impedance	400Ω max.	$\approx$ R6
Pulse delay [3]		0.25μsec max.

R2,R3: $\pm$10%; R1,R4,R5,R6: $\pm$20% limits. All C: $\pm$20% limits.

NOTES:

1. Use maximum resistance that will prevent ringing.
2. See PC 46 for other possible outputs.
3. Measured between 10% points of input and output pulses.

PC 51 BLOCKING OSCILLATOR DISTANCE-MARK DIVIDER

1. APPLICATION

Often the input to a blocking-oscillator divider is a pulse train. One of the most common applications of blocking-oscillator dividers is the generation of distance marks in radar equipment. When several different distance marks are to be displayed simultaneously, cascaded dividers are frequently employed.

2. DESIGN CONSIDERATIONS

PC 51 employs one half of a 5814A twin triode or electrical equivalent. The general principles of blocking-oscillator dividers are explained in PC 50. In PC 51 definite frequencies are known and the grid circuit values can be specified. Since operation is periodic, fixed bias must be used. The cathode output affords a convenient means for cascading dividers although any of the outputs shown in PC 46 may be used. Division by more than five in any one stage is not recommended.

Maximum pulse widths of distance markers are determined by the resolution required on the viewing device. The adjustment, R1, in the grid circuit is required because of the wide range of initial voltages (about 3 to 1) among pulse transformers and the variation of grid current flow between tubes. The trigger amplitude limits, therefore, are the same as in PC 50.

As was pointed out in PC 50, a small coupling capacitor is most desirable in the design since a large initial voltage is necessary, especially at divisions of four and five. The use of a large capacitor is nevertheless consistent with limiting the maximum total grid resistance. In this design, however, the lowest output pulse frequency, 1650pps, is greater than that prescribed in PC 50

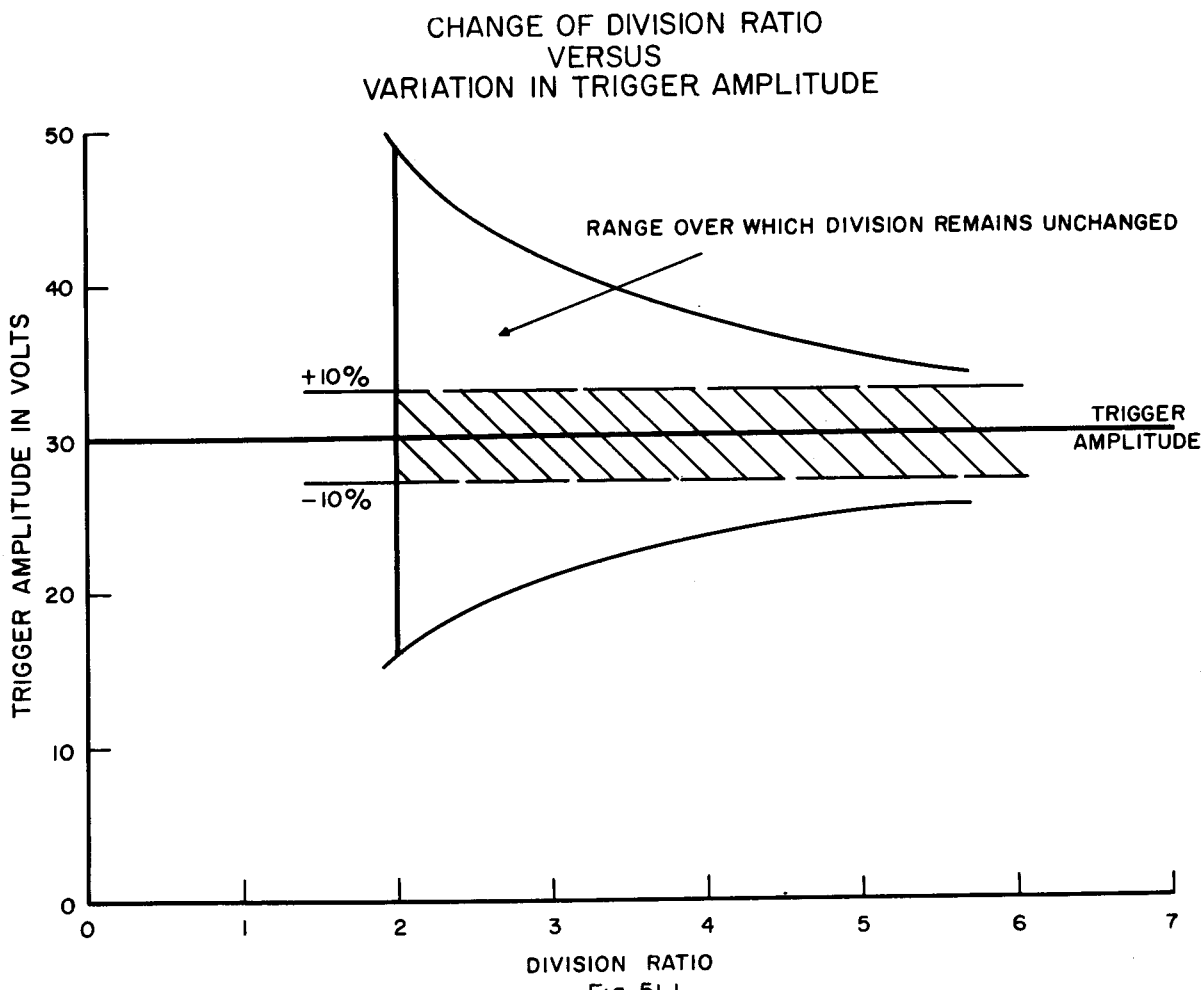


Fig. 51-1

as the low limit when using a 470$\mu\mu$f coupling capacitor, justifying the use of 470$\mu\mu$f for all the distance dividers.

The adjustment, R1, permits variation of the parameter T/R_gC (where T is the period between output pulses in microseconds and R_gC is the grid circuit time constant) between the limits 0.7 and 2.2 to accommodate a 30v trigger regardless of the transformer being used. This adjustment should be set half-way between that needed for a division of $(n-1)$ and $(n+1)$, where n is the desired division. Under these conditions no readjustment should be needed if variation of circuit parameters are within the limits specified.

3. PERFORMANCE

The trigger amplitude may vary at least $\pm 10\%$ before the divider designed for a division of five becomes unstable (fig. 51-1). The permissible variation is greater for smaller divisions. The output amplitude varies within $\pm 20\%$ for a given cathode resistor for transformers whose initial voltages are between the limits of 50v and 150v, and tubes within MIL-E-1B specifications. The pulse delay is small for trigger rise times ranging from 0.05 to 0.13μsec, but is large for trigger rise times of 0.15μsec or larger (fig. 51-2). If the trigger rise time is 0.1μsec or less, the pulse delay is less than 0.2μsec (equivalent to a delay of less than 35 yards).

The divider remains stable with the following supply voltage changes. The division (of five) remained the same without readjustment: (1) as the plate supply voltage varied between 200v and 500v, (2) for a heater voltage change from 5.1 to 8.5v, and (3) for $\pm 10\%$ variation in the bias supply, these changes not occurring simultaneously. When a tube is replaced, R1 should be adjusted as described above. The output pulse width is unaffected by the input pulse width except when they are within $\pm 15\%$ of each other. This lengthens the output pulse width slightly (usually less than 10%). For a given transformer, the pulse width obtained in a divider of this type is narrower than in triggered blocking oscillators designed for lower PF's (PC 47). This is due chiefly to the small coupling capacitor required in this design.

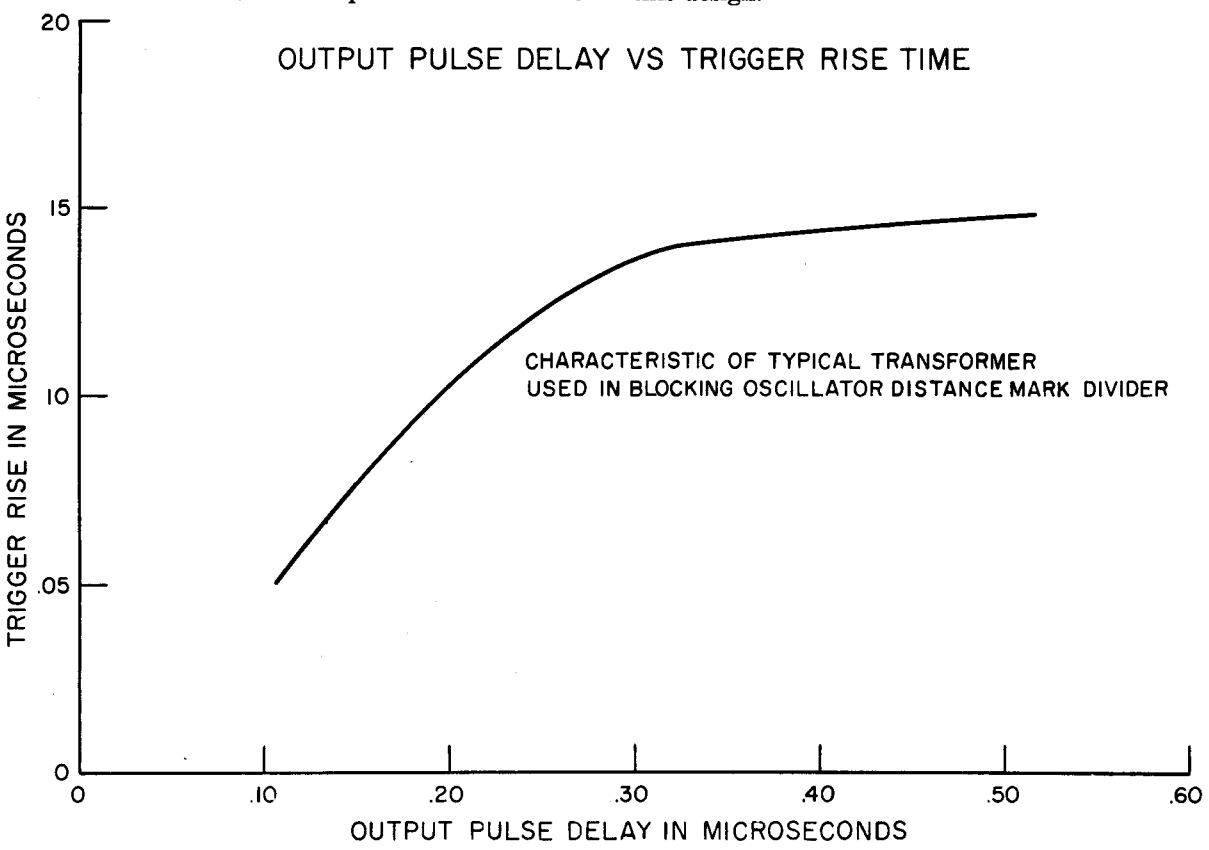
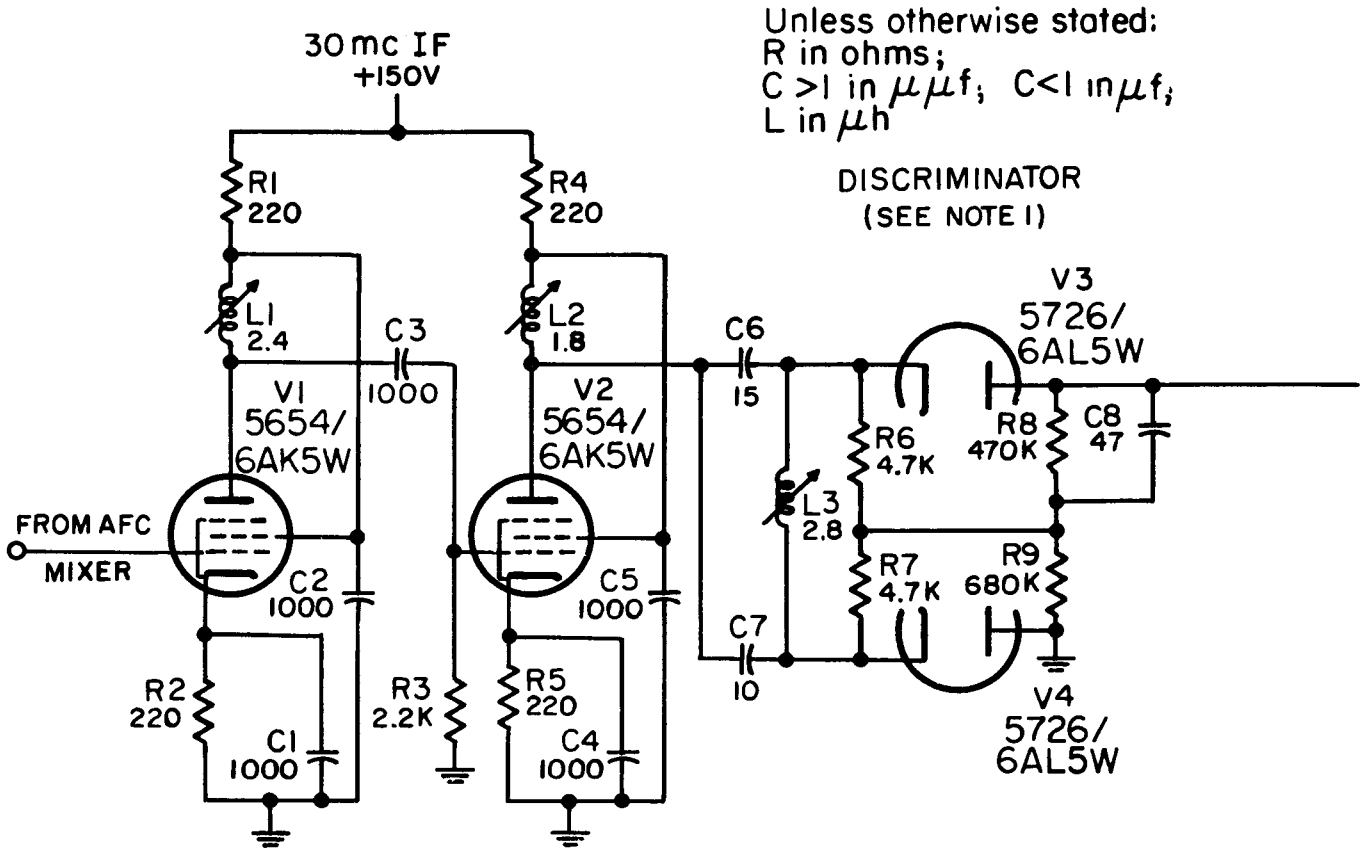


Fig. 51-2

NBS PREFERRED CIRCUIT NO. 53
PULSE AUTOMATIC FREQUENCY CONTROL, 30 MC IF

NBS PREFERRED CIRCUIT NO. 53
PULSE AUTOMATIC FREQUENCY CONTROL, 30 MC IF



Components:

R23,R24,R25,R27: See section 2.7 (e).

C12=C13 $\approx \frac{3750}{f_s}$ μμf, where f_s is the desired search frequency.

R3,R10: ±5% limits; all other R: ±20% limits. (Note 3)

C6,C7: ±5% limits; all other C: ±20% limits.

Operating characteristics:

Input:

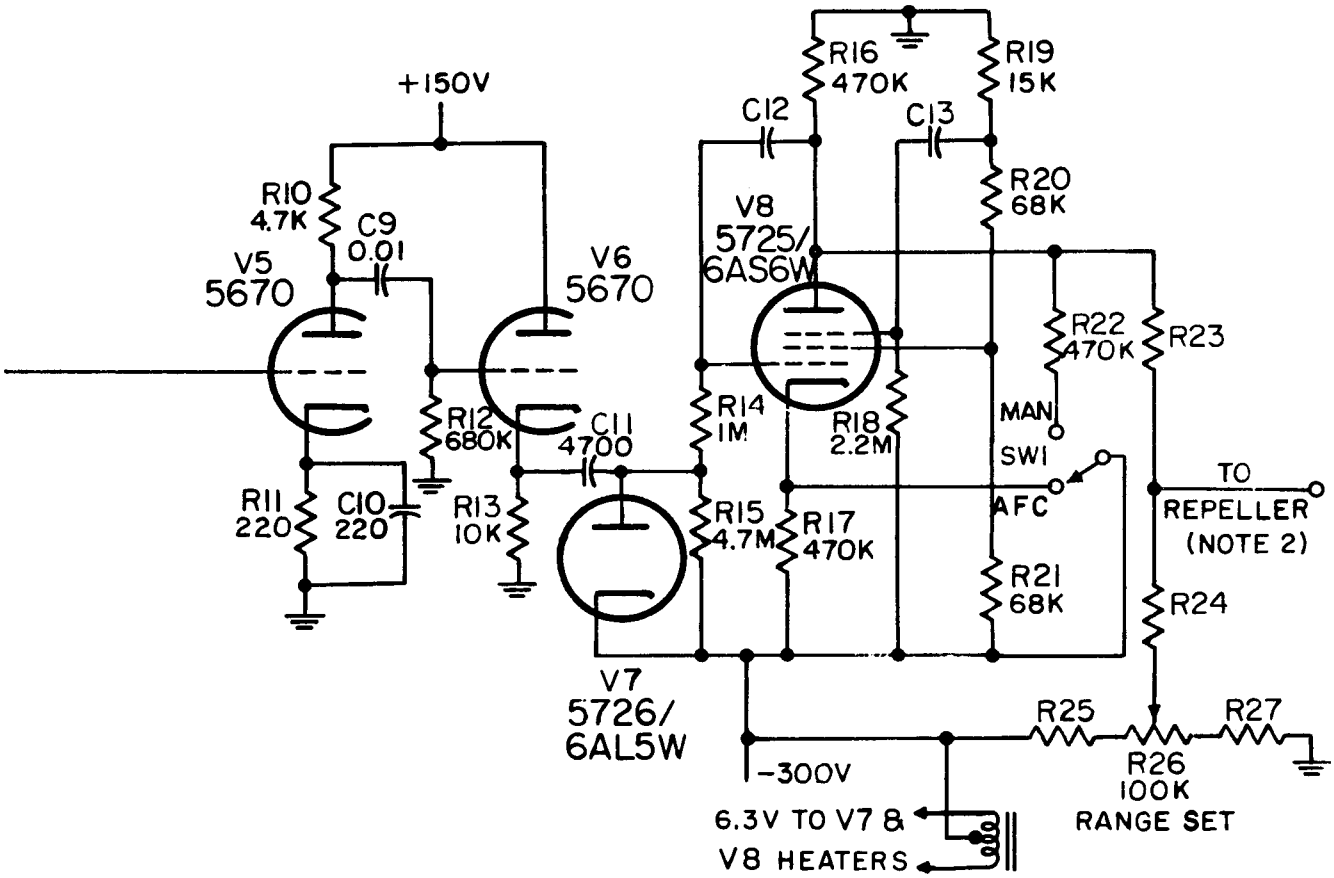
Waveform	Pulsed rf
Center frequency	30 mc
Pulse width	0.5 to 5.0 μsec
Pulse amplitude	200 mv peak (Note 4)
Duty factor	0.0002 to 0.001
Maximum harmonic ratio	−26 db

Output:

30 mc < input frequency < 32 mc

Waveform	Variable dc
Range	±10 to ±75 volts
~~Range center~~ Average Level	0 to −200 volts

VIDEO AMPLIFIER SEARCH STOPPER CONTROL CIRCUIT



$0 < f_{in} < 30$ mc; 32 mc $< f_{in} < \infty$

Waveform	Sawtooth
Frequency	0.1 to 10 cps
Amplitude	20 to 150 volts
Average level	0 to −200 volts
Recovery time	0.5% of sweep period

Power requirements:

+150 volts dc ±1%	35 ma maximum
−300 volts dc ±1%	7.5 ma maximum
6.3 volts ac ±10% (grounded)	1 ampere
6.3 volts ac ±10% (returned to −300v)	0.475 ampere

NOTES:

1. The discriminator output is of the correct polarity to maintain the frequency of a klystron local oscillator 30 mc above the transmitter signal.

2. If the line to the local oscillator control element is long, bypassing should be provided at the local oscillator. An RC circuit with a time constant not greater than 5% of the pulse repetition period is sufficient.

3. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified above. Thus, the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.

4. See section 2.2 for other input levels.

PC 53 PULSE AUTOMATIC FREQUENCY CONTROL, 30 MC IF

1. APPLICATION

PC 53 is intended for use in pulse modulated systems to maintain a difference of 30 mc between the transmitter and local oscillator frequencies. The preferred circuit (shown on pages 53–2 and 53–3) will maintain the local oscillator at a frequency 30 mc higher than the transmitter frequency. If the local oscillator is required to operate at a frequency 30 mc lower than that of the transmitter, the discriminator diodes, V3 and V4, should be reversed. In either case, the circuit must be adjusted so that the local oscillator will not sweep through the image frequency or it will lock improperly on the wrong sideband. (See Notes to the Preferred Circuits Manual, section 13.3 (b).) The circuit is classified as a hunting system,[1] since the local oscillator is swept over a band of frequencies to find the correct operating point.

Applications are restricted to systems employing pulse widths between 0.5 and 5 μsec at duty factors between 0.001 and 0.0002. The circuit is designed for a signal level of 200 mv at the input to the IF amplifier, but provisions are made for changing the amplification to accommodate input levels between 50 and 500 mv. The harmonic ratio must be less than 0.05. Although the circuit is normally employed with a klystron local oscillator, it may be used with any local oscillator whose frequency can be controlled by a voltage change of 20 to 150 volts at an average level between 0 and −200 volts.

2. DESIGN CONSIDERATIONS

PC 53 includes the portion of the afc circuit between the mixer and local oscillator, as shown in figure 53–1.

2.1 *General:* The following design considerations, although they apply to portions of the afc system not included in PC 53, are discussed because they affect the design of the preferred circuit.

[1] R. V. Pound and E. Durand, *Microwave Mixers*, *Rad. Lab. Series*, vol. 16, McGraw-Hill, N. Y., N. Y., 1948, p. 295.

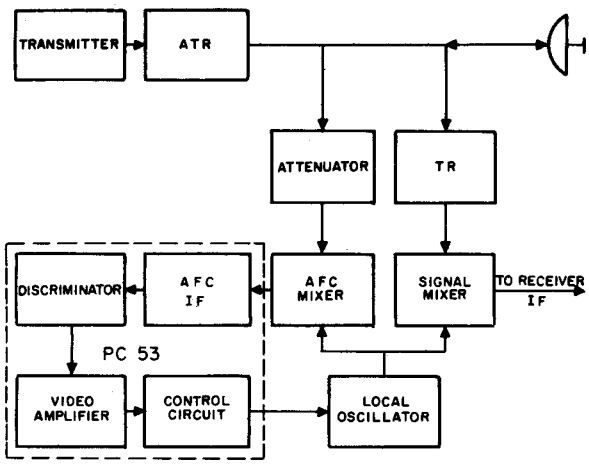


Figure 53–1.—Location of PC 53 in a typical radar system

(*a*) Input coupling network: The choice of input coupling network is left to the user since the design will depend on the crystal and mixer selected, and to some extent on the capacitance of the cable between the mixer and the afc chassis. The bandwidth of the input circuit is not governed by noise or sensitivity considerations, and should be made sufficiently wide so that the over-all bandwidth will not change appreciably with variations in circuit parameters caused by changing crystals.

(*b*) Input level: The signal level at the input to the first IF stage depends on the characteristics of the mixer and the input coupling network. It can be varied over a limited range by adjustment of the transmitter sample and local oscillator power, but these adjustments also affect the harmonic output of the mixer. The survey of recently designed equipment (see Notes to the Preferred Circuits Manual, section 13) and the literature indicate that the signal level at the IF input is usually between 50 and 500 mv. PC 53 is designed for a 200-mv signal level. If system considerations dictate a different input level within the 50- to 500-mv range, PC 53 must be modified, as indicated by Table 53–1 and section 2.2.

(*c*) Harmonics: The harmonics found in the mixer output tend to produce locking when the difference frequency is a submultiple of the

intermediate frequency.[2] (The afc circuit responds to the second, third, fourth, etc., harmonic of the difference frequency.) As noted, the harmonic content of the mixer output can be varied, but the adjustment is not independent of signal level. A maximum harmonic ratio, the ratio of the second harmonic to fundamental component of crystal output voltage, of −26 db is specified to assure proper performance of PC 53 over the range of conditions under which it must operate.

The amplification of PC 53 is adjusted to raise the minimum input signal to a level which will cut off the phantastron completely under minimum performance conditions. This is five times the amplification required to cut off the phantastron for the combination of pulse width, prf, tube condition, and supply voltage which gives maximum performance, and it is approximately ten times the amplification required to raise the signal to a level which will just arrest the sweeping of the phantastron under maximum performance conditions. Since harmonics will cause improper operation of the afc circuit if they develop sufficient bias to stop the sweeping of the phantastron, the −26 db harmonic ratio at the mixer output is reduced to a factor of two at the phantastron grid.

This margin can be increased by operating the local oscillator at a higher frequency than the transmitter. About 80% of the phantastron grid voltage appears as bias across the search stopper diode, V7. This bias must be overcome by the signal before the diode conducts and allows the phantastron bias to build up sufficiently to arrest the sweeping action. The voltage across the diode is twice as large at the beginning of the sweep as at the end, since it is proportional to the phantastron grid voltage (fig. 53–2, p. 53-10). Therefore the circuit tends to discriminate against small signals that occur near the beginning of the sweep.

Crystal harmonics are produced when the separation between the local oscillator and transmitter frequencies is less than the 30-mc IF. When the local oscillator is set to operate at a higher frequency than the transmitter, the difference frequency increases during the phantastron sweep. Harmonics, if any, are produced near the beginning of the sweep where the discrimination against small signals is most favorable. When the local oscillator frequency is set lower than that of the transmitter, the difference frequency decreases during the sweep, and harmonics are produced near the end of the sweep where they are more likely to cause locking. The fact that the correct difference frequency is encountered earlier in the sweep than are the harmonics does not assure proper locking, since, for instance, momentary interruptions of the transmitter signal might cause the local oscillator frequency to sweep from the correct operating point through the harmonics before returning to the correct operating point.

2.2 *Amplification:* The amplification of PC 53 from input to search stopper is fixed by the harmonic ratio. For the 200-mv input level specified, the component values given for the preferred circuit (see pp. 53–2 and 53–3) result in an amplification which is sufficient to minimize the possibility of locking improperly on harmonics and to assure control of the local oscillator under minimum performance conditions.

Since the search stopper output is fixed by the phantastron bias requirements, the amplification required in PC 53 is inversely proportional to the signal level at the input. The eleven levels indicated in table 53–1 are sufficient to cover the range between 50 and 500 mv. For signal levels within ±10% of these inputs, satisfactory performance will be obtained using the resistor values given in the table. If the input signal level lies between two of the levels, either adjacent level may be chosen. Selection of the load resistors associated with the lower level will result in a smaller operating error at the expense of some loss in harmonic rejection. The reverse is true if the higher input level is chosen.

Most of the change in amplification can be obtained by selection of the video amplifier plate load resistance. At the extreme input levels, however, a change in IF amplification is required as well. Change of the IF amplifier loading is permissible to a limited extent because the bandwidth requirements are not rigid.

[2] Ibid, pp. 298–299, 314–315.

TABLE 53-1. *Modifications required for input levels between 50 and 500 mv.*

Input signal level (millivolts)	R3 (ohms)	R10 (ohms)
60	2.7K	33K
75	2.7K	22K
90	2.2K	22K
110	2.2K	15K
135	2.2K	10K
165	2.2K	6.8K
200	2.2K	4.7K
250	2.2K	3.3K
300	2.2K	2.2K
370	1.5K	2.7K
455	1.5K	2.2K

The 60 and 75 millivolt inputs are not recommended for pulse widths less than 0.75 μsec. The load resistor values are correct for any input within 10% of the level indicated.

Input levels below 90 mv are not recommended since the gain-bandwidth requirements cannot be fully satisfied at these levels.

2.3 *IF Amplifier:* The bandwidth of afc IF amplifiers is usually made 3 to 4 times the reciprocal of the pulse width. While this is one and one-half to two times the discriminator peak separation, the extra bandwidth is desirable because it permits slight re-adjustment of the crossover frequency without retuning the amplifier.

The 6- to 8-mc bandwidth is required for the one-half microsecond pulse. The total tube capacitance across the plate of the first IF amplifier is between 6 and 8 μμf. An additional 5-μμf stray capacitance was assumed in determining the inductance required for tuning and in fixing the maximum load resistor value at 2.7KΩ. The inductance must be variable through a range of about ±10%to accommodate the range of 5654/6AK5W capacitances permitted by MIL-E-1/4A. The load for the first stage is provided by the grid resistor of the following stage.

The coupling between the second IF stage and the discriminator is a capacitively-coupled, double-tuned circuit. The equivalent load coupled into the IF amplifier plate circuit is about 5.6KΩ in parallel with 7 μμf. This capacitance, together with strays and the output capacitance of the 5654/6AK5W, raises the capacitance of the IF plate circuit to about 15 μμf, requiring an inductance of 1.8 μh. A tuning range of ±20% is recommended. No additional loading in the IF plate circuit is required to increase the bandwidth beyond the 2 mc obtained with the reflected resistance.

For most inputs, sufficient IF amplification is obtained using a 2.2KΩ resistor as the grid return for the ~~first~~ second IF stage. For the 60 and 75 mv inputs, however, the IF amplification must be raised by increasing this resistance, R3, to 2.7KΩ. This reduces the bandwidth to a point where satisfactory operation cannot be obtained at pulse widths less than 0.75 μsec if the tube capacitances are near the maximum permitted by MIL-E-1/4A. On the other hand, the two highest inputs, 370 and 455 mv, require more reduction in amplification than can be conveniently obtained in the video amplifier alone. In these cases, part of the reduction in amplification is obtained by decreasing the amplification of the first IF stage. The increase in bandwidth when R3 is reduced to 1.5KΩ presents no problem.

2.4 *Discriminator:* The discriminator peak separation is twice the reciprocal of the minimum pulse width so that a good average of the energy in the principal lobe of the pulse spectrum can be obtained. The required bandwidth is easily realized with standard components using the Weiss circuit.

(*a*) Coupling capacitors: The 4-mc peak separation is determined by the coupling capacitances, C6 and C7. These in turn are a function of the plate-cathode capacitance of the diode and of stray capacitance between the discriminator inductance, L3, and ground.[3] The distributed capacitance of L3 has negligible effect. The 10 and 15 μμf capacitors are correct for a diode capacitance of 3 μμf and 5 μμf of strays. If the circuit capacitances are lower, C6 may be increased to 22 μμf, or even to 27 μμf, to obtain gross adjustment of the peak separation. No reduction of C6 will ordinarily be required unless the diode plus stray capacitance is considerably greater than 8 μμf. Since exact adjustment of the peak separation is unnecessary, no trimmer capacitor is used.

[3] Ibid., pp. 308-312.

(*b*) Inductance: The discriminator inductance must resonate at 30 mc with the circuit capacitance, which includes the two coupling capacitors in series, the distributed capacitance of the coil, and the output capacitance of the circuit. The latter includes the diode capacitances, the capacitance of the video network, and the input capacitance of the video amplifier. The capacitance coupled in by the plate circuit of the IF amplifier is negligible. The total capacitance of the circuit, exclusive of strays, is about 7.5 $\mu\mu$f. Since the strays add about 2.5 $\mu\mu$f, the total circuit capacitance is 10 $\mu\mu$f. Inductor L3 should be variable from 2.2 to 2.4 μh to permit adjustment of the crossover frequency.

(*c*) Linearity: For a fixed peak separation, the linearity of the discriminator characteristic in the vicinity of crossover is a function of the bandwidth of the tuned circuits.[4] The 1.7-mc bandwidth obtained with a 9.4KΩ shunt resistance results in a discriminator output at any frequency within the middle 90% of the peak separation whose amplitude departs less than 15% of the peak amplitude from the tangent to the output characteristic at crossover. Better linearity could be obtained using a lower Q but at the expense of output amplitude.

(*d*) Video output: The video output signal is developed across the RC network which constitutes the load of the discriminator diodes. The energy of the IF pulse is stored in the circuit capacitances during the pulse and discharged through the load resistors at its termination. Pulse stretching improves the search stopper operation and can be accomplished without deterioration of the rise time because the leading and trailing edges can be controlled almost independently by adjustment of the load capacitance and resistance respectively.

The load network must also furnish IF bypassing for the ungrounded diode, V3. The effectiveness of the bypassing is limited by the small load capacitance required for good video response and by the lack of direct bypassing of the lower diode load resistor, R9.

To maintain balance, the video response of each of the diode circuits must be equal at every instant during the pulse. Video unbalance results in incomplete cancellation of the video signal at crossover. During the leading edge of the pulse, a spike appears whose polarity is determined by the circuit with the shorter time constant, since the output voltage of this circuit rises more rapidly than the opposing voltage of the other circuit. During the trailing edge of the pulse, the overshoot is of the polarity of the circuit with the longer time constant, since its output decreases more slowly.[5] The amplitudes of these unwanted outputs vary with the pulse width so that video unbalance causes the frequency at which the phantastron locks to vary with change in pulse width.

During the formation of the pulse, the diode load resistors have little effect because they are shunted by the conducting diodes, and video balance is maintained by proper selection of the value of the load capacitors. Since capacitance across the diode load slows the pulse rise, it is added only to the circuit with the shorter time constant.

At the termination of the IF pulse, both diodes become non-conducting. The coupling capacitors discharge through resistor R9, while the 47 $\mu\mu$f capacitor, C8, discharges through resistor R8. These two resistors are made unequal to preserve the video balance as much as possible during the trailing edge of the pulse.

(*e*) Output polarity: When wired as indicated in the circuit diagram, the discriminator output will be positive when the input frequency is less than 30 mc and negative when it is greater. This produces correct locking when the local-oscillator frequency is 30 mc higher than that of the transmitter. (See Notes to the Preferred Circuits Manual, section 13.3 (b).) If the polarity of the discriminator output must be reversed because of system considerations, the diodes should be reversed, since less change in the circuit capacitance results. Interchanging the coupling capacitors will also reverse the output polarity, but this requires changes in the video network to maintain video balance.

[4] Lawrence Baker Arguimbau, *Vacuum Tube Circuits*, John Wiley and Sons, Inc., New York, N. Y., 1948, pp. 486–494.

[5] Pound and Durand, *op. cit.*, pp. 305–307.

2.5 *Video Amplifier:* The error signal produced by the discriminator is a series of pulses whose amplitude depends on the frequency of the IF input and whose polarity may be either positive or negative depending on whether the input frequency is lower or higher than 30 mc. The positive pulses are not used. The negative pulses must be amplified before they can be used to develop the bias required to control the phantastron. The search stopper which follows the video amplifier requires a low-impedance signal source for best performance. The 5670 used as a video amplifier and cathode follower provides both the amplification and the low-impedance output required. Amplifications between 3.5 and 15 can be obtained by selection of the video-amplifier load resistor, R10.

2.6 *Search Stopper:* The search stopper integrates the video pulses to obtain bias to control the phantastron. Although a single diode would be sufficient, both halves of the 5726/6AL5W are used.

When the output of the cathode follower is positive, the capacitor in the search-stopper circuit charges through the diode and the output impedance of the cathode follower. When the cathode-follower output is negative, the diode is non-conducting and little energy is transferred to the capacitor since the resistance of the circuit is high. In the interval between pulses, the capacitor C11 discharges through a part of the grid resistance of the phantastron. The dc level obtained is a function of the charge and discharge times and therefore depends on the duty factor. This dependance can be reduced by minimizing the resistance of the charging path and maximizing the resistance of the discharge circuit.

As a result of the alternate charging and discharging, the signal across the diode load resistor is a sawtooth. (See fig. 53–3 (b). In this figure, the exaggeration of the time scale to show the pulse obscures the fact that the waveform is actually a sawtooth with a positive spike at the leading edge.) Capacitance C11 determines the amplitude of this sawtooth, but has little effect on the dc level because it affects both the charge and discharge time constants in the same way.

2.7 *Phantastron:*[6] During search the phantastron acts as a sawtooth generator to provide a sweep voltage for the control element of the local oscillator. Once the search stopper builds up sufficient bias to stop the sweeping, the phantastron converts the error information received from the search stopper to a voltage which maintains the local oscillator at a frequency differing from that of the transmitter by approximately 30 mc.

(*a*) Operation during search: The use of capacitive coupling between screen and suppressor

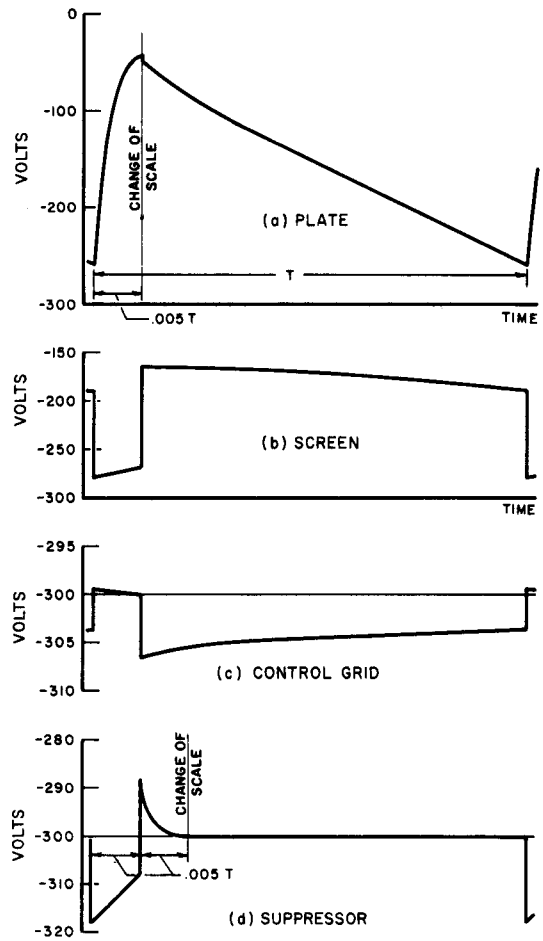


Figure 53–2.—Phantastron sweep generator waveforms

[6] This circuit is called both a phantastron and a transitron in the literature. Phantastron is used heae because it is the more descriptive of the two names. The phantastron has been defined as "the transitron Miller time base." (O. S. Puckle, *Time Bases*, John Wiley and Sons, Inc. New York, N. Y., 1951, p. 172.)

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results in astable operation of the phantastron unless external bias is supplied. The waveforms for this mode of operation, which is used when the local oscillator is searching for the correct difference frequency, are shown in figure 53–2. The sweep period depends on the size of the two coupling capacitors, C12 and C13. The relative durations of the sweep and recovery portions of the cycle and the voltage levels, however, are dependent only on the ratio of these two capacitances. Note that the time scale is greatly expanded during recovery to show the waveform in more detail. Viewed on an oscilloscope, the plate waveform has the appearance of a conventional sawtooth.

(*b*) Operation when locked on: When the afc circuit is locked at the correct local oscillator frequency, the phantastron operates as a dc amplifier with an amplification of about 100. The sawtooth output of the search stopper is smoothed to an almost constant voltage at the phantastron grid (fig. 53–3c). As the corresponding plate waveform indicates (fig. 53–3d), the grid voltage is not absolutely constant but contains a ripple component. The amplitude of the ripple varies as the afc circuit adjusts to changes in the difference frequency or in the prf.

(c) Manual operation: The manual position of switch SW1 is provided to facilitate adjustment of the klystron repeller voltage. In this position the phantastron is inoperative and its plate voltage is fixed at its midrange value. When the klystron output and frequency are optimized under these conditions, afc lock-on near the center of the phantastron range is assured. With SW1 in this position, the range set control may also be used as a manual tuning adjustment. Phantastron operation is stopped by adding resistance in series with the cathode to maintain the cathode near the −300 volt filament potential even when the phantastron is temporarily inoperative.

(*d*) Sweep amplitude: The phantastron, when free running, generates a sawtooth with an amplitude of 220 volts and an average level of about −140 volts using a bogey tube, and an amplitude of 180 volts at about the same dc level when the tube has reached its end-of-life performance limits. This is usually much greater than the amplitude of the sweep voltage required at the klystron repeller. The divider R23, R24 connected across the output of the phantastron is used to reduce the phantastron plate voltage change to a level just sufficient to cover the electronic tuning range of the local oscillator to minimize the possibility of locking on the wrong sideband.[7] The voltage to which this divider is returned is made adjustable by means of the range set control to accommodate differences among klystrons of the same type.

(*e*) Selection of resistance values for output and range set dividers, R23, R24, R25, R26, and R27: Before the values for the resistors in the output and range set dividers can be chosen, the following information must be known about the tube that is to be used as the local oscillator:

(1) The magnitude of the voltage that must be applied to the klystron repeller to sweep its frequency through the desired electronic tuning range. This voltage varies with the type of klystron, and for a given type, with the frequency and mode of operation as well. When

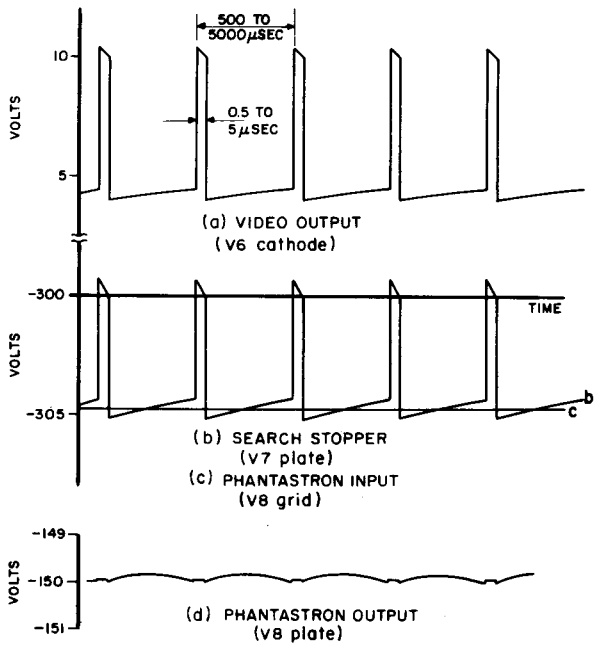


Figure 53–3.—Control circuit waveforms during lock-on

[7] S. N. Van Voorhis, ed., *Microwave Receivers, Rad. Lab. Series*, vol. 23, McGraw Hill, New York, N. Y., 1948, p. 52.

the amplitude of this voltage is known, values can be chosen for the output divider resistors, R23 and R24, to reduce the sawtooth output of the phantastron to the amplitude required by the klystron repeller.

(2) The voltage that must be applied to the klystron repeller to obtain maximum power output for the frequency and mode of operation desired. For a given resonator voltage and the correct klystron cavity tuning, this voltage varies 20 to 25% among tubes of the same type. The extremes of this range are specified by the "reflector voltage" test of the klystron specification. (See MIL–E–1, par. 4.10.5.4. and the individual specification sheet for the type of klystron desired.) When this range is known, the voltage limits of the range set potentiometer and the resistor values for the range set divider can be determined.

To avoid excessive changes in the sweep amplitude with changes in the setting of the range set control, the resistance of the range set divider should be kept small compared to the resistance of the output divider. Since the total resistance of the output divider, R23 plus R24, is between 2.5 and 4.0 megohms, the total resistance in the range set divider, R25, R26, and R27, should be approximately 250K to 400K ohms. A convenient rule of thumb for obtaining values for the range set divider is to assume a divider current of approximately 1 ma.

A nomogram, such as figure 53–4, is the most convenient way to determine the voltage limits of the range set control when one knows the midpoint of the phantastron plate swing, the voltage sweep required to sweep the klystron frequency over the desired electronic tuning range, and the limits of the klystron repeller voltage required for maximum klystron output. If the klystron repeller requires a sweep amplitude of 20, 40, 60, 80, or 100 volts, figure 53–4 can be used directly; if other sweep amplitudes are desired, it must be modified as indicated below.

At the left of the nomogram, the phantastron plate voltage swing is indicated on line A for both the bogey tube (−30 to −250 volts) and the end-of-life tube (−50 to −230 volts). On the right, line C, is the total voltage available

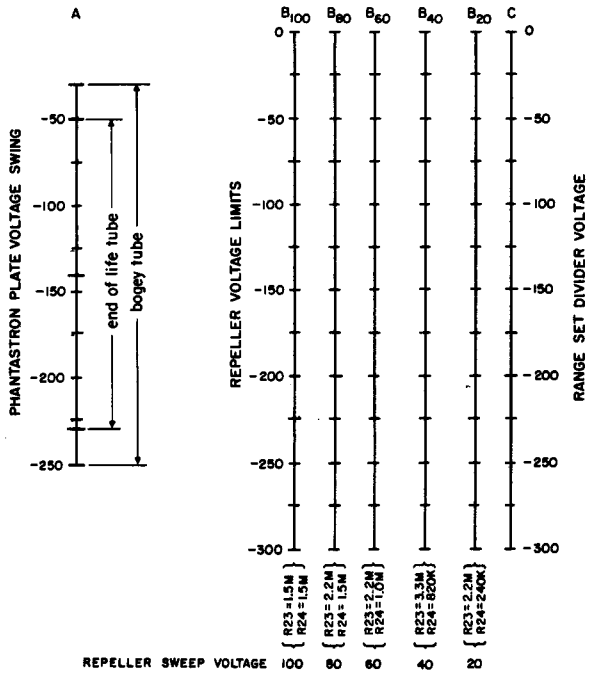


Figure 53–4.—Nomogram for calculating resistor values in the output and range set dividers

in the range set divider, R25, R26, and R27. Both of these are fixed by the circuit constants of PC 53. Actually, only the midpoint of the phantastron plate swing (−140 volts) is of interest in determining values for the range set divider.

The horizontal distance between lines A and C is divided in proportion to the ratio of the resistances used in the output divider, R23 and R24. This has been done in figure 53–4 for resistor values which will give sweep amplitudes between 20 and 100 volts in 20-volt steps. These values have been computed using a phantastron plate voltage swing of 200 volts which is the mean of the values obtained with a bogey and an end-of-life tube. Under these conditions the amplitude of the sweep at the repeller is 10% high using a bogey 5725/6AS6W, and 10% low when tube performance has fallen to its end-of-life conditions. If this is not satisfactory, or if the sweep amplitude required is not one of those given, other values for the output divider resistors are easily calculated. The ratio of the resistance of R24 to the total resistance of the divider, R23 plus

R24, should be in the same ratio as the amplitudes of the klystron repeller swing and the phantastron plate swing, respectively. Having calculated the values of the two resistors, divide the horizontal distance from left to right in proportion to the resistances of R23 and R24.

The limits of the klystron repeller voltage specified in MIL–E–1 can now be plotted directly on the vertical line that represents the klystron repeller swing. If the maximum klystron output is desired at the center of the phantastron plate swing, which is usually the case, lines are drawn from the center of the phantastron plate swing (−140 volts) to each of these two points and extended to intersect the line representing the total range set divider voltage. The two points of intersection represent the voltage limits of the range set potentiometer, R26. The values of R25, R26, and R27 are easily determined by assuming the divider current to be 1 ma. The voltage range of the potentiometer should be increased 10 to 25% to allow for the assumptions made in the nomogram and the tolerances of the divider resistors.

Since the nomogram is based on no-load conditions, the currents drawn from the dividers will result in true voltages which are slightly different from those obtained from the nomogram. The maximum error introduced is less than 10%, provided: (1) The range set divider current is at least 1 ma (in some cases the resistance of the potentiometer must be changed); (2) the output divider has a total resistance of at least 2.5MΩ; and (3) the maximum total repeller current (MIL–E–1, par. 4.10.6.7.1) represents an effective resistance to ground of at least 5MΩ.

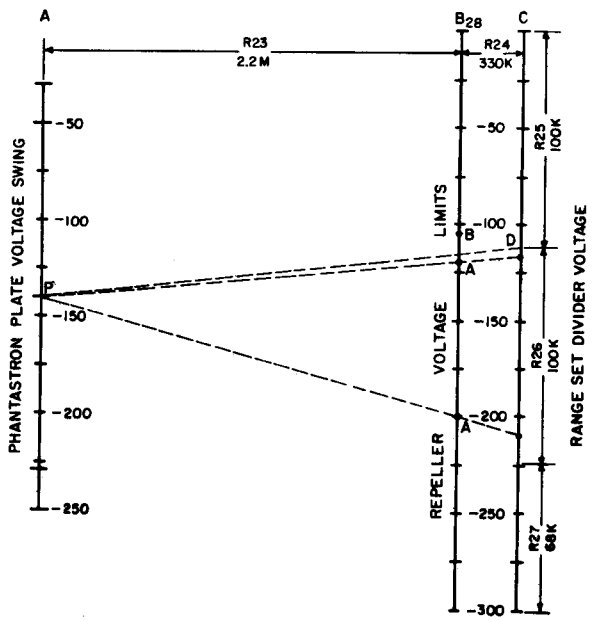


Figure 53–5.—Example of the use of a nomogram to determine the output and range set divider resistors for a klystron type 2K22

For an example of the use of figure 53–4, assume that the local oscillator is to be a klystron type 2K22 operating in mode A at a frequency of 4600 mc. Technical data for this tube indicates that for this frequency and mode the electronic tuning range is 34 mc and requires a repeller change of 28 volts. Maximum output is obtained at repeller voltages between −120 and− 200 volts; at 4600 mc the maximum negative voltage at which mode B can be obtained is −105 volts.[8]

The output divider for a 28-volt repeller swing must first be determined, since it is not shown in figure 53–4. The ratio of the repeller to phantastron plate swing is 28/200= 0.14. Values of 2.2MΩ and 330KΩ for R23 and R24 have a ratio of R24/(R23+R24)=0.13, which is close enough. The horizontal distance on the nomogram is now divided in the ratio of R23 and R24, as indicated by line B in figure 53–5. In practice this could be done on the original nomogram, figure 53–4, but is done here on a separate figure for clarity. The limits of the klystron repeller voltage at which maximum power output is obtained can now be plotted on line B at −120 and −200 volts. For reference the maximum mode B voltage, −105 volts, is also plotted.

Since it is desired that maximum output occur at the center of the phantastron sweep, lines are drawn from this point, P, through the points A to intersect the range set divider voltage line, C, at −118 and −204 volts. These are the voltages required at the ends of the range set

[8] JAN–1A, JAN–2K22, 8 Aug. 1945. Technical Data for Armed Services Preferred List of Electron Tubes, 2K22, June 1956.

potentiometer, R26. Assuming a 100KΩ potentiometer and a divider current of 1 ma, values of 100KΩ for R25 and 68KΩ for R27 are approximately correct. These values actually give a range set voltage which is variable from −112 to −224. The increase allows for nomogram and resistor tolerances and does not permit adjustment on mode B, since line PD does not enclose point B.

(*f*) Sweep rate: The time required for the rundown of the phantastron is determined by the grid circuit time constant, and can be varied by changing either the grid resistance or the feedback capacitance. Since the grid resistance is also a part of the search stopper circuit, the feedback capacitor is used to set the sweep rate.

The feedback capacitance can be determined from the rate of change of plate voltage, which is [9]

$$\frac{dV_p}{dt}=\frac{V_g}{R_gC_g}\frac{A}{1+A}$$

$$\approx\frac{V_g}{R_gC_g}$$

since the circuit gain, A, is much greater than 1.

Substituting the values for mean grid voltage, V_g, change in plate voltage during rundown, ΔV_p, and grid circuit time constant, R_gC_g, we obtain:

$$\frac{1}{\Delta t}=f_s\approx\frac{4.7}{220\times5.7C_g\times10^{-6}}$$

$$C_g=\text{C12}\approx\frac{3750}{|f_s|}\quad\mu\mu\text{f}$$

where f_s is the phantastron sweep frequency.

Since each cycle of the phantastron output sweeps the local oscillator through its electronic tuning range, the local oscillator search rate is easily related to the phantastron sweep frequency.

$$R_s=f_s\,(etr)\qquad\text{mc/sec/sec}$$

$$|\text{C12}|=\frac{3750\,(etr)}{R_s}\qquad\mu\mu\text{f}$$

where R_s is the local oscillator search rate in mc/sec/sec and etr is the electronic tuning range of the klystron in mc.

[9] Pound and Durand, *op. cit.*, pp. 326–331.

The maximum permissible search rate is fixed by the lock-on requirements. To assure lock-on, two successive video pulses from the cathode follower must be of sufficient amplitude to overcome the search stopper bias and cause diode V7 to conduct. Even under minimum performance conditions the input to the search stopper exceeds the maximum diode bias for at least 1 megacycle of the negative discriminator peak. The maximum search rate consistent with satisfactory locking is

$$R_{s\,max}=\frac{\Delta f}{\Delta t}=\frac{1\text{ mc}}{2\left(\frac{1}{prf}\right)}$$

$$=0.5\,prf\qquad\text{mc/sec}^2$$

The maximum search rate consistent with the lock-on requirements should be used, since the search rate is the maximum rate at which the local oscillator can increase its frequency to follow changes in difference frequency. Since neither the rate of change of phantastron plate voltage nor the electronic tuning sensitivity of the klystron is constant during the sweep, the maximum values should be used in determining the maximum search rate.

(*g*) Sweep linearity: The rate of change of plate voltage is proportional to the grid voltage and therefore changes by a factor of almost 2 to 1 during rundown. Based on the average rate of change, this is a change of ±30%, being maximum at the beginning of the sweep and minimum at the end. This does not include the almost instantaneous drop in plate voltage at the instant the rundown begins.

(*h*) Sweep recovery: The capacitive coupling between screen and suppressor is responsible for the free-running properties of the phantastron. As in the conventional phantastron, at the conclusion of the rundown a fraction of the drop in screen voltage is coupled to the suppressor to cut off plate current flow. Since the coupling is capacitive, however, the suppressor bias is gradually lost and the rundown is repeated as soon as the exponential voltage at the suppressor grid has dropped below the bias required for plate current cutoff.

The rate of decay of suppressor bias is determined by the coupling capacitance, C13, and

the suppressor return, R18. One-half of the time constant R18, C13 is required for the suppressor bias to fall to a level which will allow phantastron plate current to flow. During this time the plate circuit of the phantastron must recover. Since the rate of plate voltage recovery is determined by C12 and the phantastron plate load resistor, R16, the values of C12 and C13 can be related. With equal values for C12 and C13, the recovery time is less than 0.5% of the length of the sweep, and the phantastron plate voltage recovers to within 10% of its supply voltage.

The tap on the screen divider couples about one-sixth of the screen voltage change to the suppressor. If more than one-sixth of the screen voltage change is used, the rundown terminates prematurely. If the fraction is made smaller than one-sixth, the time during which the plate current is cut off will not be sufficient to allow the plate voltage to recover completely. In either case the amplitude of the output is reduced.

3. ADJUSTMENTS

Four adjustable components are required to compensate for variations in tube characteristics permitted by MIL–E–1. These components are discussed below.

3.1 *IF Amplifier Tuning:* Permeability tuned coils that center the response of the IF amplifiers at 30 mc are specified. The response of the first IF amplifier is a single peak centered at 30 mc. When the discriminator circuit is coupled to the second IF amplifier, the response is the double-humped curve characteristic of overcoupled, double-tuned circuits. In PC 53, the dip occurs at 30 mc and the peaks occur at approximately one-half the discriminator peak separation above and below 30 mc.

3.2 *Discriminator Tuning:* The variable inductance, L3, of the discriminator circuit is used to adjust the crossover to 30 mc. Over a small range, the entire discriminator curve is shifted without alteration of its shape. If more than one pulse width is used, the change in crossover frequency with change in pulse width is minimized by adjusting crossover using the widest pulse. With the tuned circuits all peaked at 30 mc, the discriminator peaks will not be of equal amplitude because of the difference in the coupling capacitors.[10] They may be equalized by detuning L2 slightly.

3.3 *Range Set Control:* The range set control in conjunction with the manual-afc switch, SW1, is used to adjust the local oscillator to the correct difference frequency when the phantastron is at the center of its sweep. When SW1 is in the manual position, the sweeping of the phantastron is arrested and its output is fixed at approximately the mid-voltage of the sweep. The local oscillator output and frequency can then be adjusted for the correct difference frequency by means of the resonator cavity and the range set potentiometer, which is the repeller voltage control. When SW1 is returned to the afc position, the operating point will be fixed at the center of the phantastron sweep where the afc circuit can effectively compensate for changes in difference frequency in either direction. If this operating point does not coincide exactly with the correct difference frequency, small corrections can be made by adjusting the crossover frequency.

4. PERFORMANCE

Preferred Circuit 53 has been designed to minimize the effects of supply voltage changes and tube aging. With well-regulated plate supplies, it will perform satisfactorily with the filament supply voltages 10% low and with half of the tubes at their end-of-life limits.

4.1 *Static Performance:* Typical transfer characteristics are shown in figure 53–6. These curves were obtained statically and give no indication of the rate at which the system will follow changes in input frequency. They are of use, however, in estimating the operating error and gain of the circuit and in illustrating the effect of pulse width and duty factor. Although the curves were obtained using the circuit specified for a 200 mv input level, they are typical of the performance at any of the other inputs, provided the corresponding component values listed in table 53–1 are chosen.

[10] Ibid, p. 311.

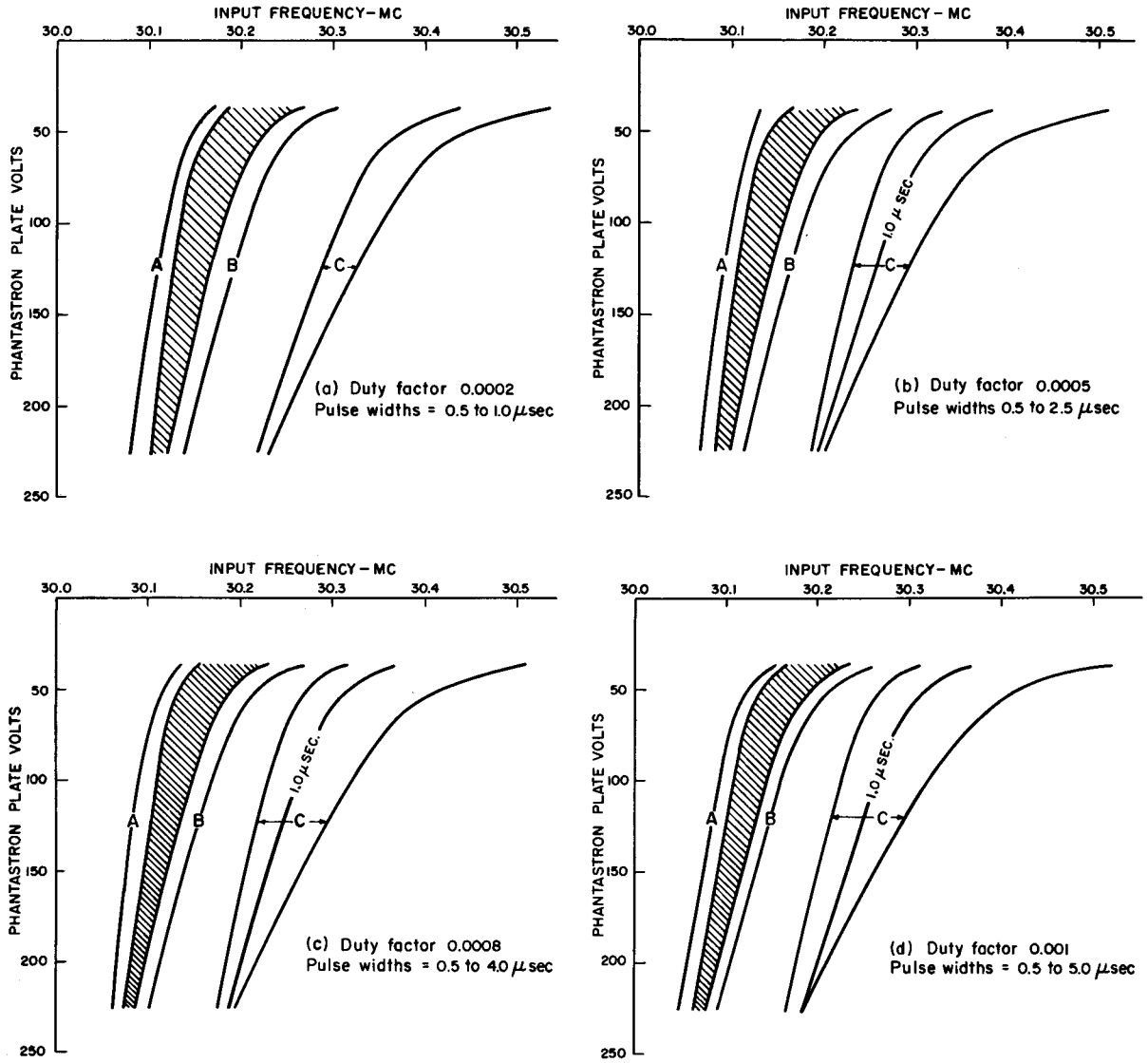


Figure 53–6.—Static performance of PC 53

The crosshatched areas indicate normal performance obtained using the nominal input signal level, rated supply voltages, and bogey tubes. Variations within this region are caused by the fact that the circuit gain is proportional to the pulse width. At each duty factor all the measurements were made with the crossover frequency set to 30 mc using the widest pulse.

For each set of curves, the letters A, B, and C indicate:

- *A. Maximum change in performance caused by raising the input signal level or the filament voltage 10%.*
- *B. Maximum effect of reducing the input signal level 10%.*
- *C. Typical end-of-life performance obtained with half of the tubes at their end-of-life limits and the filament voltage 10% low. The 1.0 μsec curve is plotted to show the extent to which short pulses affect the minimum performance. If the 5725/6AS6W is one of the tubes whose characteristics have reached their end-of-life ratings, the limits of the plate voltage swing will be reduced to —50 and —230 volts.*

The normal curves indicated by the cross-hatched area are for the nominal input, bogey tubes as defined in MIL–E–1, and rated supply voltages. As indicated by curves A and B adjacent to this area, inputs within 10% of the input level specified have a negligible effect on performance. The minimum performance curves shown in region C were taken with the filament voltage 10% low and with half of the tubes at their end-of-life limits as defined by MIL–E–1.

The amplification of PC 53 is proportional to both the pulse width and the duty factor of the signal input because the discriminator "gain" is a function of the former, and search stopper "gain" is a function of both. Of the two, the effects of pulse width are more pronounced, as shown in the curves, and must be taken into consideration because several pulse widths may be used in a single microwave system, whereas the duty factor will remain approximately constant. In figure 53–6, an increase in amplification is indicated by an increase in the slope of the curve and a shift of the entire curve toward the crossover frequency. Curves are given for several duty factors so that the performance can be estimated at any pulse width and duty factor combination within the specified range. At each duty factor the discriminator was adjusted for crossover at the maximum pulse width, since in actual systems one crossover adjustment must serve for all the pulse widths used.

If the local oscillator frequency is lower than that of the transmitter, PC 53 will operate a few tenths of a megacycle lower than 30 mc rather than above, as shown in figure 53–6. In this case the static performance curves are the mirror images of those shown.

4.2 *Frequency Correction:* The amount by which a relative change between the transmitter and local oscillator frequencies is reduced can be estimated from the slope of the static performance curves (fig. 53–6) and the characteristics of the local oscillator.

The slope of the straight portion of the static performance curves is between 2000 and 3500 volts per megacycle under normal performance conditions and between 1000 and 2000 volts per megacycle when the circuit performance has fallen to its minimum satisfactory level. This represents the rate of change of phantastron plate voltage (ΔV_p) with respect to a change in input frequency (Δf_{in}). The required repeller swing (ΔV_r) and the electronic tuning sensitivity ($K=\Delta f_{LO}/\Delta V_r=etr/\Delta V_r$) can be determined once the type of local oscillator is selected. For a fixed transmitter frequency, the change in local oscillator frequency (Δf_{LO}) is equal in magnitude and sense to the change in input frequency if the local oscillator is operating at a higher frequency than the transmitter.[11] The open loop amplification, A, of the afc system is therefore

$$A=K\frac{\Delta V_p}{\Delta f_{in}}\frac{\Delta V_r}{\Delta V_p}=\left(\frac{\Delta V_p}{\Delta f_{in}}\right)\frac{etr}{\Delta V_p}$$

For PC 53

$A=4.5$ (etr) when the slope is 1000 v/mc.
$=15.9$ (etr) when the slope is 3500 v/mc.

Once the loop amplification has been determined, the amount by which a change in the difference frequency is reduced can be found by dividing the frequency change by the loop amplification plus one.[12] This is essentially a static measurement applying only to slow changes in frequency such as are caused by thermal effects, or to the change in difference frequency after the circuit has reached equilibrium conditions following a transient. The instantaneous error during a sudden shift in frequency, such as is caused by transmitter pulling, is several times this magnitude. As an example, if a 2K22 operating in mode A at a frequency of 4600 mc is used as local oscillator, the electronic tuning range is 34 mc.[13] The minimum loop amplification is 4.5 x 34=153, and a 15 mc change in difference frequency would be reduced to 15 mc/153+1 ≈100 kc by the action of the afc system.

[11] If the local oscillator is operating at a lower frequency than the transmitter, the change in input frequency is equal in magnitude to the change in local oscillator frequency but opposite in sense. In this case the slope of the performance curves is also negative so that the loop amplification is still a positive quantity.

[12] Van Voorhis, *op. cit.*, p. 31.

[13] Technical Data for Armed Services Preferred List of Electron Tubes, 2K22, June 1956.

4.3 *Tube Characteristics:* Tube characteristics affect the over-all amplification of the circuit, and in the case of the IF amplifiers and discriminator, the tuning as well because the tube capacitance is a part of the tuned circuit. It is advisable to adjust the tuning when the IF amplifier tubes are changed, although the frequency change caused by the change in tube capacitance is small. It is essential that the tuning of the discriminator be adjusted when the discriminator tube is changed, since a change in crossover frequency affects the sensitivity of the radar receiver. The tuning of the plate circuit of the second afc IF stage should also be checked in this case.

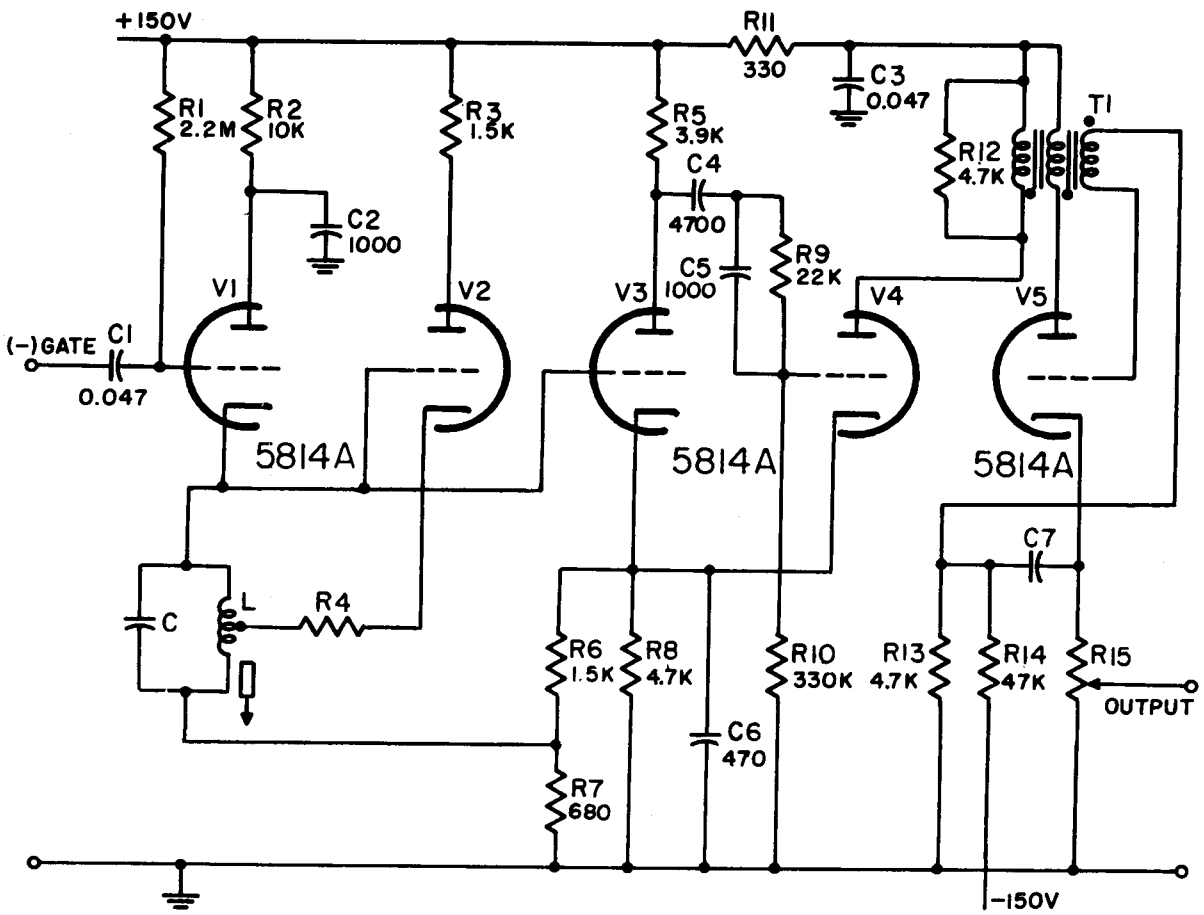
The amplification of PC 53 is unaffected by diodes in the discriminator and search stopper circuits which have reached their end-of-life performance limits. End-of-life tubes will reduce the amplification of any of the other circuits about 25%. The afc circuit will perform satisfactorily when all the tubes have reached their end-of-life limits, provided the supply voltages are maintained at their rated value. Since it is unlikely that the filament supplies will be regulated, the minimum performance curves (fig. 53–6) were run with the maximum number of low tubes that could be tolerated when the filament voltage is 10% low. The data for these curves (region C) were obtained with 5654/6AK5W's which had reached their end-of-life performance limits in both of the IF amplifier sockets. The same results are obtained if the video amplifier and one IF amplifier are the low tubes, or if the transconductances of all of the tubes are the minimum acceptable under MIL specifications. If the 5725/6AS6W is one of the tubes whose performance is reduced to end-of-life conditions, the frequency shift will be accompanied by a 20% reduction in the amplitude of the plate voltage change.

4.4 *Supply Voltages:* Since the afc circuit is sensitive to supply voltage changes, the plate supply voltages should be regulated. (See PC 1 and PC 3A.) Regulation of the principal filament supply (grounded filaments) would be beneficial but is not necessary. A $\pm 10\%$ change in this filament supply was assumed in determining the minimum performance characteristics and the -26 db maximum harmonic ratio.

Performance is not affected by $\pm 10\%$ changes in the 5725/6AS6W filament supply voltage. A 10% increase of the principal filament supply voltage almost doubles the amplification of the afc circuit; a 10% decrease in filament voltage reduces the amplification about 25%. A 10% reduction of the 150-volt supply also reduces the circuit amplification 25%, while a 10% increase in the positive plate voltage has little effect on performance. A change in the -300 volt supply results in an even greater percentage change in the amplitude of the phantastron output, since the plate-cathode voltage at bottoming remains almost constant in spite of supply voltage changes, and the accompanying change in plate voltage at cutoff is negligibly small.

NBS PREFERRED CIRCUIT NO. 55
DISTANCE-MARK GENERATOR

NBS PREFERRED CIRCUIT NO. 55
DISTANCE-MARK GENERATOR



Unless otherwise stated: R in ohms; C > 1 in $\mu\mu$f; C<1 in μf; L in μh

The distance-mark generator is used to generate accurately spaced pulses which are mixed into the video amplifier chain to indicate the range of radar echo pulses.

Distance-mark spacing	1 to 25 miles. [1]
Input Gate Amplitude	60 to 210v, negative. [2]
Input Gate PRF	200 to 2000pps.
Delay (input gate to marker)	0.1 to 0.2μsec.
Marker Amplitude	30v (R15:220Ω). [3]

C7 nominally 1200$\mu\mu$f.

C1,C2,C3,C4,C5,C6,C7: ±10% limits.

All R: ±10% except R2,R11: ±20% limits.

NOTES:

1. L,C and R4 determined by DM spacing selected.
2. Input gate from PC 41 used in tests.
3. For complete characteristics of blocking oscillator see PC 47.

PC 55 DISTANCE-MARK GENERATOR

1. APPLICATION

The distance-mark generator is used to generate accurately spaced pulses which are mixed into the video amplifier chain to indicate the range of radar echo pulses.

2. DESIGN CONSIDERATIONS

2.1 *Operation:* This distance-mark (DM) generator is suitable for medium-precision applications such as for use in search radars. The formation of the markers takes place in three steps. The DM spacing time interval is determined by the frequency of the switched Hartley oscillator V2. The resulting sine-wave is shaped by a monostable multivibrator, V3,V4, and furnishes the trigger for the blocking oscillator. The blocking oscillator, V5, produces the narrow marker pulses. The negative gate which operates the switch tube, V1, corresponds in duration to the selected mileage range, and its PRF depends upon the type of service and range of the radar set.

The interdependent operation of the switch tube, the Hartley oscillator, and the trigger shaper makes desirable the treatment of these circuits together. The blocking oscillator, which receives the output of the generator, is discussed separately in PC 47, Triggered Blocking-Oscillator for Fast Recovery.

The DM is derived from the initial negative swing of the Hartley oscillator and each successive negative-going portion of the sine-wave. For one-mile spacing (12.2μsec), the corresponding oscillator frequency is 81.9kc. Different spacing of the distance marks can be selected by changing the resonant circuit and resistance of R4.[1,2] The range is changed by selecting the duration of the negative gate. In the tests of the DM generator, the negative gate was obtained from PC 41, Main Gate Multivibrator.

3. PERFORMANCE

3.1 *Zero Error:* The "zero error", or time delay of the DM generator is the time difference between the negative gate and the blocking oscillator output measured at the 10% amplitude points. A delay of 0.6μsec corresponds to an error of 100 yards. The delay measured at the plate of the second trigger shaper tube, V4, is about 0.05μsec. The over-all delay is about 0.1μsec which corresponds to about 20 yards. These results are tabulated in table 55–1.

The performance of the generator was measured for distance-mark spacings of 1, 5, and 25 miles at representative mileage ranges. The oscillator sine-wave amplitude is measured when a uniform wave-train is attained by adjusting the feedback resistor, R4. Values for various ranges are given in the table.

3.2 *Tube Substitution Performance:* Thirteen combinations of three tube sets with various transconductance value tubes were operated in the DM generator. Tubes in the MIL transconductance range and tubes above and below the MIL range were selected and placed in sockets V1,V2,V3,V4, and V5. Operation was satisfactory for all combinations with respect to time delay and output amplitude. The oscillator was least affected by tube changes. Most affected by

TABLE 55–1—*Distance-mark Generator Performance*

DM spacing	1-mile		5-mile		25-mile	
Gate PRF pps (50% duty cycle)	200	800	2000	200	800	200
Gate length μsec	2500	625	250	2500	625	2500
Mileage range	200	50	20	200	50	200
Osc. sine-wave amplitude (p-p volts)	65	65	65	90	90	75
Osc. resistor, R4 (Ω)	1.8K	1.8K	1.8K	680	680	680
DM amplitude volts (~~R16~~, 220Ω) R-15	[1]30	30	30	30	30	30
DM delay (μsec)	0.10	0.10	0.10	0.11	0.11	0.11

NOTE 1. After the third pulse; the first and second pulses are greater by 15% and 5%, respectively.

[1] Theodore Soller, ed., *Cathode Ray Tube Displays, Rad. Lab. Series*, vol. 22, McGraw-Hill, 1949, p. 245.
[2] Britton Chance, ed., *Electronic Time Measurements, Rad. Lab. Series*, vol. 20, McGraw-Hill, 1949, p. 108.

changes was the trigger-shaper, V3 and 4, which resulted in increased delay with low transconductance tubes. The blocking oscillator output amplitude decreased about 15% with low tubes compared to tubes within the MIL range.

3.3 *Supply and Filament Voltage Variation:* Operation was satisfactory with respect to delay and DM amplitude for supply-voltage variation of +10%, −25%, and ±10% change in filament voltage. The increase in time delay for a −25% decrease of supply voltage is greatest for the 25-mile spacing and increases about 0.1μsec to an over-all delay of 0.2μsec. There is a 0.02μsec decrease in delay with 10% increase in supply voltage.

Of the eight generators discussed in the Notes, Sec. 8, two of each type were tested. The results are tabulated in table 55–2. The oscillator sine-wave amplitude was measured when adjusted for uniform wave-train. The time delay of the multivibrator shaper is less by a factor of 3 or more than the amplifier-shaper. For comparison a radar range of 100 yards is 0.61μsec in time. The delay of the MV-shaper, circuit A, is 0.25μsec or 41 yards; the delay of the amplifier-shaper, circuit E, is 0.9μsec or 150 yards. On this basis of a shorter delay time for the MV-shaper, the MV was selected for use in the DM generator, PC 55.

The distance-mark amplitudes and polarity differ for various circuits, but this is not important for these comparisons. They can easily be changed with minor modifications in the blocking oscillator.

The function of the various components will be described briefly except for those concerned with the blocking oscillator. The positive grid return of the switch tube serves to keep heavy current conduction through the oscillator coil. The plate resistor limits the current to a value within the tube rating. The bypass capacitor at the plate assures the presence of the initial negative-going sine-wave which otherwise tends to jitter or diminish. The oscillator feed-back resistor value is adjusted for uniform amplitude; otherwise the oscillations increase or decrease. The resistor on the ground side of the LC circuit in the case of the MV-shaper provides a positive bias for the first MV tube to keep it normally conducting. The filter in the form of a resistor-capacitor or a resistor-choke in the plate of the first MV tube is to prevent interference with the waveform of the Hartley oscillator.

The stability of the Hartley oscillator frequency for a ±10% change in supply voltage is better than 3 parts in 10,000, better than 9 parts in 10,000 (increase) for a −25% decrease. The change in frequency with a filament voltage variation (of ±10%) is less than 6 parts in 100,000. The frequency-stability with respect to temperature change depends upon the LC circuit, and is adequate except for precision applications which would require a temperature-controlled oven. [3] This type of generator is suitable for medium-precision paplications and the accuracy can be maintained to better than 1%.

TABLE 55–2—*Summary of Distance-mark Generator Characteristics*

Circuit	Trigger shaper	Delay (μsec)	Type Trigger	Osc. sine-wave amplitude (p-p)	RM amplitude (v)
A	MV	0.25	Parallel third W. [1]	80v	24
D	MV	0.12	Parallel third W. [1]	80v	3.6
E	Amp	0.9	Series	85v	60
H	Amp	3.3	Parallel	48v	−4.2

NOTE 1. Third winding of blocking-oscillator transformer.

3.4 *Use with Pulse-train Divider:* Satisfactory operation of the Blocking Oscillator Pulse-train Divider, PC 51, was obtained with this generator for 1-mile DM spacing and PRF's listed in table 55–1, for division factors of 2, 3, 4, and 5.

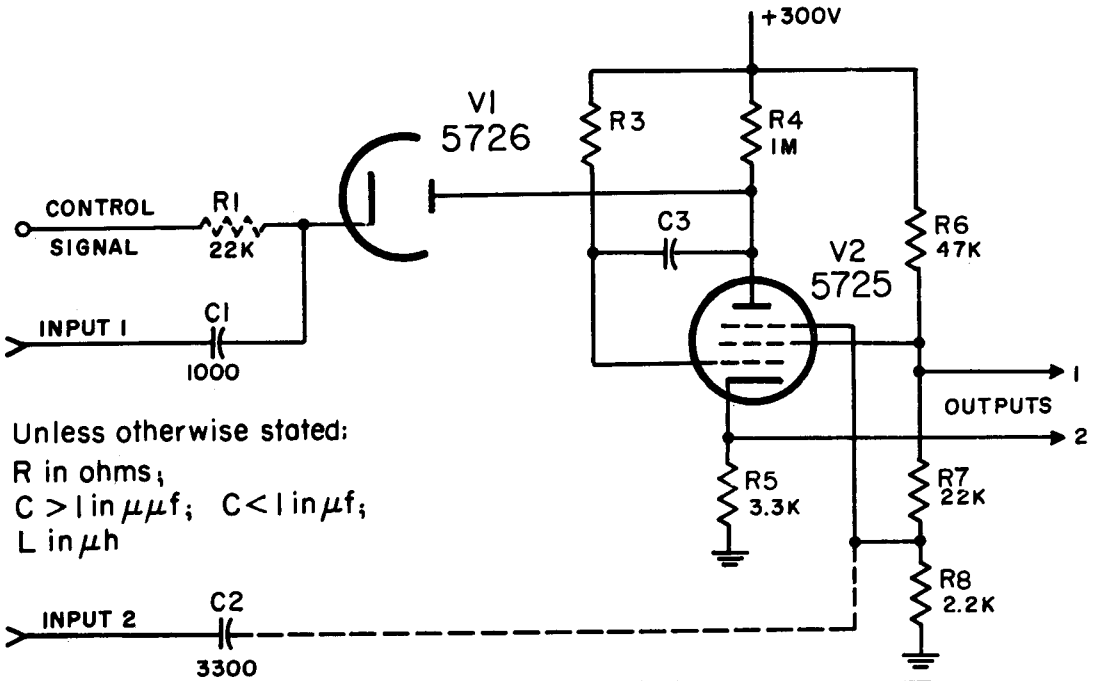
The DM amplitude falloff (change in amplitude from first to last DM) is less than 1% except for the 1-mile spacing, 200pps. For this case the first marker is 15%, and the second 5% greater than the remainder of the train.

In regard to the input gate amplitude, a gate amplitude of 210v is available from the Main Gate Multivibrator, PC 41. The figure of 60v was selected as the lowest for attaining a uniform wave-train from the Hartley oscillator.

[3] Britton Chance, ed., *Waveforms, Rad. Lab. Series*, vol. 19, McGraw-Hill, 1949.

NBS PREFERRED CIRCUIT NO. 56
PHANTASTRON DELAY

NBS PREFERRED CIRCUIT NO. 56
PHANTASTRON DELAY



R3 megohms	C3 μμf	Minimum duration (V_c = 20v) μsec	Maximum duration (V_c = 280v) μsec	Maximum recovery time [1] (V_c = 280v) μsec
1.0	100	7	90	270
1.0	220	15	200	600
1.0	470	30	440	1600
1.0	1000	70	930	2700
2.2	1000	150	2000	2700
2.2	1200	180	2450	3250
3.3	1200	265	3700	3250

Control Signal, V_c: 20v to 280v. [2]
Maximum Error: 0.1 percent of maximum duration. [3]

Terminal		Amplitude v	Rise time μsec	Duration	Decay time	Impedance	Polarity
Input	1	15	0.1	1 to 5μsec	—	—	Negative
	2	20	0.1	0.2 to 2μsec	—	—	Positive
Output	1	60	0.2	—	0.1% [4]	≈20KΩ	Positive
	2	10	0.2	—	0.1% [4]	≈1KΩ	Negative

R3: ±5%; R5,R6,R7,R8: ±10%; R1,R4: ±20% limits. C1,C2: ±20%; C3: ±5% limits. R3,C3: temperature stable.

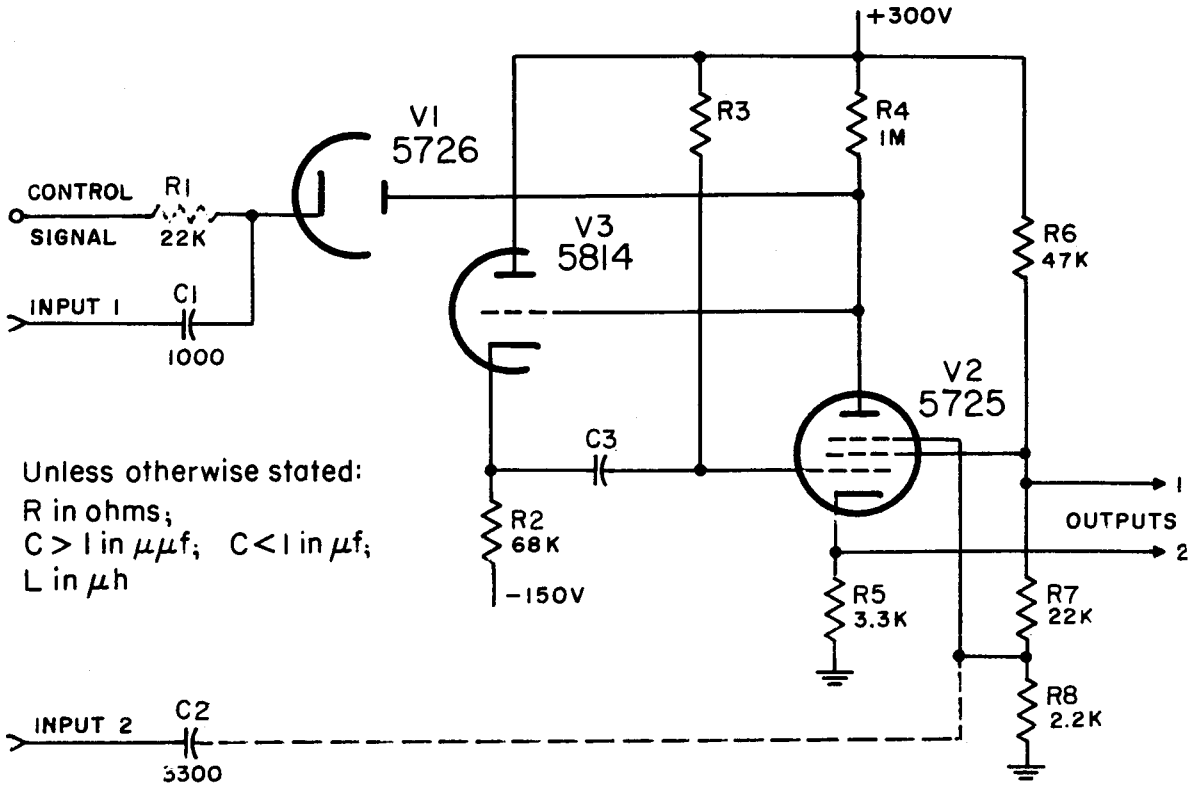
NOTES:

1. If shorter recovery time is required see PC 57.
2. Control signal source must furnish a dc return to ground for V1.
3. Maximum error may be reduced by reducing maximum control voltage (see text and fig. 56–1).
4. In percent of maximum duration.

NBS PREFERRED CIRCUIT NO. 57
PHANTASTRON DELAY, FAST RECOVERY

+300V

NBS PREFERRED CIRCUIT NO. 57
PHANTASTRON DELAY, FAST RECOVERY



Maximum duration	*R3*	*C3*
< 1000μsec	1.0 megohm	100 to 1000μμf
1000 to 5000μsec	3.3 megohm	330 to 2200μμf

Maximum duration $\approx R3C3 \frac{V_c \text{ max.}}{E_{bb}}$

Maximum recovery time ≈ 40μsec.
Control signal, V_c: 20v to 240v. [1]
Maximum error: 0.5 percent of maximum duration. [2]

Terminal		Amplitude v	Rise time μsec	Duration	Decay time	Impedance	Polarity
Input	1	15	0.1	1 to 5μsec	—	—	Negative
	2	20	0.1	0.2 to 2μsec	—	—	Positive
Output	1	60	0.2	—	0.1% [3]	≈20KΩ	Positive
	2	10	0.2	—	0.1% [3]	≈1KΩ	Negative

R3: ±5%; R5,R6,R7,R8: ±10%; R1,R2,R4: ±20% limits. C1,C2: ±20%; C3: ±5% limits.
R3,C3: temperature stable.

NOTES:

1. Control signal source must furnish a dc return to ground for V1.
2. Maximum error may be reduced by reducing maximum control voltage (see text and fig. 56–1).
3. In percent of maximum duration.

PC 56 and 57 PHANTASTRON DELAY

1. APPLICATION

PC 56 and PC 57 are phantastron circuits capable of generating a rectangular waveform whose duration is almost directly proportional to a control signal. Such circuits are frequently used in radar equipment to produce movable markers for display and to time-modulate a pulse in accordance with a variable quantity such as antenna position.

The two circuits are identical except for the inclusion of the cathode follower, V3, in PC 57. The cathode follower decreases the usable range of the control voltage and the linearity but is necessary in order to reduce the recovery time when the duty factor is greater than 30 to 60%. Whether PC 56 or PC 57 is used in a given application is determined entirely by recovery time considerations.

2. DESIGN CONSIDERATIONS

These circuits are cathode coupled phantastrons. The suppressor is returned to the screen divider for economy of parts and power drain; it is operated about 5v positive during rundown to minimize jitter in the trailing edge of the output waveform. The use of a cathode-coupled phantastron increases the amplitude of the initial step in the plate waveform, but permits a low impedance output from the cathode. The increased amplitude of the initial plate drop is not troublesome in this application.

2.1 *Circuit Parameters:* The table in PC 56 gives values for the grid resistance and capacitance, R3 and C3, for frequently used delays. For applications that do not fall within one of these ranges, values for R3 and C3 can be determined from the following relations:

(1) Maximum output duration

$$\approx RC \quad \frac{V_c \text{ max.}}{E_{bb}} \text{ sec.}$$

(2) Maximum recovery time:

(*a*) Without cathode follower

$$\approx RC \ln \frac{E_{bb}}{E_{bb} - V_c \text{ max.}} \text{ sec.}$$

(*b*) With cathode follower $\approx 40\mu$sec

where V_c is the control signal voltage. By substituting the values for control signal and the requisite duration of the waveform, R3,C3 can be determined.

R3 is limited to a minimum value of one megohm to avoid excessive grid current in the tube during quiescent periods. C3 should be at least $100\mu\mu$f to minimize the effects of stray capacitances. Delays shorter than 100μsec require more complex circuits. [1] The maximum values of both R3 and C3 are limited only by the stability of the components.

If several ranges are to be obtained by switching, the most satisfactory arrangement is to leave R3 fixed and switch C3 to obtain the delays desired. A cathode follower will probably be required to minimize the recovery time, but should be used in any case to provide a low impedance point for switching and to minimize the effects of the added stray capacitance.

R4 determines the recovery time of both circuits. In PC 56, C3 is charged by the grid current of the pentode flowing through the plate load resistance, giving a recovery time determined by equation 2 (*a*). Addition of the cathode follower in PC 57 permits C3 to recharge through the low impedance output of the cathode follower, but the plate voltage recovery is still retarded by the output capacity of the tube and other stray capacities. The latter is generally the longer of the two recovery times when a cathode follower is used.

2.2 *Tube Type:* The phantastron requires a pentode with two control grids. The 5725 is the best tube for the purpose because of the sharp cutoff characteristic of the suppressor. The 5725 is a miniature, sharp cutoff pentode whose control and suppressor grids can be used as independent control elements; it is a preferred premium type which is electrically equivalent to the 6AS6. The 5784WA and 5636 are preferred subminiature equivalents.

In these tubes the total space current is determined almost entirely by the voltages on the control and screen grids. It is independent of suppressor bias except near suppressor cutoff, and independent of plate voltage except at very low plate voltages. The division of space current

[1] Britton Chance, ed., *Waveforms, Rad. Lab. Series*, vol. 19, McGraw-Hill, 1949, pp. 200-203.

between plate and screen is predominantly a function of the suppressor bias. The ratio of plate to screen current is constant at positive suppressor voltages, and is nearly independent of control and screen grid voltages.

2.3 *Control Signal:* The duration of the phantastron waveform can be made proportional to any quantity that can be represented by a voltage. When the control voltage is obtained from a potentiometer, the potentiometer should obtain its current from the plate supply of the phantastron to minimize error due to changes in supply voltage. Since the potentiometer loading error is opposite in sense to the phantastron error, partial compensation can be obtained by balancing the two errors against each other. This requires that the sum of the potentiometer resistance and any other resistance between the potentiometer and the plate supply be between one and five percent of the plate load resistance. If the minimum resistance between the potentiometer and ground is greater than 22KΩ, R1 may be omitted. Rheostats in series with both ends of the potentiometer are usually provided to permit setting the reference voltage to the desired range.

In many cases the control signal is a continuously varying voltage proportional to another quantity; for instance, a sine-wave whose amplitude at any instant is proportional to the sine of the angle between a radar antenna and a reference line (ship heading, true north, etc.). If the source impedance is low and plate triggering is used, R1 may be necessary to prevent shorting the trigger to ground.

To permit the clamping diode to operate, the control signal source must provide a dc return to ground for V1. Note also that the maximum control voltage is lower (240v) for PC 57 than it is for PC 56 (280v) because a minimum plate voltage of about 60v is necessary for the cathode follower. These plate voltages are within the maximum ratings of the 5725 as defined by MIL–E–1B, paragraph 3.5.1.

2.4 *Trigger:* The circuit can be triggered at either the plate or the suppressor of the phantastron.

(*a*) Input 1. Triggering is accomplished by a negative trigger coupled to the phantastron plate through the diode V1. The trigger source does not load the phantastron because it is disconnected by the diode as soon as the phantastron fires. The control signal line may require decoupling to prevent false triggering if the control voltage is obtained from a remote source.

The trigger must have an amplitude of 15v and a duration of 2μsec for reliable operation. Higher voltage triggers produce a spike at the beginning of the waveforms; excessively long triggers may distort the leading portion of the waveform and increase the minimum duration.

(*b*) Input 2. The circuit may also be triggered by a positive trigger applied to the suppressor. The amplitude requirement here is 20v and triggering is more critical because the trailing edge of the trigger may tend to end the phantastron cycle prematurely. A duration between 0.1 and 2μsec is required. This input is especially useful for direct coupling. A diode may be used to eliminate the effects of the negative-going portion of the trigger.

2.5 *Output:* The outputs are approximately rectangular pulses whose amplitudes are constant but whose duration is a function of the reference voltage. Output 1 from the screen is positive and about 60v in amplitude, and output 2 from the cathode is negative and 10v in amplitude. The rise time of either output is 0.1 to 0.2μsec and the decay time about 0.1% of the maximum duration. If the final output required is a trigger or marker pulse, the trailing edge of output 2 may be used as the series trigger for a blocking oscillator such as PC 49.

2.6 *Performance:* While equation (1) can be used to determine the output duration approximately, a more careful analysis [2] indicates that the gain of the feedback circuit also has an effect. Tube aging will cause gradual changes in duration, and replacing either the 5725 or the 5814A may cause relatively large changes. Typical changes in maximum duration with change in tubes are about 2% for the 5725 and 0.3% for the 5814A. For highest accuracy the circuit should be calibrated frequently.

Figure 56–1 shows typical curves of error versus control signal for these circuits. These curves were obtained by plotting duration versus control vol-

[2] F. C. Williams and N. F. Moody, "Ranging Circuits, Linear Time Base Generators and Associated Circuits," *Proc. IEE*, Radiolocation Convention, No. 1, 1946, vol. 93, pp. 1188–1190.

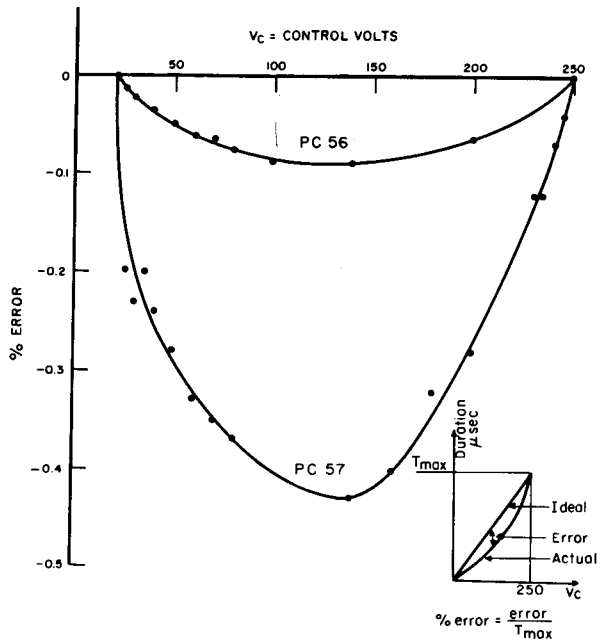


Fig. 56-1

The phantastron was calibrated for zero error at control voltages of 20 and 250 volts. The error expressed in percent of maximum duration is approximately correct for durations up to 2500 microseconds.

tage from 10 to 250v. The error is the difference between this curve and a straight line drawn through the initial and final points on the curve. When expressed as a percentage of the maximum duration, the error is essentially independent of the values of C3 and R3. These curves represent the error introduced by the preferred circuit itself (due to non-linearity of the plate rundown, finite turn-on and turn-off times, etc.). Since the control circuit must supply current to diode V1, the phantastron loads the control signal source. This usually introduces additional error which must be determined for the individual application. The control circuit does not load the phantastron because it is disconnected by the diode as soon as the phantastron fires.

As indicated by the curves, the maximum error is increased when a cathode follower is used. The phantastron linearity is obtained by the feedback between grid and plate which tends to maintain a constant discharge current from the grid capacitor. The compensation is less complete using a cathode follower since its gain is less than unity.

Determining the error by calibration at the end points of the duration versus control voltage curve as described above is convenient for presenting error curves, but results in an error which is always negative and larger than it need be. If the circuit can be calibrated to give equal positive and negative errors, the error can be reduced 50%. A simple way to do this approximately is to calibrate for zero error at 85% of maximum control voltage (fig. 56-2). Still further reduction is obtained by

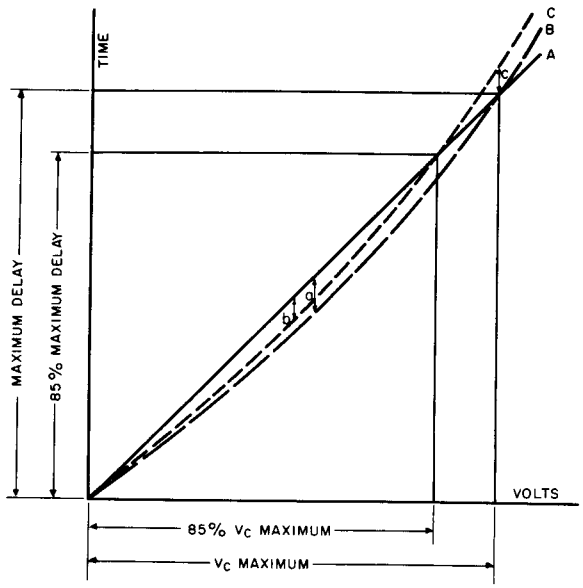


Fig. 56-2 PHANTASTRON CALIBRATION

A. Ideal curve of duration versus control voltage.
B. Actual curve of duration versus control voltage calibrated for zero error at maximum control voltage. (Curvature is greatly exaggerated). Error (a) is always negative.
C. Actual curve of duration versus control voltage calibrated for zero error at 85% of maximum control voltage. Positive and negative errors (b) and (c) are approximately equal and about half the error (a).

calibrating at the 10 and 85% points. Lowering the range over which the control signal voltage varies also reduces the error. For example, reducing the maximum control voltage to 150v reduces the error to about 0.05% for PC 56 and 0.1% for PC 57.

Jitter is negligible when the suppressor voltage is maintained at least 2v positive with respect to the cathode during rundown.

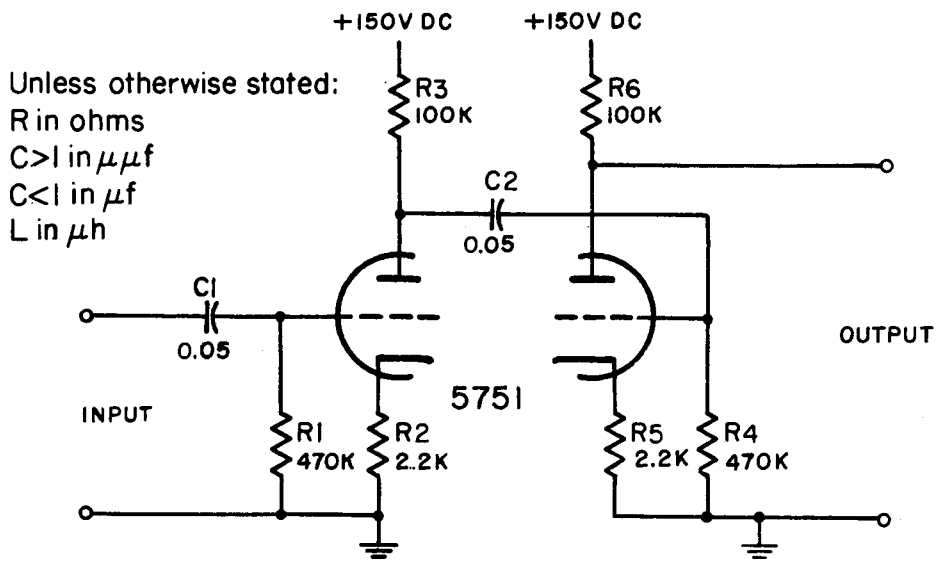
The control signal should be derived from the plate supply whenever possible to minimize the effects of changes in plate supply voltage. Under

these conditions a 10% change in supply voltage causes about 0.1% change of maximum duration. A 10% change in filament voltage also causes a 0.1% change in duration. These changes in duration are nearly constant over the range of the control voltage and are in the same direction. [3] If the plate supply and control voltage change independently the duration will change proportionally. When the circuit was operated from an unregulated supply, the change in duration with change in line voltage was not constant over the control range but varied from 0.1% to 0.6% of maximum duration as the control voltage increased from 20 to 250 volts.

[3] B. Chance, ed., *Electronic Time Measurements, Rad. Lab. Series*, vol. 20, McGraw-Hill, 1949, p. 122.

NBS PREFERRED CIRCUIT NO. 60
AUDIO VOLTAGE AMPLIFIER

NBS PREFERRED CIRCUIT NO. 60
AUDIO VOLTAGE AMPLIFIER



Frequency response: 30 to 8000cps ±1db.
Voltage gain per stage: approximately 18.
Intermodulation distortion: 2% at maximum output.
Harmonic distortion: less than 1% at maximum output.
Input level: 0.07v rms maximum.
Output level: 21v rms maximum output across 500KΩ load.
15v rms maximum output across 100KΩ load.
Noise level: 0.016v rms across 100KΩ load.
R2,R3,R5,R6: ±10%; R1,R4: ±20% limits.
All C: ±20% limits.

PC 60 AUDIO VOLTAGE AMPLIFIER

1. APPLICATION

The purpose of the audio voltage-amplifier stage is to amplify audio signals in communications or other equipment to the level necessary to drive a power-output stage.

2. DESIGN CONSIDERATIONS

In choosing a tube for this application, the 12AX7 was found to have the best characteristics.

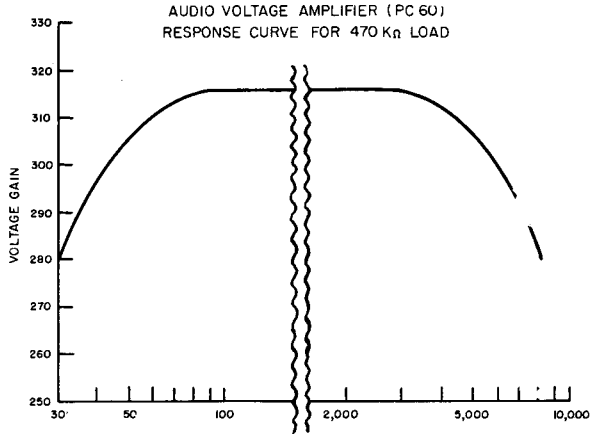


Fig. 60-1

It had one drawback however, as the tube is prone to be microphonic. Its equivalent, the 5751, which is not microphonic, has almost the same characteristics with one exception, the amplification factor of the 5751 is 70 while the amplication factor of the 12AX7 is 100.

The circuit is conventional except for the degenerative feedback chosen to compensate for voltage and tube variation.

The frequency response chosen adequately covers the speech range, which is from 150cps to 7000cps, as shown in figure 60-1, with intermodulation distortion of 2%.

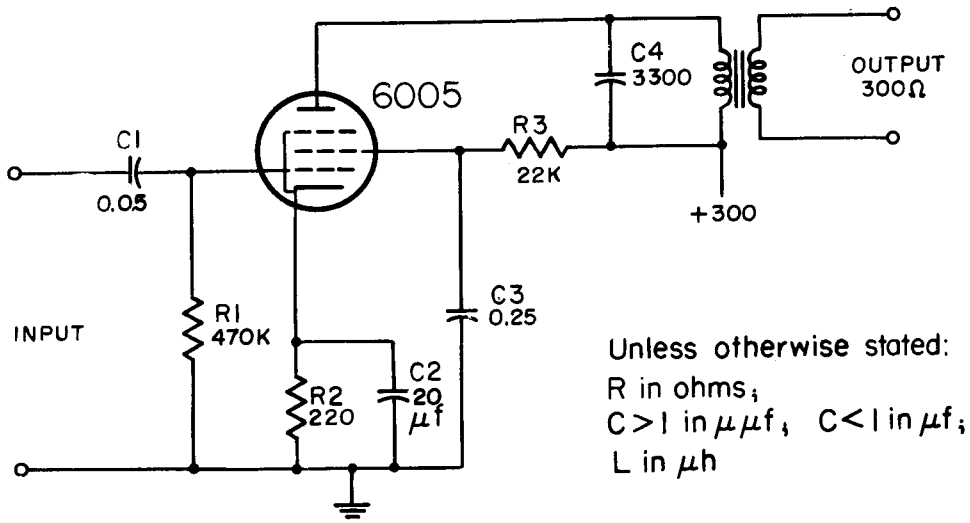
Since the circuits preceding the audio section supply signal levels in the order of 0.01v rms to 0.06v rms, a voltage gain of 320 was considered sufficient to drive a power-output stage.

Each stage can be operated separately with no loss in gain per stage or loss in fidelity.

Power-supply voltage was set at 150v because higher values would increase the voltage gain very little, while power dissipation would be increased by a large amount. This value is one of the preferred values of supply voltage.

NBS PREFERRED CIRCUIT NO. 61
AUDIO POWER AMPLIFIER

NBS PREFERRED CIRCUIT NO. 61
AUDIO POWER AMPLIFIER



Frequency response: Down 3db at 300 and 6500cps.
Maximum input level: 5v rms.
Maximum output level: 25v rms across 300Ω load.
Maximum power output: 2 watts.
Harmonic distortion: 4% at maximum power output.
Output impedance: 300Ω.
Noise level: 0.005v rms.
All R: ±20% limits.
All C: ±20% limits.

PC 61 AUDIO POWER AMPLIFIER

1. APPLICATION

The audio power-amplifier converts a signal voltage, generally obtained from a voltage amplifier, into an output of sufficient level for driving a transducer, such as a loudspeaker, or a long transmission line.

The audio power-amplifier is used most frequently as the output stage of AM or FM receivers.

2. DESIGN CONSIDERATIONS

The tube type chosen was the 6005, which is the "reliable" equivalent of the 6AQ5. This beam power tube was selected because it has higher plate efficiency and greater power sensitivity than a triode, while the higher-order harmonic distortion is less than for power pentodes. The beam power tube distortion is predominantly second-harmonic and can be minimized by the use of negative feed back.

The circuit is a conventional transformer-coupled power stage. A capacitor shunted across the primary of the output transformer limits the high-frequency response. Its value may be lowered to favor the higher frequencies if desired.

An important factor in determining the response of a power-amplifier is the output transformer. In equipment where space and weight are important factors, it is necessary to limit the physical size of the transformers. This reduces the amount of iron and copper, thus limiting the low-frequency response and the primary current capacity.

The transformer used in testing this circuit had a frequency response of ±2db at 300 to 10,000cps and a maximum primary current of 40ma. Using a 0.0033μf capacitor across the primary of the output transformer, the frequency response of the amplifier is down 3db at 300 and 6500cps as shown in figure 61-1.

Total harmonic distortion at maximum power output is less than 4% over most of the frequency range. At the lower frequencies the harmonic distortion rises very rapidly because of the drop in tube load impedance due to the shunting effect of the primary inductance of the output trans-

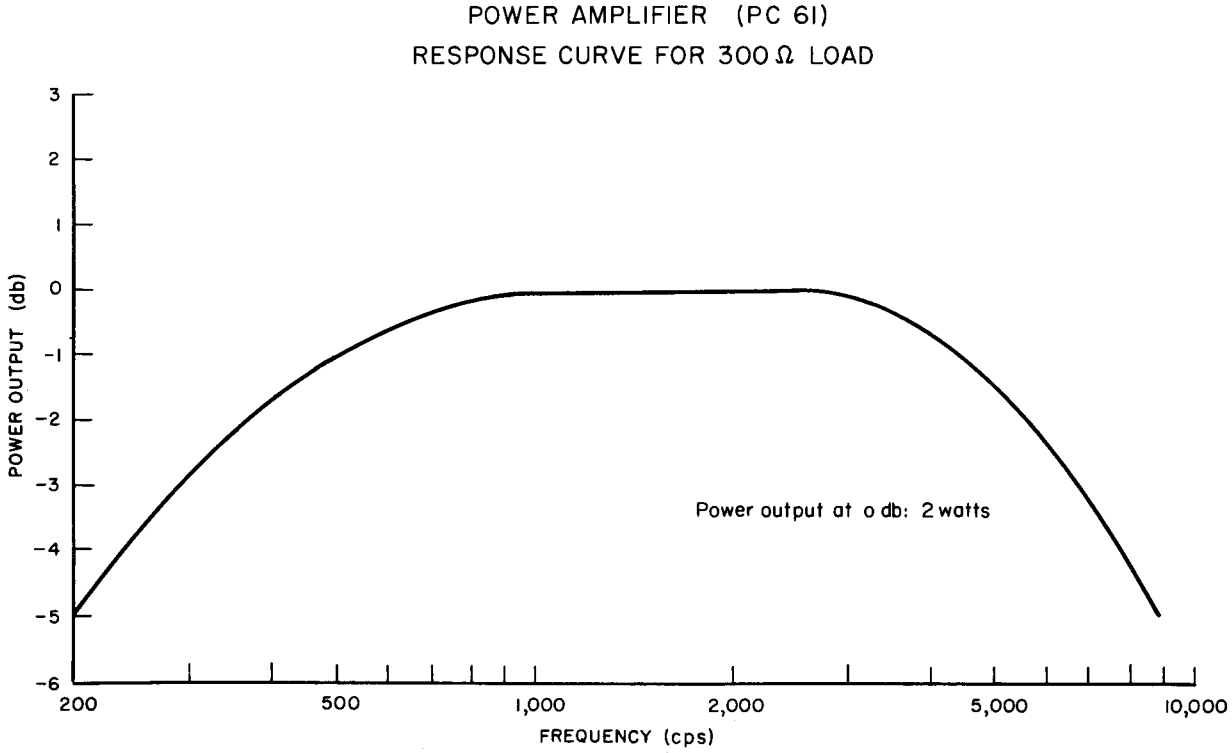


Fig. 61-1

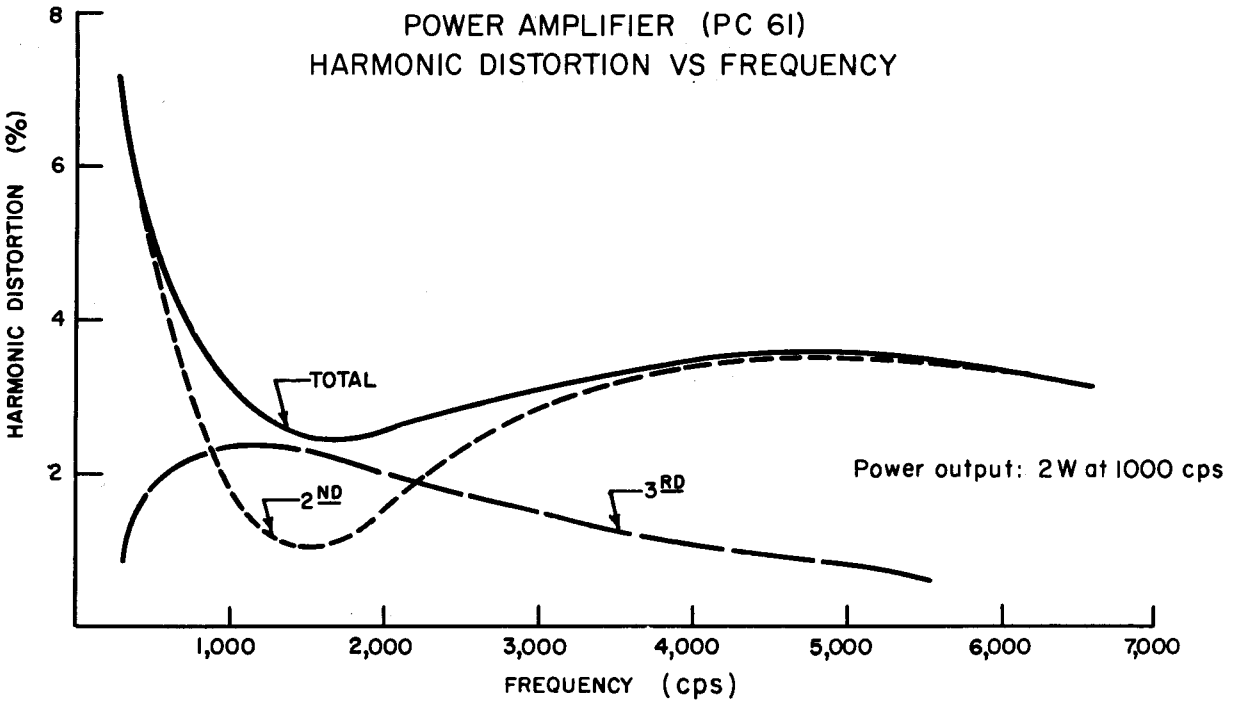


Fig. 61-2

former. Figure 61-2 shows the harmonic content of the amplifier at maximum power output. Figure 61-3 shows the rise in percent distortion with increase in power output.

This circuit is designed to draw about 30ma plate current at maximum power output of 2 watts.

The output impedance was chosen as 300Ω as this is a standard line impedance. Other output impedances may be taken by changing the output transformer to the desired ratio, keeping in mind that the primary impedance must be approximately 5000Ω.

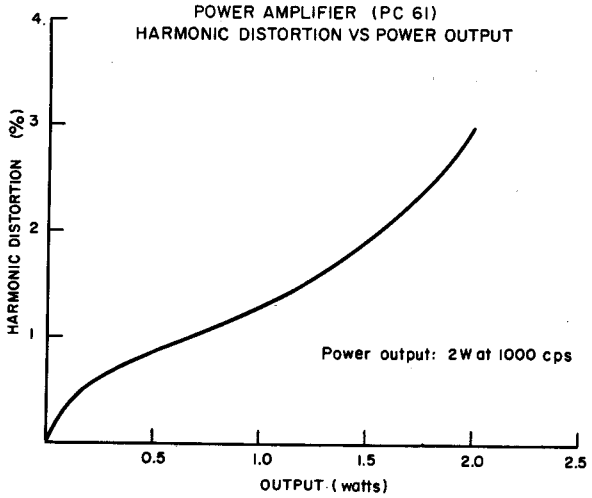
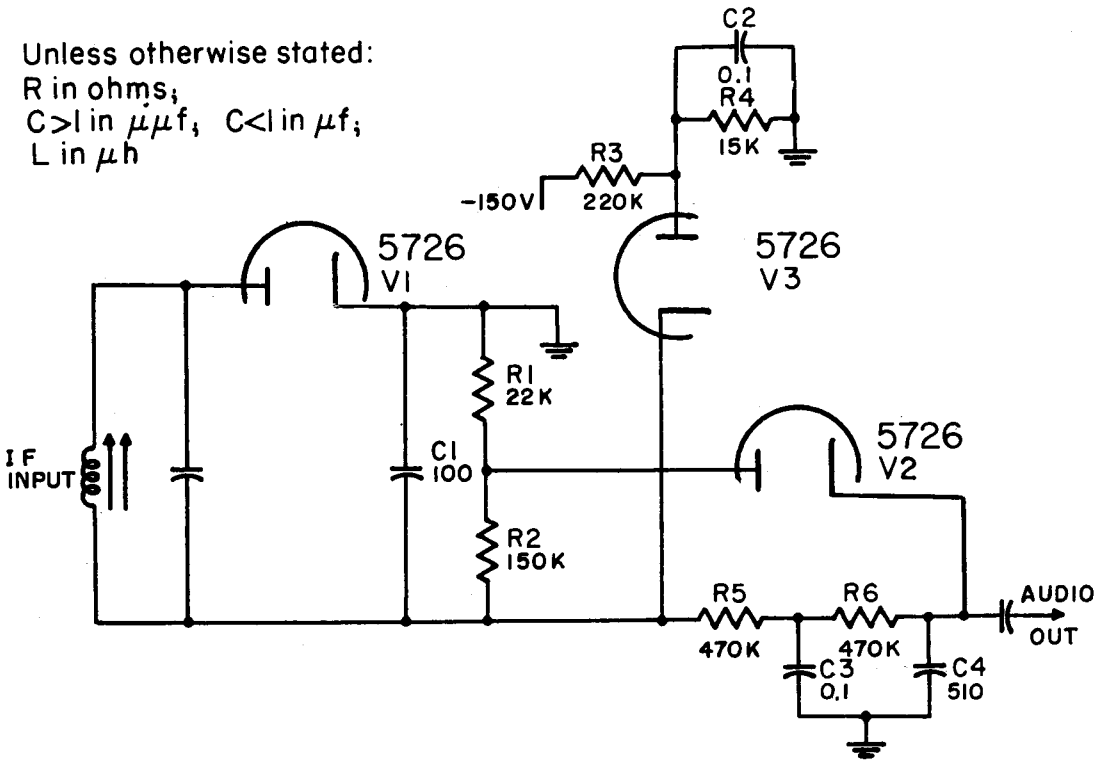


Fig. 61-3

NBS PREFERRED CIRCUIT NO. 62
DETECTOR AND NOISE LIMITER

NBS PREFERRED CIRCUIT NO. 62
DETECTOR AND NOISE LIMITER



Detector:

Input: i-f modulated signals; 1.6 to 30mc; 1 volt rms to 7v rms.

Output: 0.025 to 0.20v rms audio signal across 22KΩ load.

DC voltage developed: −1.5v to −7.5v (automatic bias).

Limiter:

Output: 0.02 to 0.15v rms.

Clips all pulses above automatic bias.

Shunts output for noise-pulse magnitudes greater than −10v peak.

Frequency response: down 1.5db at 4000cps from 30cps.

R3,R4: ±10%; R1,R2,R5,R6: ±20% limits. All C: ±20% limits.

PC 62 DETECTOR AND NOISE LIMITER

1. APPLICATION

The function of the detector and noise limiter combination is to demodulate the incoming signal and to reduce the effect of short-duration electrical disturbances on the output of an AM receiver.

2. DESIGN CONSIDERATIONS

The input is a modulated i-f sinusoidal signal. V1, the diode detector, is connected to clip the positive half of the signal. The carrier is bypassed to ground and the demodulated signal is fed to the plate of V2, the series noise limiter. The series limiter is biased automatically by the incoming signal; any noise pulse exceeding this bias is clipped. V3 is used as a shunt limiter. Noise pulses with peak amplitudes exceeding the fixed bias of −10 volts on the plate cause the diode to conduct, effectively placing a short circuit across the output of the last i-f transformer for the duration of the pulse. This pulse is thereby prevented from operating the agc circuit and desensitizing the i-f amplifiers.

The input level of the detector ranges from 1 to 7 volts rms. Output of the detector with the above input is from 0.025 to 0.2 volts rms across a 22K load. The output range can be extended by varying the voltage divider at the output of the detector.

The frequency input range of the detector depends upon the rf bypass capacitor in the output. The range may be extended by increasing the value of this capacitor.

The frequency response of the detector and noise limiter combination is down 1.5db at 4000cps from 30cps. The drop at the high end is due to the time constants of the filter network of the noise-limiter circuit. Figure 62-1 shows this response.

Figures 62-2 and 62-3 (page 62-4) show the ac and dc characteristics of the detector.

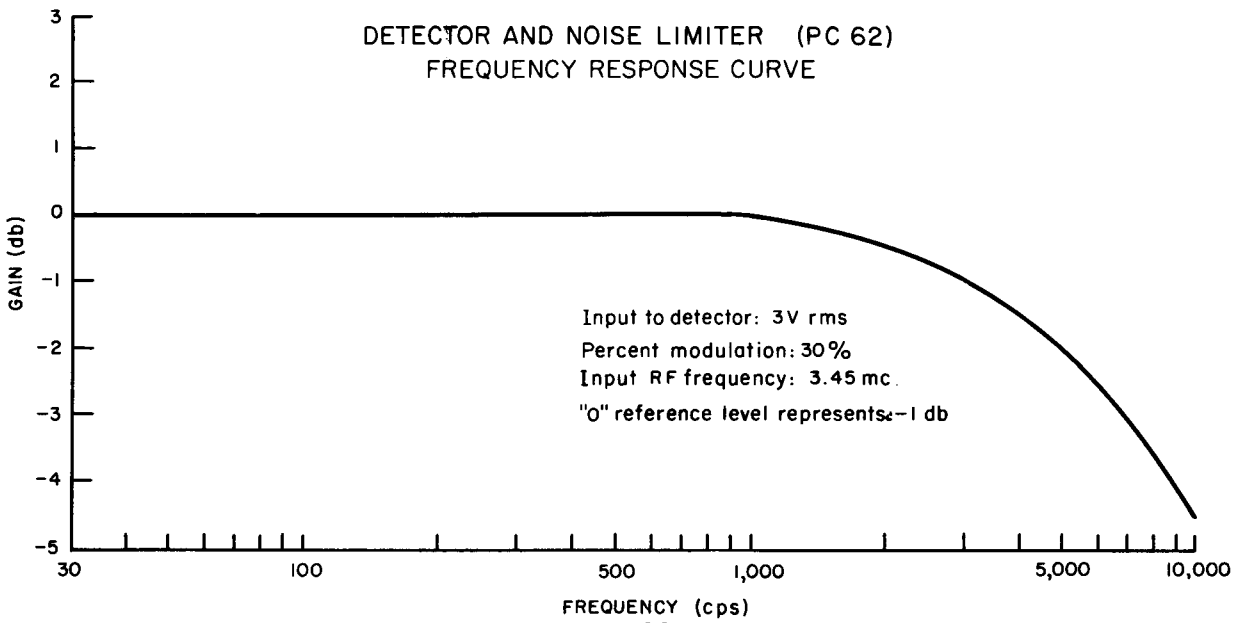


Fig 62-1

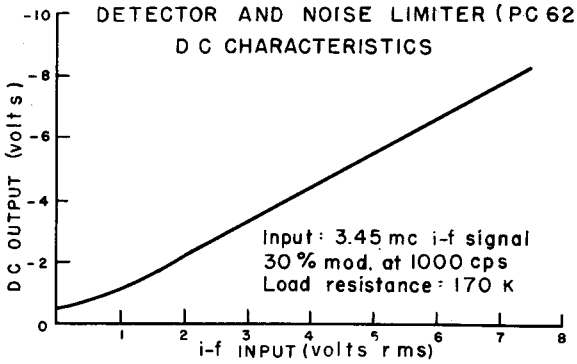


Fig. 62-2

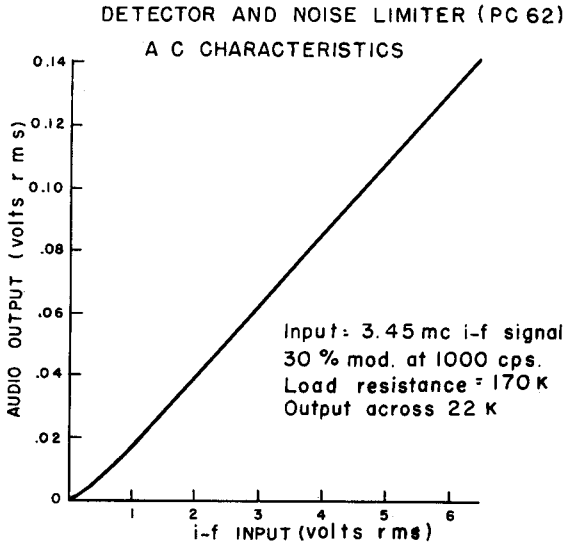
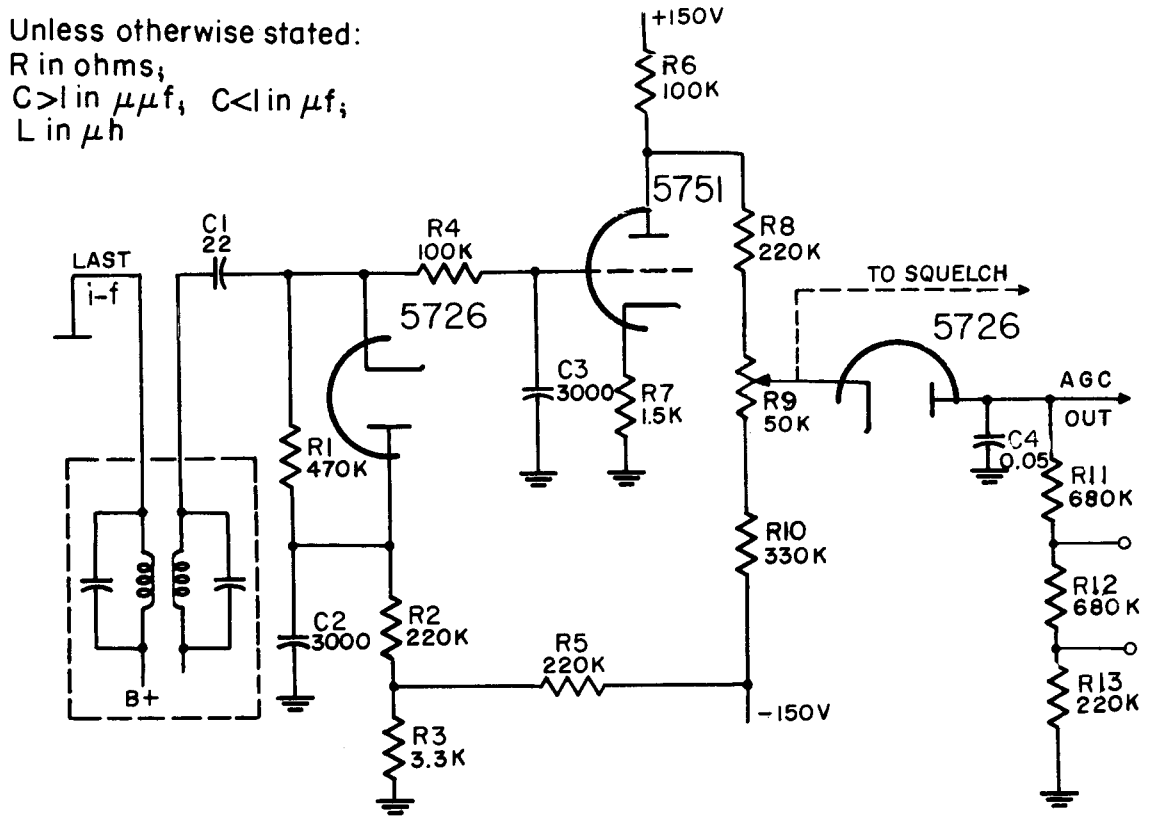


Fig. 62-3

NBS PREFERRED CIRCUIT NO. 63
AUTOMATIC GAIN CONTROL

NBS PREFERRED CIRCUIT NO. 63
AUTOMATIC GAIN CONTROL



Input: i-f modulated signals; 1.6 to 30mc.
Level: 0 to 7v rms.
Output: 0 to −35v dc.
Delay voltage: +1.5v dc.
R2,R6,R8,R10: ±10%; R1,R3,R4,R5,R7,R9,R11,R12,R13: ±20% limits.
C3: ±10%; C1,C2,C4: ±20% limits.

PC 63 AUTOMATIC GAIN CONTROL

1. APPLICATION

Automatic gain-control is a device which automatically varies the over-all gain in a radio receiver in an inverse ratio to the strength of the received rf signal.

2. DESIGN CONSIDERATIONS

Amplified "agc" was selected because this method offers an effective way of controlling the total amplification of a radio receiver. The advantages of this method are that it retains the full amplification of the agc channel under all conditions and some isolation between the agc and i-f channel does exist.

The signal is taken from the secondary of the last i-f transformer and is rectified by a separate detector. The rectified positive voltage is used to control the dc amplifier. The amplifier uses a 5751 with cathode degeneration for gain stability.

The voltage-divider network, connected from the plate of the amplifier to the negative voltage supply, effectively shunts the dc amplifier.

The voltage divider at the output of the diode may be any combination of values as long as the total resistance is not less than 1.5MΩ. Below this value the output of the circuit is reduced.

This circuit has the advantage that if the dc amplifier becomes inoperative so that the 5751 ceases to draw current, the receiver continues to operate.

Figure 63–1 is an agc characteristic curve showing peak-to-peak input volts at the agc detector versus agc output voltage. The slight reverse bend in the curve is due to the response of the dc amplifier. Figure 63–2 is an agc performance

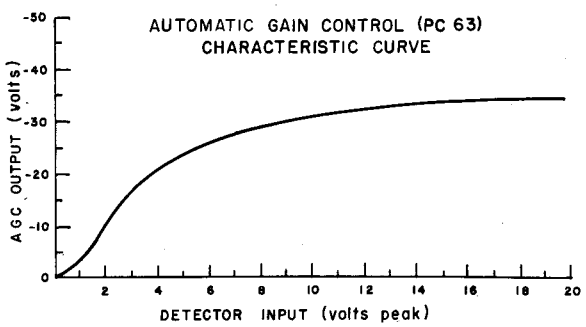


Fig. 63–1

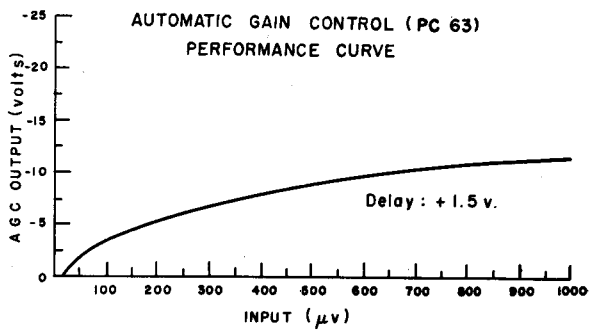


Fig. 63–2

curve showing agc control on a three-stage i-f strip. Two of the i-f amplifiers have full agc voltage applied to them while the stage preceding the agc detector has only a part of the agc voltage applied. This was done to reduce distortion due to nonlinearity of the tube characteristics. The most severe conditions for nonlinear distortion will be obtained in the i-f stage preceding the detector stage and the worst condition is given when the grid bias, due to agc, is large.

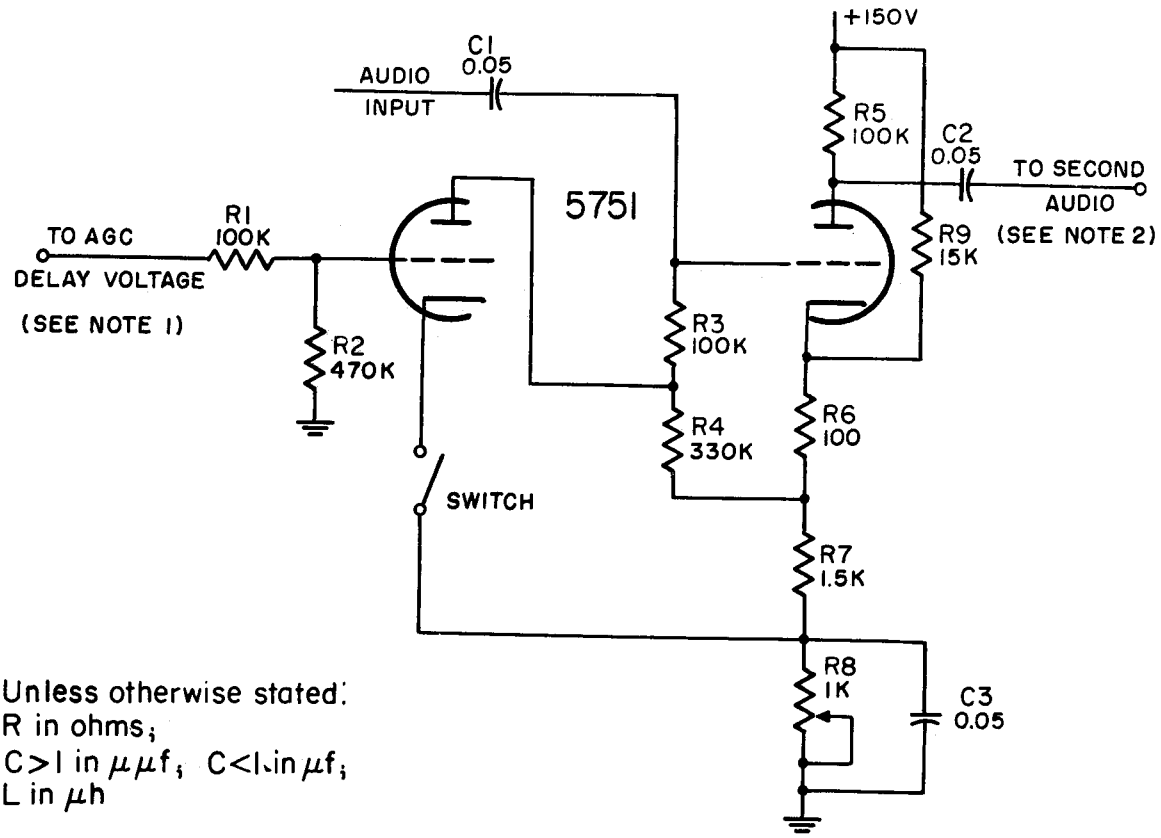
Under no-signal conditions, the agc amplifier stage is cut off and 1.5v positive can be measured at the junction of R8 and R10, due to the values chosen for the voltage-divider network. This voltage is used to delay the application of agc voltage to the i-f and rf stages. In addition, this positive voltage is used to operate the squelch circuit PC 64. Also at the junction of R8 and R10 a diode is connected so that it will only pass a negative voltage, thus providing "delayed agc" and protecting the controlled stages from high positive potentials in case the negative supply voltage fails.

With an input signal, an integrated positive dc voltage is applied to the grid of the dc amplifier, causing it to conduct. This produces a voltage drop at the plate which in turn produces a negative voltage at the junction of R8 and R10. This voltage is then applied to the cathode of a diode whose plate circuit feeds the agc voltage to the i-f and rf amplifiers. The agc is delayed because no agc voltage is applied to the grids of the controlled stages until the carrier amplitude reaches a high enough value to overcome the positive delay voltage. Therefore, the receiver will have its maximum sensitivity for signals below this level.

392077 O-56-10

NBS PREFERRED CIRCUIT NO. 64
SQUELCH

NBS PREFERRED CIRCUIT NO. 64
SQUELCH



Input:

(*a*) No signal condition: agc delay voltage of +1.5v dc.

(*b*) Signal condition: agc voltage of 0 to −35v dc.

Cutoff voltage: −1.6v dc for threshold set at minimum sensitivity.
−0.8v dc for threshold set at maximum sensitivity.

R3,R4,R5: ±10%; R1,R2,R6,R7,R8: ±20% limits.

All C: ±20% limits.

NOTES:

1. This point is connected at the potentiometer arm of R9 of PC 63 or, in case another agc circuit is used, to the agc delay point.
2. The audio section of this circuit includes the first audio of PC 60.

PC 64 SQUELCH

1. APPLICATION

In a sensitive receiver incorporating agc the purpose of the squelch circuit is to reduce the objectionable increase in noise output as the receiver is tuned from one signal to another. It is also used to silence the receiver until a signal of usable level is received.

2. DESIGN CONSIDERATIONS

With this type of circuit it is desirable for the receiver to come into operation with the weakest possible signal voltage. To achieve this high sensitivity without excessive background noise from various sources, it is desirable to have a variable "threshold" control. This control, which is located in the cathode circuit, varies the amount of bias on the squelch tube and therefore controls the sensitivity of the circuit. The squelch tube is used as a dc amplifier to control the amount of bias on the first audio stage.

With no input signal to the receiver, the agc delay voltage, which is positive, appears on the grid of the squelch tube, causing the tube to draw maximum current. The current flowing through the high-value plate resistor produces a voltage drop at the grid of the first audio, thus cutting off the stage. For signal conditions, the grid of the squelch tube becomes negative, due to agc action, so that this stage is cutoff and the first audio amplifier operates at normal gain. The squelch tube cuts off with an agc input of −0.8v dc at maximum sensitivity and at −1.6v dc at minimum sensitivity.

The cathode circuit of the squelch is completed through a switch, which is normally closed. By opening the switch the squelch is made inoperative. The bias on the cathode is varied from approximately +2 volts for maximum sensitivity to 0 volts for minimum sensitivity by the threshold control.

The sensitivity of the circuit is shown graphically in figure 64–1. The threshold control is set for maximum sensitivity.

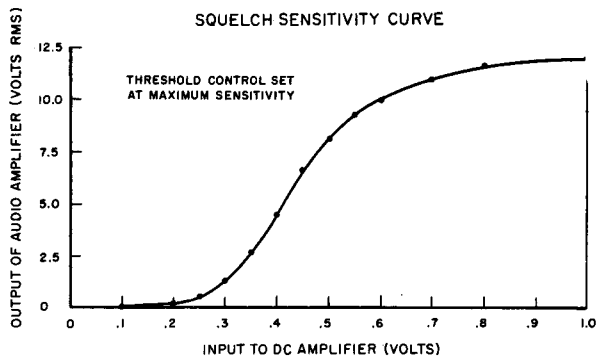


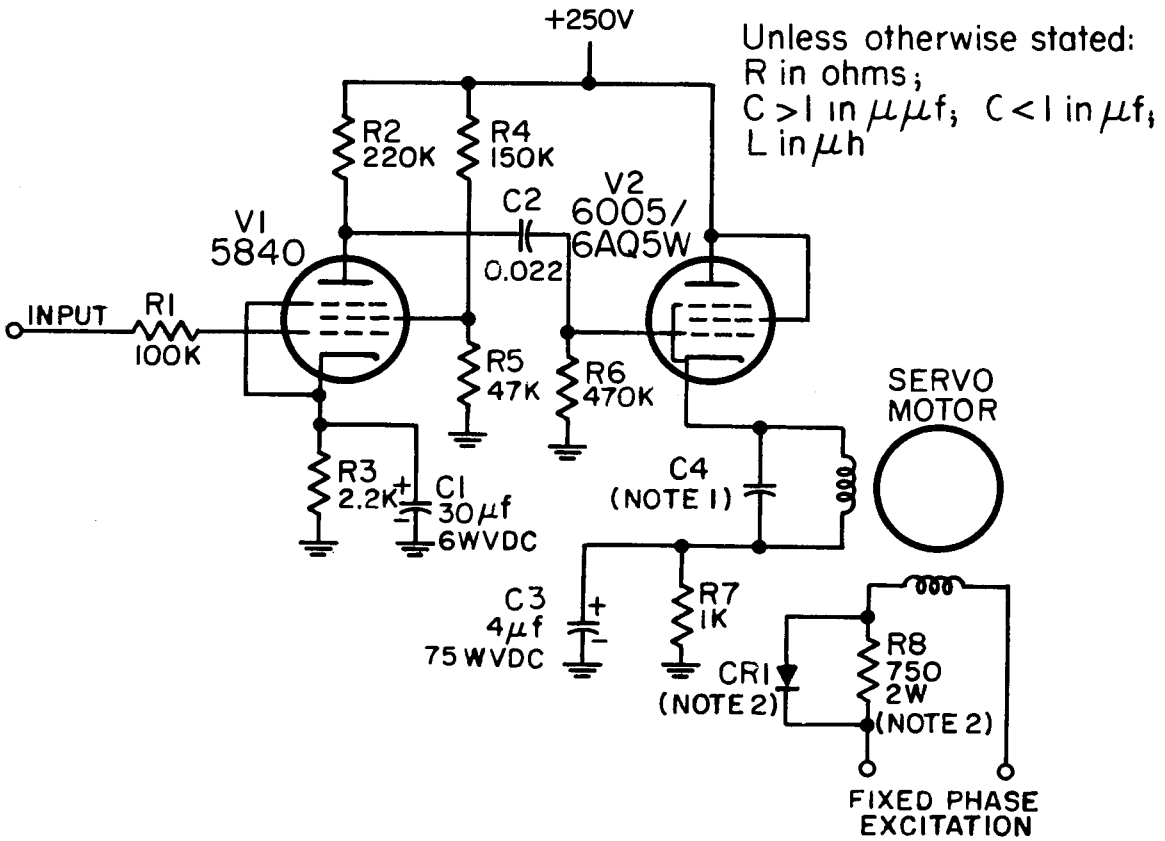
Fig. 64-1

NBS PREFERRED CIRCUIT NO. 70

INSTRUMENT SERVO MOTOR CONTROLLER

NBS PREFERRED CIRCUIT NO. 70

INSTRUMENT SERVO MOTOR CONTROLLER



Components:

Servo motor: Mark 7 Mod 1 or Mark 14 Mod 0, Navy Bureau of Ordnance.

CR1: Silicon rectifier with rating of 75 ma and 70-volt reverse working voltage.

All R: ±20% limits. C2: ±20% limits; C1, C3: −20%, + 50% limits; C4: ±10% limits. (Note 3)

(Specifications continued on next page.)

Operating characteristics:

Signal frequency: 380 to 420 cps.

Small-signal voltage amplification: 65.

Effective load resistance: 2K to 4KΩ.

Nominal power output: 1 watt.

Voltage output: Equivalent to 50 volts rms of fundamental in-phase component.

Power requirements:

250 volts dc ±5% at 18 ma for zero signal, and 30 ma for maximum signal.

6.3 volts ac ±10% at 600 ma.

NOTES:

1. C4 resonates with the motor winding. Because of the large resonance currents, a 100-volt rms rating at the highest expected ambient temperature is required. An extended foil type is recommended to decrease dissipation. Typical values are 0.27 μf for the Mark 7 Mod 1 and 0.15 μf for the Mark 14 Mod 0.

2. CR1 and R8 are selected to provide the desired amount of direct current in fixed Phase winding. (See section 2.3.)

3. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified above. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.

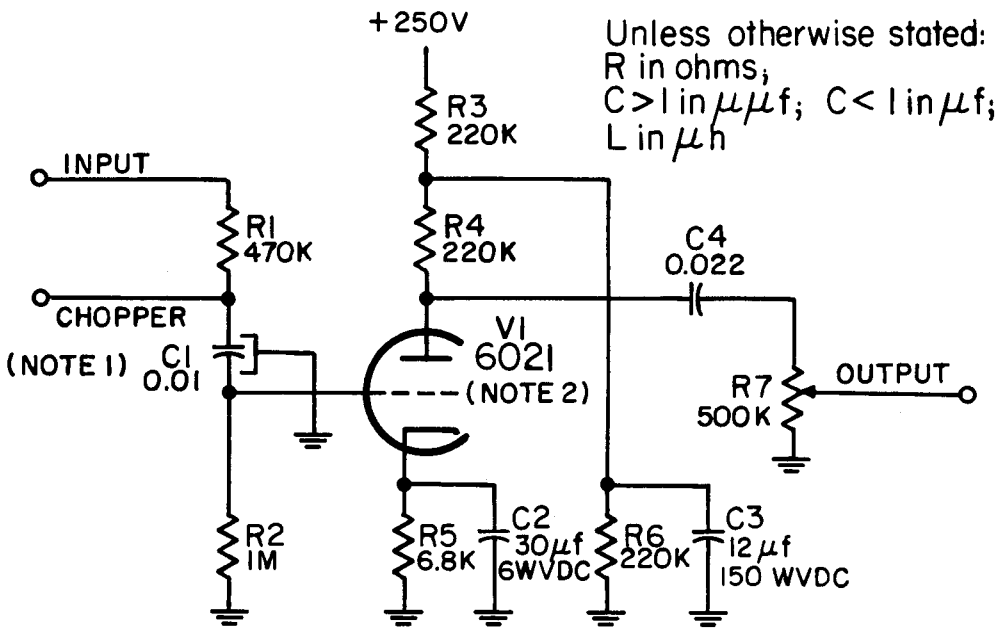
4. Separate ground systems are required for signals, power, and shielding. (See Notes to the Preferred Circuits Manual, section 15.)

NBS PREFERRED CIRCUIT NO. 71

SERVO PREAMPLIFIER, AMPLIFICATION 15

NBS PREFERRED CIRCUIT NO. 71

SERVO PREAMPLIFIER, AMPLIFICATION 15



Components:

All R: ±20% limits. C1, C4: ±20% limits; C2, C3: −20%, +50% limits. (Note 3)

Operating characteristics:

Signal frequency: 380 to 420 cps.

Voltage amplification for 400 cps input: 15.

Approximate voltage amplification for dc input: 2.0 volts peak-to-peak output for 0.1 volt dc input.

Maximum sine-wave output voltage: 7.5 volts rms (2.5% distortion).

Power requirements:

250 volts dc ±5% at 0.7 ma.

6.3 volts ac ±10% at 300 ma (150 ma if a 5718 is used).

NOTES:

1. Chopper is used with dc inputs only.
2. If a single triode is required, a 5718 may be used to provide a gain of 11.
3. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified above. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.
4. Separate ground systems are required for signals, power, and shielding. (See Notes to the Preferred Circuits Manual, section 15.)

NBS PREFERRED CIRCUIT NO. 72

SERVO PREAMPLIFIER, AMPLIFICATION 70

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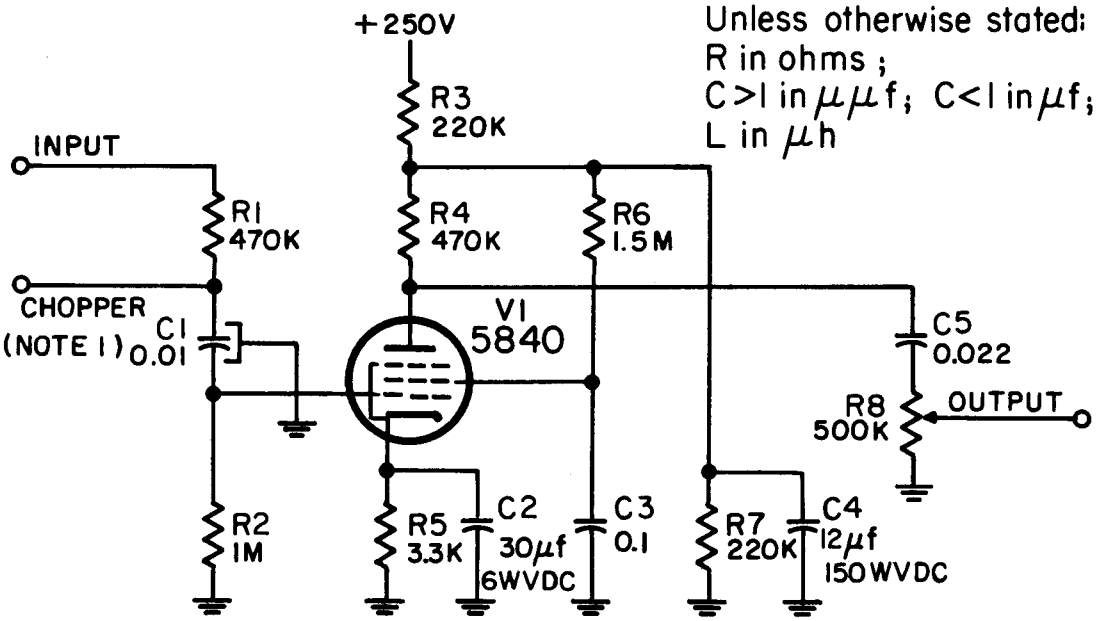
NBS PREFERRED CIRCUIT NO. 72

SERVO PREAMPLIFIER, AMPLIFICATION 70



Components:

All R: ±20% limits. C1, C5: ±20% limits; C2, C3, C4: −20%, + 50% limits. (Note 2)

Operating characteristics:

Signal frequency: 380 to 420 cps.

Voltage amplification for 400 cps input: 70.

Approximate voltage amplification for dc input: 2.0 volts peak-to-peak output for 0.02 volt dc input.

Maximum sine-wave output voltage: 7.5 volts rms (2.5% distortion).

Power requirements:

250 volts dc ±5% at 0.75 ma.

6.3 volts ac ±10% at 150 ma.

NOTES:

1. Chopper is used with dc inputs only.

2. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified above. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.

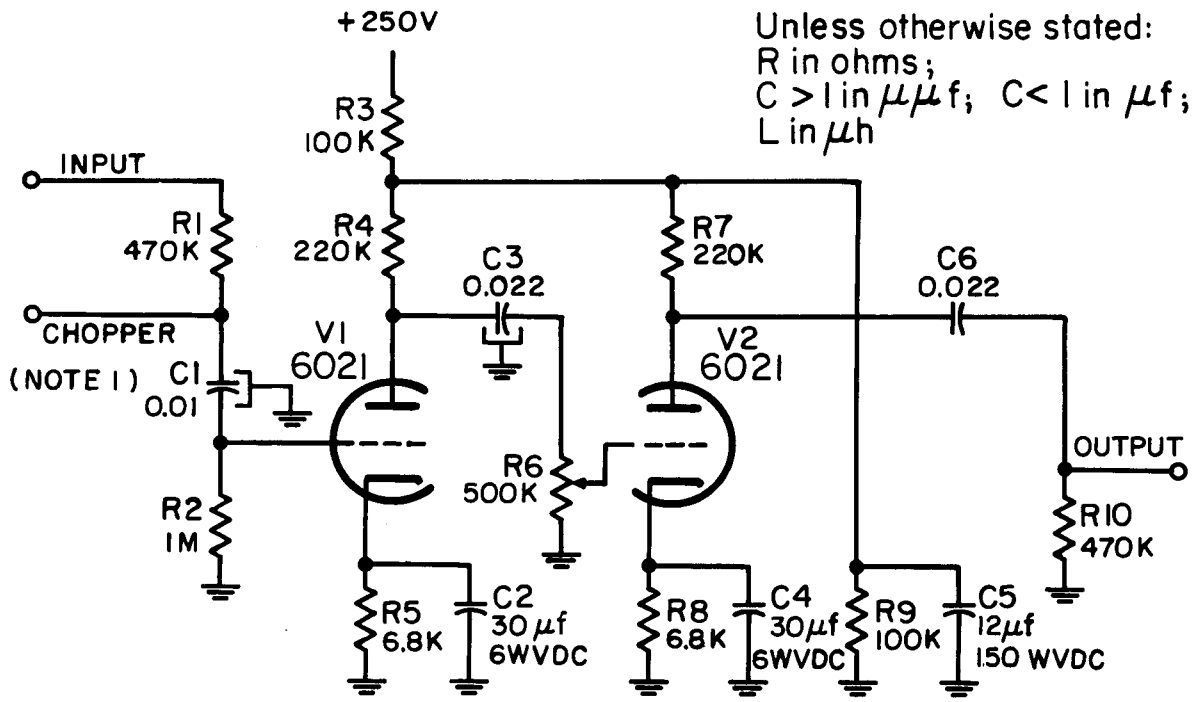
3. Separate ground systems are required for signals, power, and shielding. (See Notes to the Preferred Circuits Manual, section 15.)

NBS PREFERRED CIRCUIT NO. 73

SERVO PREAMPLIFIER, AMPLIFICATION 300

NBS PREFERRED CIRCUIT NO. 73

SERVO PREAMPLIFIER, AMPLIFICATION 300



Components:

All R: ±20% limits. C1, C3, C6: ±20% limits; C2, C4, C5: −20%, +50% limits. (Note 2)

Operating characteristics:

Signal frequency: 380 to 420 cps.

Voltage amplification for 400 cps input: 300.

Approximate voltage amplification for dc input: 2.0 volts peak-to-peak output for 0.004 volt dc input.

Maximum sine-wave output voltage: 7.5 volts rms (2.5% distortion).

Power requirements:

250 volts dc ±5% at 1.5 ma.

6.3 volts ac ±10% at 300 ma.

NOTES:

1. Chopper is used with dc inputs only.

2. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified above. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.

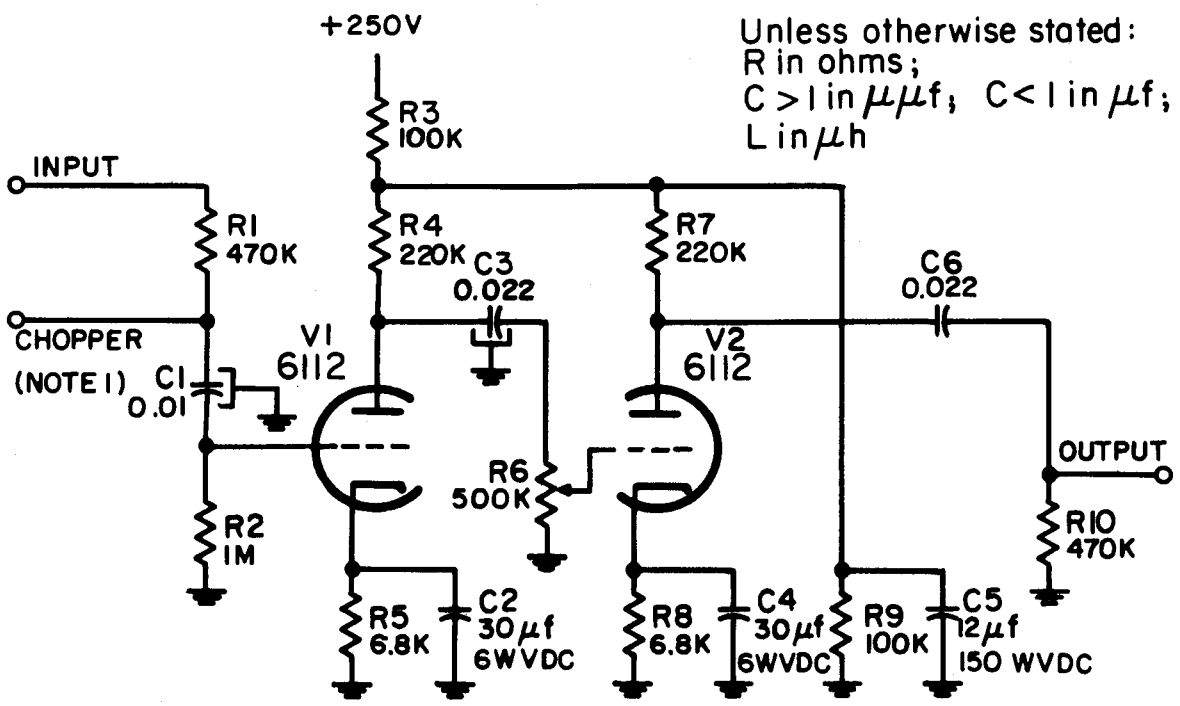
3. Separate ground systems are required for signals, power, and shielding. (See Notes to the Preferred Circuits Manual, section 15.)

NBS PREFERRED CIRCUIT NO. 74

SERVO PREAMPLIFIER, AMPLIFICATION 1200

NBS PREFERRED CIRCUIT NO. 74

SERVO PREAMPLIFIER, AMPLIFICATION 1200



Components:

All R: ±20% limits. C1, C3, C6: ±20% limits; C2 C4, C5: −20%, +50% limits. (Note 2)

Operating characteristics:

Signal frequency: 380 to 420 cps.

Voltage amplification for 400 cps input: 1200.

Approximate voltage amplification for dc input: 2.0 volts peak-to-peak output for 0.001 dc input.

Maximum sine-wave output voltage: 7.5 volts rms (2.5% distortion).

Power requirements:

250 volts dc ±5% at 1.5 ma.

6.3 volts ac ±10% at 300 ma.

NOTES:

1. Chopper is used with dc inputs only.

2. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified above. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.

3. Because of the high gain of this circuit, care in layout must be exercised to avoid oscillation.

4. Separate ground systems are required for signals, power, and shielding. (See Notes to the Preferred Circuits Manual, section 15.)

PC 70 INSTRUMENT SERVO MOTOR CONTROLLER
PC 71, 72, 73, AND 74 SERVO PREAMPLIFIERS

1. APPLICATION[1]

The instrument servo motor controller, PC 70, is used to excite the control winding of a two-phase servo motor of the Navy Bureau of Ordnance size 11 or size 15 class similar to Mark 7 Mod 1 and Mark 14 Mod 0, as identified in Navy Bureau of Ordnance Publication OP–1755–A. The circuit will deliver a nominal output of one watt to loads with effective resistances between 2K and 4KΩ.

The 50-volt maximum output of PC 70 is less than the rated control voltage of either of the motors specified. The speed and torque *per degree error* are increased, however, by the use of direct current in the motor windings to increase the motor damping and permit higher amplifier gains. The result is a servo with improved torque and speed of response at low inputs (small errors), although maximum speed and torque are decreased.

The 115-volt connection for the motor control winding must be used to satisfy the load impedance requirements. With direct current in the windings and the 50-volt maximum output of the amplifier, the no-load speed of the motor is reduced 25% and the stall torque about 50% from their rated values. The decreased no-load speed increases the settling time when the computer is turned on and also the time required for the computer to respond to large errors. The decrease in stall torque can be tolerated if the loaded motor will run continuously with 10 volts on the control phase and 115 volts on the fixed phase.

The preamplifiers, Preferred Circuits 71, 72, 73, and 74, are used with the instrument servo motor controller to increase the available gain. The choice of preamplifier circuit depends on the gain required, which in turn depends on the error voltage per degree error available.

These circuits were selected as preferred circuits because of their simplicity. Since they form part of an all-ac servo, the drift due to environmental changes, input power variations, or gain changes in the amplifier is slight, and a balance control is unnecessary; the performance is adequate for most airborne computer applications. While the method of obtaining damping is unconventional, the circuit is not new and has had extensive field use in airborne fire-control equipment.

Analog computer applications of these circuits are found in section 4 below where a summing amplifier, dc and ac integrators and differentiators, and a gain-compensating servo are described. For a general discussion of analog computers, see Notes to the Preferred Circuits Manual, section 15.

2. DESIGN CONSIDERATIONS

2.1 *Instrument Servo Motor Controller:* The motor controller consists of a pentode voltage amplifier followed by a cathode follower power amplifier used to drive the control winding of a servo motor. Direct current is used in both the control and fixed phase windings to increase the motor damping and improve its performance.

(*a*) Cathode follower: The triode connected 6005/6AQ5 used as a cathode follower is capable of driving the control winding of either of the specified instrument servo motors directly. Placing the load at the cathode rather than at the plate requires increased drive, but improves the damping and minimizes the tendency of the motor to single phase, i. e., run as a single phase motor when the excitation is removed from the control winding. The added damping is not realized if the control field is placed in the plate circuit.

The circuit is capable of delivering one watt to the control winding of a servo motor, provided the effective resistance is between 2K and 4KΩ. The maximum voltage output under these conditions is about 50 volts rms at the fundamental frequency. The winding is rated for 115 volts rms, but 50 volts rms will produce

[1] The basis of selection of these Preferred Circuits is discussed in the Notes to the Preferred Circuits Manual, section 15.

75% of the rated no-load speed and 50% of the rated stall torque. The performance at maximum output would not be improved by using the 57.5-volt control winding, since the effective resistance would be reduced by a factor of four, and the impedance mismatch would be increased. Capacitor C4, whose value is usually specified by the motor manufacturer, resonates with the motor winding.

(*b*) Voltage amplifier: The voltage amplifier employs a 5840 subminiature pentode in a circuit with a gain of about 90 and negligible phase shift at frequencies in the vicinity of 400 cps. Some degeneration, which aids in stabilizing the gain, is provided by the omission of the screen bypass capacitor. A 6AU6WA may be substituted for the 5840 if a miniature tube is desired. The series grid resistor limits grid current when the error voltage is large. This resistor should be included whether the amplifier is driven directly by a synchro or is preceded by one of the preamplifiers.

2.2 *Preamplifiers:* The four servo preamplifiers (PC 71 through PC 74) have voltage gains ranging from 15 to 1200. Each is provided with a gain control, which is usually required when potentiometers are used in the follow-up system. Only a limited range exists between the gain control setting at which hunting between the potentiometer wires occurs and the setting at which the torque gain is sufficient to overcome the static friction and produce good positional accuracy. A gain control is required to set the operating point of the servo system so that it lies between the two limits described above. For applications in which the gain required in the preamplifier is only slightly higher than that provided by one of the units, the next higher gain unit is likely to operate with its gain control at too low a setting to give easy adjustment. This difficulty can be corrected by using logarithmic controls or by adding a resistor in series with a linear control in the higher gain unit.

For dc applications both the input and chopper connections are used. When the analog is an ac voltage, the chopper is not needed and R1 limits grid current during large error signals. The dc gain is different from the ac gain because the chopper does not produce an output of one volt of ac for each dc volt input.

2.3 *Servo Motor:* Direct current is used in the fixed winding of the servo motor to increase the damping and to produce a time constant which is nearly uniform over the range of control voltages. This permits a higher amplifier gain for a given peak amplitude in the closed-loop frequency response, and increases the frequency at which the peak response occurs.

The direct current in the fixed phase winding of the servo motor results in a more linear speed versus voltage characteristic, as indicated in figure 74–1 (a). As the amount of direct current in the fixed phase is increased, the initial slope of the speed characteristic decreases, but the linear portion is extended up to a 60-volt input. Over the larger part of this range the stall torque is unaffected. At inputs above 60 volts, the opposite effect occurs, and the torque is reduced more than the speed. The effect on the stall torque is shown in figure 74–1 (b).

The motor velocity constant, K_v ($K_v = \theta_{out}/V_{in}$ radians per second per volt), is proportional to the slope of the torque-voltage characteristic and to the reciprocal of the viscous damping. The reciprocal can be obtained approximately by dividing no-load speed by the stall torque for a given input voltage. In the region between 0 and 60-volt input, the slight reduction in the slope of the torque characteristic, as well as the reduction in no-load speed for a given input voltage, results in a smaller velocity constant but one which is more uniform over the range of input voltages. The amplifier gain can be increased to compensate for this reduction in the velocity constant.[2]

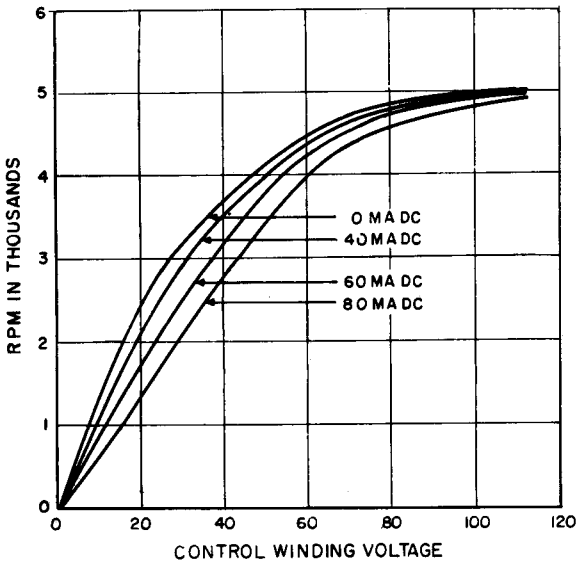
The motor time constant is proportional to the moment of inertia and to the reciprocal of the viscous damping. The moment of inertia is a constant which is unaffected by the direct

[2] The open-loop transfer function of PC 70 is of the form

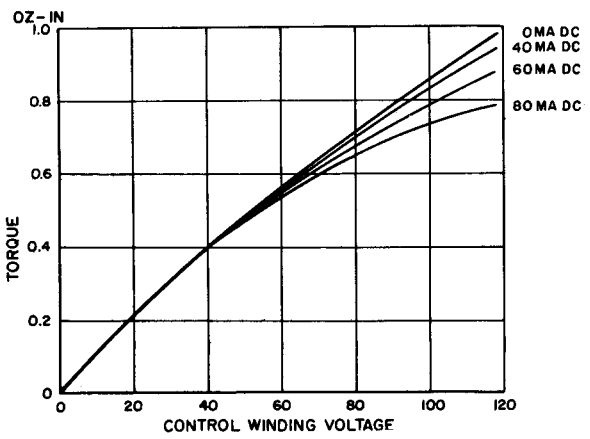
$$G = \frac{\theta_{out}}{V_{in}} = \frac{A K_v}{s(1+Ts)}$$

where A is the amplification, K_v is the velocity constant, T is the time constant of the motor, and s is the Laplace operator. Since A and K_v occur as a product, either can be increased to compensate for a decrease in the other.

current in the windings, while the effect of the direct current on the reciprocal of the damping can be determined by plotting the ratio of no load speed to torque versus control voltage. The product of this ratio and the rotor inertia is the time constant, which is plotted against control voltage in figure 74–2. The time constant over the entire range of input voltages is reduced to its approximate value at rated maximum input voltage with no direct current in the fixed winding. The frequency at which the peak of the closed-loop response occurs is increased since it is inversely proportional to the time constant. The speed of response is improved because it is very nearly proportional to the frequency of the peak closed-loop response.[3]



(a) No-load speed



(b) Stall torque

Figure 74–1—Effect of direct current in the fixed phase on the performance of an instrument servo motor

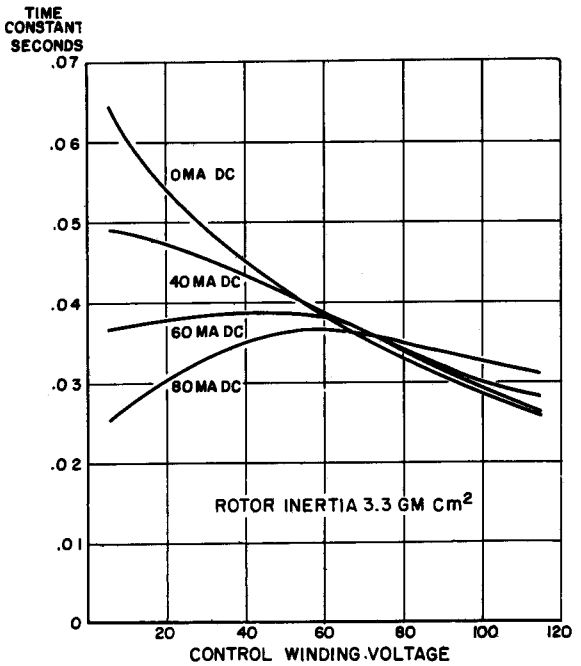


Figure 74–2—Effect of direct current in the fixed phase on the time constant of a typical instrument servo motor.

[3] When connected in a synchro loop whose output and input shaft positions are θ_{out} and θ_{in}, respectively, the closed-loop transfer function is

$$\frac{\theta_{out}}{\theta_{in}}=\frac{G}{1+G}=\frac{\frac{K}{T}}{s^2+\frac{1}{T}s+\frac{K}{T}}$$

where K is the open-loop gain including the synchros; the other symbols are defined in footnote 2. The denominator is the characteristic of the system and is of the form

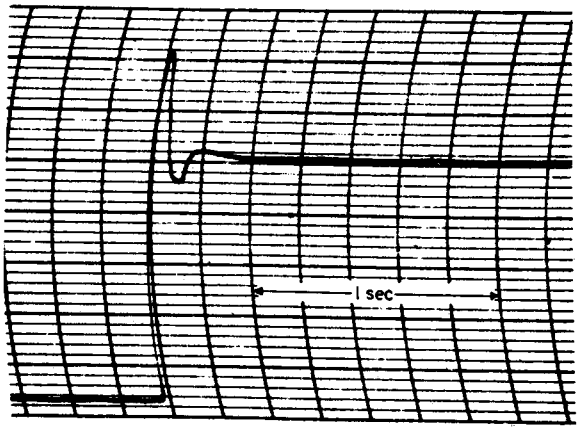
$$s^2+2\delta\omega_c s+\omega_c^2$$

where $\omega_c=\sqrt{\frac{K}{T}}$

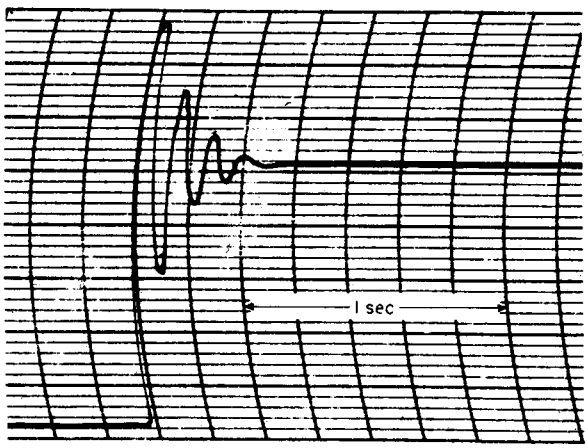
and $\delta=\frac{1}{2T\omega_c}$

from which $\omega_c=\frac{1}{2\delta T}$

The frequency at which the peak in the closed-loop response occurs is inversely proportional to the damping factor, δ, and the motor time constant, T. The damping factor is fixed by the allowable peak amplitude; therefore, for a fixed peak amplitude, ω_c is inversely proportional to the motor time constant.



(a) With dc in the fixed phase



(b) Without dc in the fixed phase

Figure 74–3—Step input response of PC 70 used in a synchro servo circuit

The response of the synchro servo circuit (fig. 74–5) to a step input is indicated in figure 74–3, which shows clearly that the damping is improved by the direct current in the fixed phase. When the direct current is removed, the decrease in the damping results in a less stable system, unless the amplifier gain is also reduced with a corresponding reduction in the speed of response.

The direct current is obtained by placing the parallel combination of CR1 and R8 (see p. 70–2) in series with the fixed phase of the motor to produce both direct and alternating current components in the winding. The circuit of figure 74–4 is suggested for determining the effects of direct current in the fixed-phase winding on the performance of the motor.

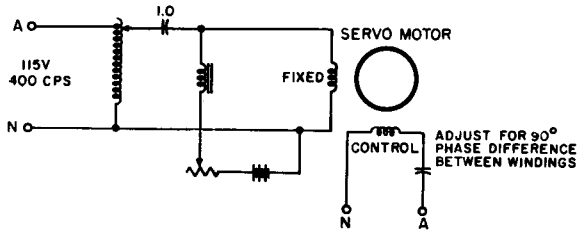


Figure 74–4—Circuit for evaluating performance of servo motor with direct current in the fixed phase

The no-load speed and stall torque are measured over the range of control voltages with the magnitude of the direct current as a parameter. The optimum amount of direct current is that which produces the most uniform time constant (fig. 74–2), and CR1 and R8 can be selected to obtain this current. CR1 must be polarized in the direction which gives symmetrical speed-versus-voltage curves for both directions of rotation. The value of R8 is best determined experimentally. A value should be chosen which will produce the desired amount of direct current without severely distorting the ac component; 750Ω is typical for servo motors of the type specified.

Preferred Circuit 70 has been used successfully with Dolecam SM071A, GM Labs 665–54–10, John Oster 15–5153–11 and 11–5101–10, and Kearfott R110 and R119 servo motors. When the effects of direct current on the performance of equivalent instrument servo motors are being determined, the extent to which the direct current heats the windings and saturates the iron should be observed.

3. PERFORMANCE

3.1 *Instrument Servo Motor Controller, PC 70:* The over-all performance of the motor control circuit depends on the servo motor used. The test data were obtained using a Kearfott R110 servo motor with a gear ratio of 72.5 to 1 from motor to follow shaft. Any of the other motors mentioned in the preceding paragraph will give similar results.

Both gain and power output vary with the effective resistance of the motor winding, but are within the limits specified, provided this resistance is between 2K and 4KΩ. The gain

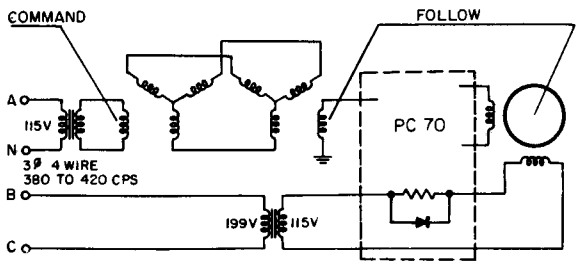


Figure 74–5—Synchro servo circuit

will vary from the nominal value by as much as ±4% because of the range in transconductance permitted by MIL–E–1/82B and MIL–E–1/13B. Simultaneous 10% changes in plate and filament supply voltages, which are additive in effect, result in a gain change of less than 4%.

For synchro retrieving, PC 70 may be connected as indicated in the synchro servo circuit, figure 74–5. With an error voltage from the synchros of 0.45 volts per degree follow error and a 72.5 to 1 gear box, a velocity constant of 160 degrees per second per degree error is obtained. This gives a frequency response which has a peak of 2 at 11 cps. The stability is not conditional, and a gain control is unnecessary.

For satisfactory performance the residual signal at null due to quadrature and harmonic components must not exceed 0.2 volts rms at the input of PC 70 or exceed 15 volts rms at the motor control winding. The gear box should have less than 0.003 inches total backlash measured at a one-inch radius on the output shaft. In addition, the friction should be low enough for the gear box and motor combination to run continuously with 10 volts on the control phase and 115 volts on the fixed phase.

3.2 *Preamplifiers PC 71 through PC 74:* The performance of the preamplifiers is specified on pages 71–2, 72–2, 73–2, and 74–2. At room temperature, the amplification will not change more than 10% from the nominal as a result of deterioration of tube performance (within MIL end-of-life limits) and 10% changes in supply voltage in the direction that causes greatest change in performance.

4. EXAMPLES OF USE

Preferred circuits 70 through 74 are suitable for computer systems in which either ac or dc voltages are used as the analogs of physical quantities. If the input analog is an ac voltage, the circuit is connected as shown in figures 74–5 ~~and~~ 74–6; differentiation and integration can be performed by employing tachometers, as indicated in the examples in sections 4.5 and 4.6. For dc applications a chopper is added as shown in figure 74–7; typical dc applications are described in sections 4.1 through 4.4.

4.1 *Summing Amplifier:* Parallel addition networks may be used as shown in figure 74–7 to obtain a shaft position which is proportional to the sum of the input voltages. The relationship between the shaft position and the input voltages is obtained by assuming that the

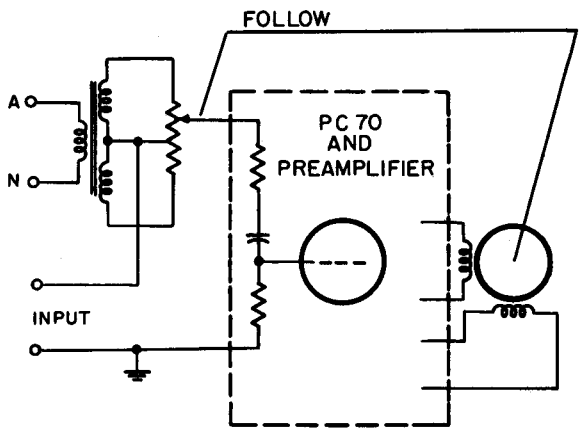


Figure 74–6—AC servo circuit

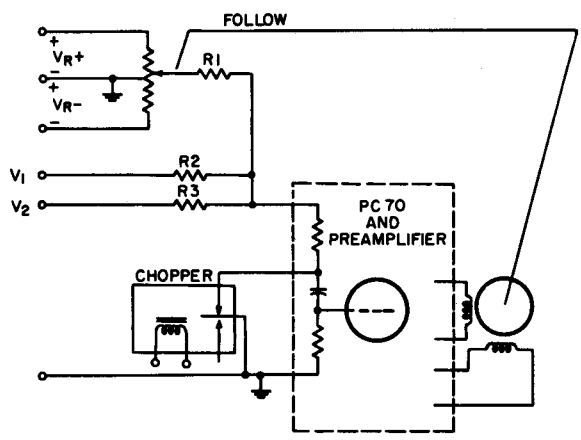


Figure 74–7—DC summing amplifier

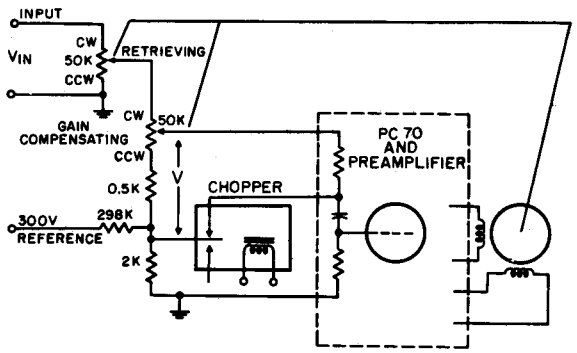


Figure 74–8—Reciprocal servo circuit

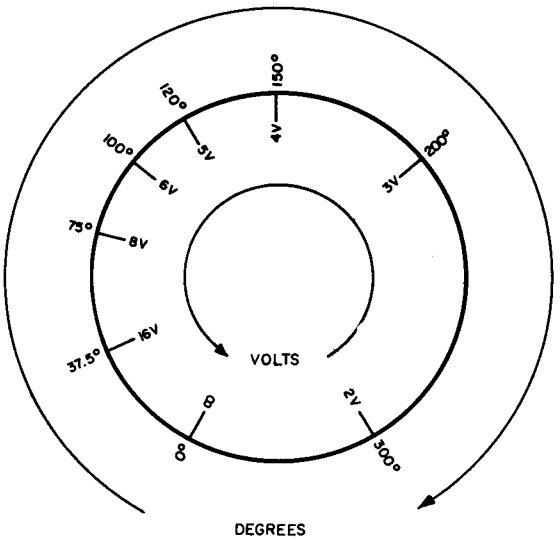


Figure 74–9—Output (degrees) of the reciprocal servo versus input (volts)

voltage at the summing junction is zero and solving for the currents at this node.

$$\theta=\frac{\theta_{max}}{V_R}\left(V_1\frac{R1}{R2}+V_2\frac{R1}{R3}\right)$$

where θ_{max} is the total possible rotation of the potentiometer shaft and θ is the actual angle of the shaft; the other quantities are identified in figure 74–7. The resistance of the potentiometer must be small compared to that of the feedback resistor, R1.

4.2 *Gain Compensated Servo:* Some servos must be gain compensated for satisfactory operation because the required servo amplifier gain varies with the magnitude of the input signal. An example of such a servo system is shown in figure 74–8; this reciprocal servo is used to obtain a follow shaft position, θ, proportional to the reciprocal of the dc input voltage, V_{in}. The relationship between the input voltage and the follow shaft position is shown in figure 74–9.

In the reciprocal servo the retrieving is accomplished by means of a linear potentiometer excited by the input voltage, V_{in}. The potentiometer wiper arm is positioned by the follow shaft. The voltage at the wiper arm is compared through the gain-compensating potentiometer with a 2-volt reference. The servo controller is arranged to position the follow shaft so that the difference between the voltage at the wiper arm and the 2-volt reference is reduced to zero.

The gain-compensating potentiometer is also a linear potentiometer, with its wiper arm positioned by the follow shaft. Without this potentiometer, the velocity constant would vary directly with the input voltage. This would result in poor positioning for small input voltages, and in hunting between potentiometer wires for large input voltages. With the gain-compensating potentiometer attenuating the error signal, V, to the servo amplifier, a uniform velocity constant is maintained as the servo approaches its correct position. This allows the servo to position accurately and stably for inputs between 2 and 100 volts.

The full counterclockwise shaft position corresponds to an infinite input voltage which requires zero amplifier gain. If the gain compensator were allowed to reduce the gain to zero, the servo would become permanently stuck when positioned at this point. This difficulty can be avoided by adding a small resistor at the counterclockwise end of the gain-compensating potentiometer. If the source from which the analog signal voltage is derived always remains proportional to the dc reference power supply from which the 2-volt reference is obtained, the output shaft position will be unaffected by variations in the dc reference voltage.

4.3 *DC Integrating Servo:* If the input analog is a dc voltage, integration can be performed by servo systems that employ frequency-sensitive feedback networks. Satisfactory performance cannot be obtained unless, in

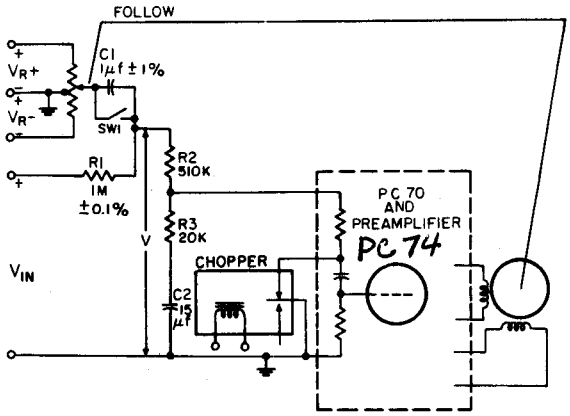


Figure 74-10—DC integrating servo

addition to the feedback network (R1, C1), another frequency-sensitive network (R2, R3, C2) is added to alter the performance of the basic motor controller. An example of such a servo system is shown in figure 74-10. This system is used to obtain a follow shaft position, θ, proportional to the time integral of the dc input voltage, V_{in}. Switch SW1 is normally closed and maintains the follow shaft in its initial position, theta equals zero. It is opened to start the integration.

The performance of the unit should be reasonably independent of the gain of the motor controller. If a low-resistance, linear retrieving potentiometer is used, and the motor controller maintains the error voltage, V, equal to zero, the following relation between θ and V_{in} exists:

$$\frac{\theta}{V_{in}}=\frac{\theta_{max}}{V_R}\left(\frac{1}{\mathrm{R1C1}s}\right)$$

$$\theta=\frac{\theta_{max}}{V_R\mathrm{R1C1}}\int_{t_1}^{t_2}V_{in}(t)dt$$

where t_2 is the time of observation of θ, t_1 is the time when SW1 was opened, and $V_{in}(t)$ is the input voltage as a function of time. The symbol s stands for the Laplace operator and may be replaced by $j\omega$ to give the steady state frequency response. It may be interpreted also as the differential operator, d/dt; hence, $1/s$ indicates integration. In an actual system an error voltage, V, different from zero is required to actuate the motor controller. For this reason, the expressions stated above do not exactly define the relationship between θ and V_{in}.

Analysis of the exact performance is simplified by referring to the equivalent block diagram, figure 74-11. In this diagram, s represents the effect of the feedback network[4] and G is the transfer function of the motor controller.

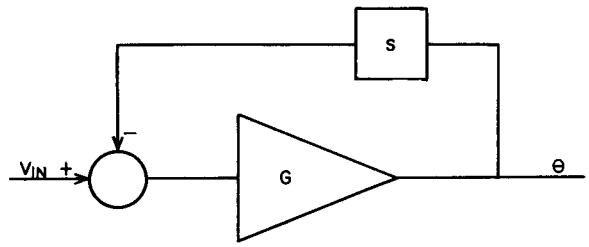


Figure 74-11—Block diagram of integrating servo

From this diagram it is evident that the relation between θ and V_{in} is

$$\frac{\theta}{V_{in}}=\frac{G}{1+Gs}=\frac{1}{s}\left(\frac{Gs}{1+Gs}\right)$$

For the preferred circuit the transfer function is of the form

$$G=\frac{AK_v}{s(1+Ts)}$$

where A is the voltage gain of the preferred circuit including the preamplifier if used, and K_v and T are the velocity constant and time constant, respectively, of the servo motor and gear box.

Combining these two equations we obtain

$$\frac{\theta}{V_{in}}=\frac{1}{s}\left(\frac{AK_v}{AK_v+1+Ts}\right)$$

and if $Ts \ll 1$

$$\frac{\theta}{V_{in}}\approx\frac{1}{s}\left(\frac{AK_v}{AK_v+1}\right)$$

Even at low frequencies where Ts is small compared to 1, the relationship is not sufficiently independent of gain and is not equal to the desired result: $\theta/V_{in}=1/s$. If the controller is preceded by an integrator to obtain

[4] In an integrator, the error signal is obtained by comparing the input with the derivative of the output.

a new transfer function G' consisting of the original G multiplied by $1/s$, the following relations will exist:

$$G' = \frac{AK_v}{s^2(1+Ts)}$$

$$\frac{\theta}{V_{in}} = \frac{1}{s}\left(\frac{AK_v}{AK_v+s+Ts^2}\right)$$

If Ts^2 and s are each much less than AK_v, then $\theta/V_{in} \approx 1/s$. In this case, the integration is sufficiently independent of changes in AK_v. For short integration periods such as are required in airborne fire-control equipment, one integration in the controller can be approximate. This can be accomplished by placing an integral network such as R2, R3, and C2 in the error signal path (fig. 74–10). In the construction of a servo integrator for a high performance inertial guidance system where integration is to extend over a long period, a second motor would probably be employed to produce the required double integration in the controller.

In the typical system shown in figure 74–10, the high gain preamplifier PC 74 is used. The potentiometer is a 10KΩ linear wire-wound unit with a total rotation of 300 degrees and a tap at the 50% resistance point. The references are plus and minus 20 volts. The output is 7.5 degrees per second for an input of 1 volt using the R110 motor and a 72.5 to 1 gear ratio.

4.4 *DC Differentiating Servo:* The servo system shown in figure 74–12 provides a shaft follow position, θ, proportional to the time derivative of the dc input voltage, V_{in}; C2 and R2 are added to filter the derivative and to improve the stability of the circuit. With the component values given in figure 74–12, satisfactory performance is obtained without adding a network to alter the basic transfer function G of the controller. The basic response [5] in this case is

$$\frac{\theta}{V_{in}} = \frac{\theta_{max}}{V_R}\,\frac{6s}{(1+0.099s)(1+0.04s)}$$

The actual response is this basic response multiplied by a factor which is similar to that given for the frequency response of the simple servo. For the reference voltages and potentiometer used, this system gives an output displacement of 60 degrees for an input of 1 volt per second when using the R110 motor and a 72.5 to 1 gear ratio.

4.5 *AC Differentiating Servo:* To obtain the derivative of an ac analog, it is only necessary to make the shaft position proportional to the ac input voltage, and drive a tachometer through a suitable set of gears from the controller output shaft. The output of the tachometer will be an ac voltage that is proportional to the derivative. The required shaft position can be obtained using the circuit of figure 74–6. Drag-cup induction tachometers are made specifically for this purpose. These tachometers are usually temperature controlled or temperature compensated to give a constant output versus speed curve. They are available with a linearity of 0.1% with speed, but the errors from changes in scale factor due to changing line voltage and frequency, uneven temperatures, etc. must be considered in determining the over-all accuracy of the system. In addition, the effects of the added inertia on the servo system and the high speed needed to get reasonable voltages must be considered in designing such a system.

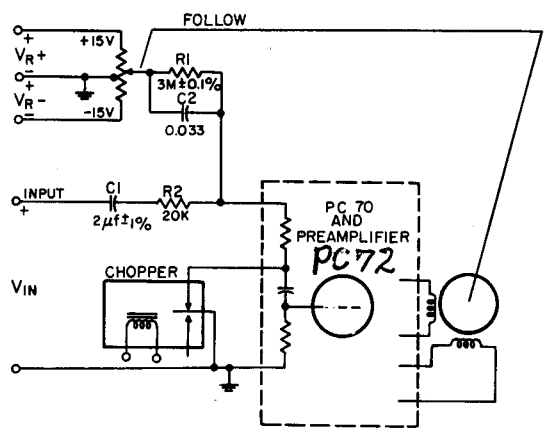


Figure 74–12—DC differentiating servo

[5] The basic response of this circuit is obtained by writing the current equations for the node at the input to the preferred circuit and assuming that the feedback network and controller act to maintain this node at ground potential. For the circuit of figure 74–12 the basic response is

$$\frac{\theta}{V_{in}} = \frac{\theta_{max}}{V_R}\left[\frac{\mathrm{R1C1}s}{(1+\mathrm{R1C2}s)(1+\mathrm{R2C1}s)}\right]$$

C1 is a polystyrene or other Low Leakage Capacitor.

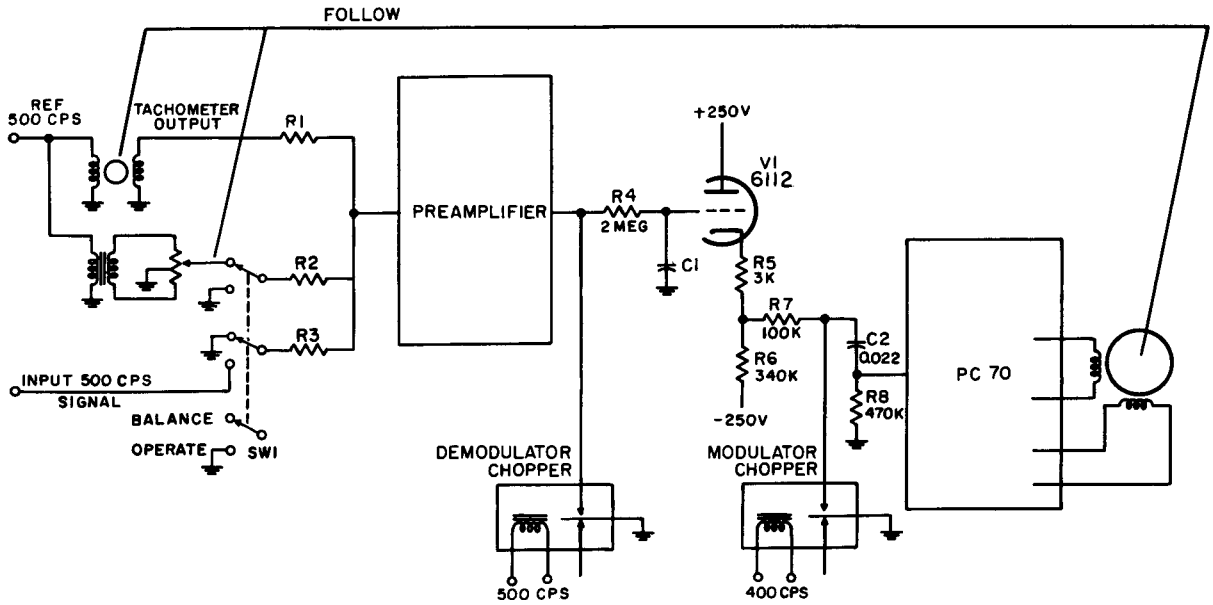


Figure 74–13—AC integrating servo

4.6 *AC Integrating Servo:* In making an integrator a tachometer may be used as the feedback element to give the required "s", as indicated in figure 74–11. In this case the needed integral network cannot be added directly. (See Sec. 4.3.) It is necessary to demodulate the errror signal, integrate in the added network, and remodulate. This procedure allows the signal frequency and the motor voltage frequency to be different. An example of such a system is shown in figure 74–13.

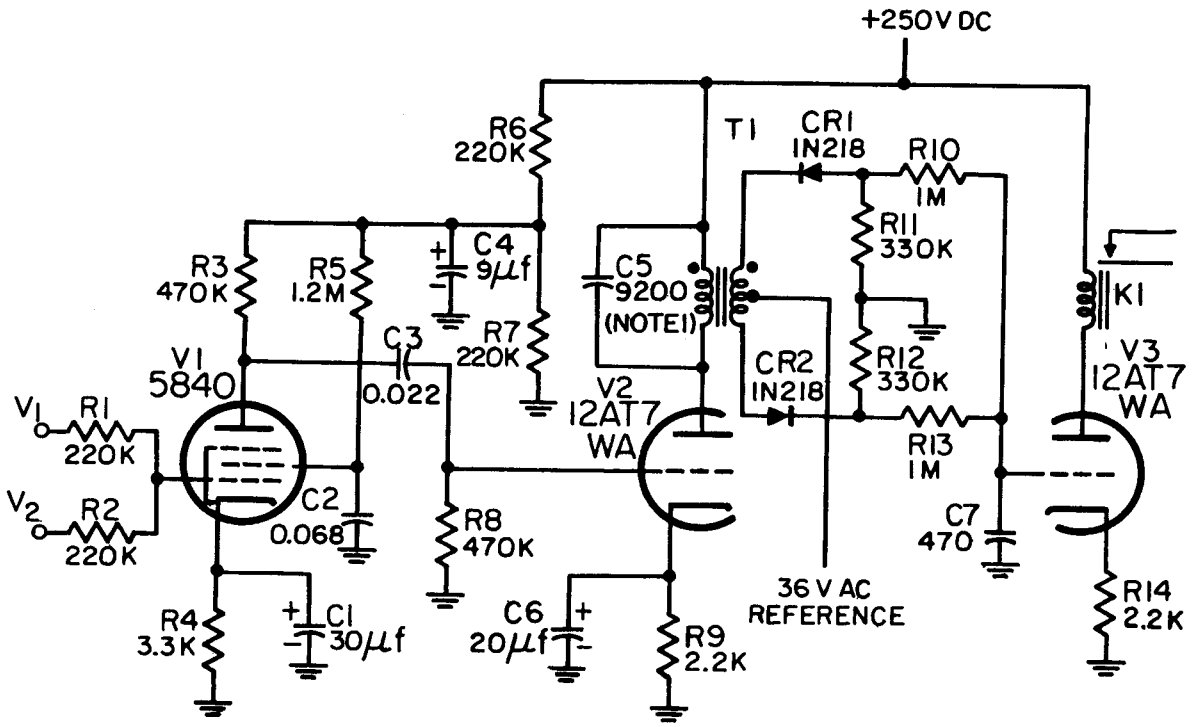
Before integration is started, SW1 is in the balance position. At this time feedback is obtained through resistor R2 from the follow potentiometer to give an initial condition of theta equals zero. When it is desired to start integrating, the position of SW1 is changed to operate. This disconnects the potentiometer feedback and connects the input voltage through resistor R3. The demodulator chopper converts the ac error signal to a dc signal, and the network R4,C1 furnishes the required approximate integration. The cathode follower V1 prevents loading this network. The modulator chopper converts the dc signal to an ac signal which, when amplified, is suitable to drive the motor. Those component values that depend on the gear ratio, scale factors, tachometer output, etc. are not given. Resistors R1 and R3 are precision resistors. For proper operation, the electrical and mechanical phase shift of the demodulator chopper must ~~produce a voltage which is in phase with the error signal~~ be small, while the modulator chopper must produce a voltage which is 90 degrees out of phase with the fixed-phase motor voltage. In some cases the addition of the tachometer will increase the system inertia to the extent that the time constant of the motor controller will be too great for satisfactory operation. In this case the filter network R4 and C1 must be replaced by a lead-lag network.[6]

[6] H. Chestnut and R. W. Mayer, *Servomechanisms and Regulating System Design*, Vol. I, John Wiley & Sons, New York, Inc., N. Y., 1951, pp. 246–269, 334–336.

NBS PREFERRED CIRCUIT NO. 78
PHASE SENSITIVE NULL DETECTOR

548679 O—60——2

NBS PREFERRED CIRCUIT NO. 78
PHASE SENSITIVE NULL DETECTOR



Components:

Relay, K1:

DC resistance: 5KΩ.

Impedance: 10KΩ or less.

Rated coil current: 2 to 4 ma.

Transformer, T1: UTC type O–7, or equivalent.

Approximate power dissipation: R1, R2, R4, R5, R8, R9, R10, R11, R12, R13: negligible; R3: 0.015 watt; R7: 0.05 watt; R6, R14: 0.125 watt.

Limits (these are not tolerances; see note 2 below): R10, R11, R12, R13: ±5%; R6, R7: ±10%; all other R: ±20%. All C: ±20%.

Operating characteristics: See Performance, sec. 3, p. 78–4.

Power requirements:

250 volts dc ±10% at 9 ma.

6.3 volts ac ±10% at 450 ma.

NOTES:

1. C5 tunes T1 at the operating frequency.

2. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.

PC 78 PHASE SENSITIVE NULL DETECTOR

1. APPLICATION

PC 78 is designed to operate a dc relay when the sum of the input currents is equal to zero (i.e., $V_1/R1+V_2/R2=0$). It finds applications in servo control circuits. Although the data are given for operation at 500 cps, the circuit can be adjusted for any operating frequency within the range 300 to 1000 cps by selection of capacitors C5 and C7.

2. DESIGN CONSIDERATIONS

PC 78 consists of an ac amplifier, a phase sensitive detector, and a relay control tube. The input currents establish an ac error voltage at the grid of V1. This is amplified and applied to the phase detector where it is combined with the reference voltage, rectified by CR1 and CR2, and applied as a dc voltage to the grid of the relay control tube, V3. The circuit is adjusted so that the change in control voltage at the grid of V3 is sufficient to actuate the relay which serves as a plate load.

The ac amplifier is straightforward in design and is similar to the one used in PC 76. The output transformer is tuned by C5 to peak the response at the operating frequency. The voltage amplification from the grid of V1 to the plate of V2 is approximately 3000.

The amplitude and polarity of the voltage output of the phase detector are determined by the amplitude of the input voltage at V1 grid and its phase with respect to the reference voltage, V_r. With the circuit connected as shown in the preferred circuit diagram, the phase detector output is positive when the input voltage is in phase with V_r and negative when it is out of phase. If a negative output voltage is desired when the input is in phase with V_r, the connections to the primary or secondary of the transformer may be reversed, or the diodes may be reversed.

If the input signal is in phase with V_r, the signal and reference voltages add during the half cycle when CR2 conducts and are opposed when CR1 conducts; therefore, the positive voltage built up across R12 exceeds the negative voltage across R11, and the phase detector output is positive. If the transformer secondary voltage on either side of the center tap is less than the reference voltage, the output voltage is proportional to the input voltage. The output reaches a maximum when the portion of the signal across one-half the transformer secondary, V_1, is just equal to V_r, in which case the net voltage across CR1 is zero while that across CR2 is twice the reference voltage. If the amplitude of V_1 exceeds that of V_r, the net voltage delivered to the RC filter remains twice the reference voltage regardless of the magnitude of V_1. This follows because the voltage across CR2 is V_1+V_r, the voltage across CR1 is V_1-V_r, and the output is proportional to the difference between the two. If the input signal is out-of-phase with V_r, the action of the circuit is the reverse of that just described, and the output voltage is negative.

The output of the phase detector is applied to the grid of the relay control tube through a filter consisting of R10 and R13, and C7. C7 must be adjusted to give the desired performance. Increasing the capacitance increases the delay but improves the ac filtering and reduces the danger of switching at the wrong time when the inputs are noisy signals.

Without C7, the dc grid voltage is approximately equal to $2\alpha V_1/\pi$ when $V_1 < V_r$ and approximately equal to $2\alpha V_r/\pi$ when $V_1 \geqq V_r$. As the capacitance of C7 is increased, the grid voltage approaches the peak value of the sine wave, $2\alpha V_1$ or $2\alpha V_r$.

In the above

V_1 = peak value of voltage across one-half of secondary winding of transformer.

V_r = peak value of reference voltage applied between ground and the center tap of transformer.

$\alpha = \alpha_1 = \alpha_2$

$$\alpha_1 = \frac{R12+R13}{R10+R12+R13} \quad (CR1 \text{ conducting } r_{d1} << R11)$$

$$\alpha_2 = \frac{R10+R11}{R10+R11+R13} \quad (CR2 \text{ conducting, } r_{d2} << R12)$$

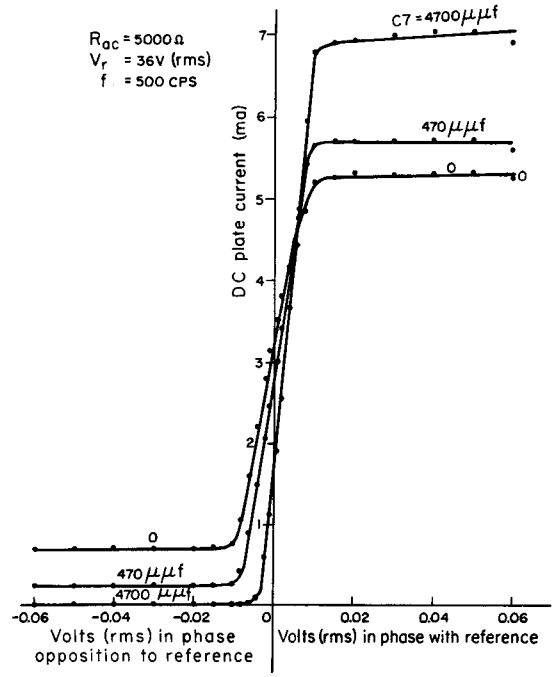
r_d = diode forward resistance.

In the absence of input and reference signals, the quiescent plate current of the relay control tube is established by the cathode bias. The ac component of the reference signal has an effect on the quiescent plate current if it is large enough to cut off the plate current during a portion of the cycle. This is a function of the ac load presented to the tube by the relay and also of the amplitude of the reference signal and the size of capacitance C7, as indicated in figure 78–1. For a given ac load, the amplitude of the reference signal and capacitance C7 should be adjusted to obtain the desired performance. The quiescent plate current of the relay tube should be the current required to actuate the relay, and the plate current swing should be sufficient to assure positive operation. An upper limit to the size of C7 is set by the permissible time delay.

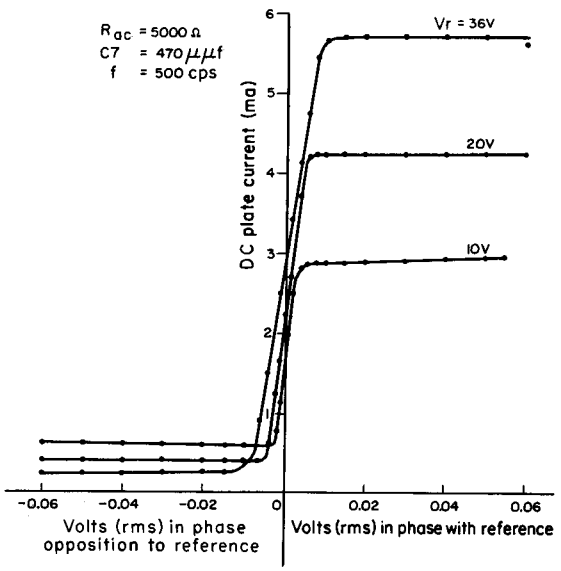
3. PERFORMANCE

Figure 78–1 shows the static performance curves of PC 78 which were obtained by applying a 500 cps voltage at the grid of V1 and measuring the plate current of V3 for values of input grid voltage in-phase-with and in-phase-opposition-to the reference voltage. A 5000 ohm resistor was substituted for relay K1 during these measurements. Two sets of curves are given with C7 and reference voltage as running parameters. Either or both of the parameters may be adjusted to give the desired performance. Using the 36-volt reference and a 470 $\mu\mu$f capacitance for C7, the switching time for a change in input signal from -0.02 volts to $+0.02$ volts is about 0.03 seconds using an Allied Control RSHX–83 relay.

Tube changes and supply voltage variations have negligible effect on the functioning of the circuit.



(a) Effect of filter capacitor C7 on performance.

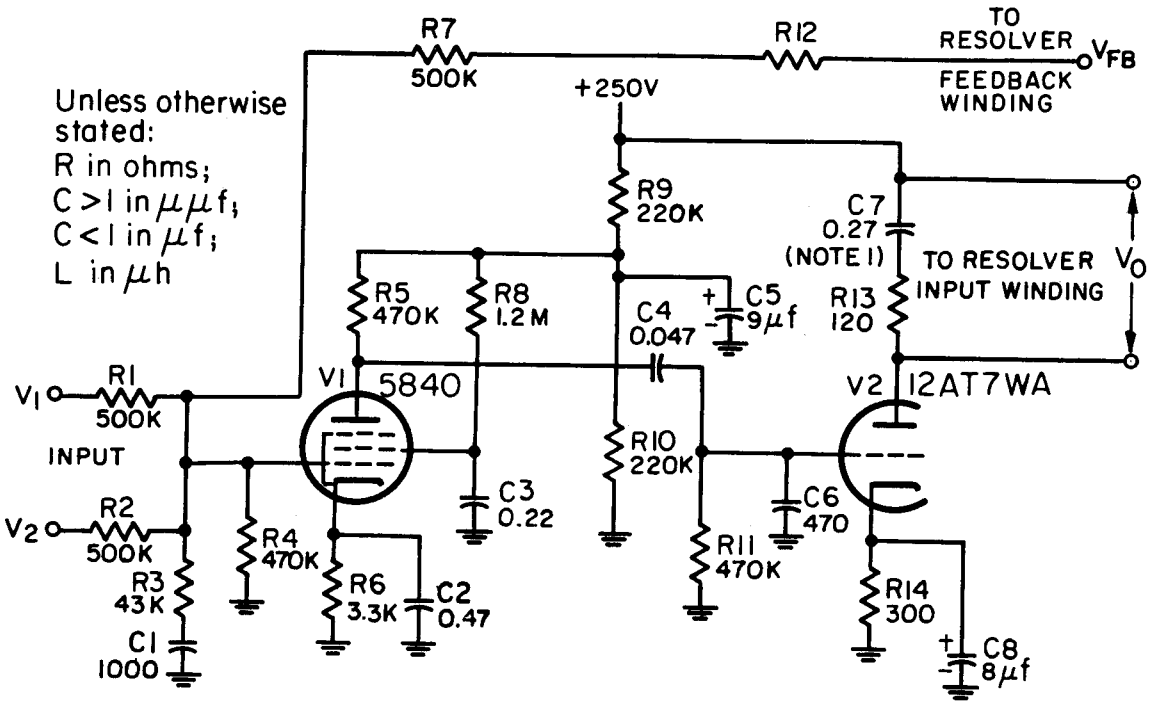


(b) Effect of reference voltage on performance.

Figure 78–1.—Static performance of PC 78.

NBS PREFERRED CIRCUIT NO. 79
RESOLVER DRIVER

NBS PREFERRED CIRCUIT NO. 79
RESOLVER DRIVER



Components:

R1, R2, R7: The relative stability must be such that the ratio R7/R1 and R7/R2 does not change more than 0.05%.

R12=[1/300+(1−a)] R7, where a is the resolver transformation ratio.

R3,R4,R6,R12: ±5% limits; R9,R10: ±10% limits; all other R: ±20% limits.

C1,C2,C7: ±5% limits; all other C: ±20% limits. (Note 2)

Operating characteristics:

$$V_o \approx -\left(V_1 \frac{R7}{R1} + V_2 \frac{R7}{R2}\right)$$

Maximum output (5% distortion): 50 volts rms.

Stability: (Note 3)

	Lower	*Upper*
Amplification margin	14 db	12 db
Phase margin	50°	60°

Power requirements:

250 volts dc ±10% at 8.7 ma.

6.3 volts ac ±10% at 450 ma.

(For Notes, see next page)

NOTES:

1. The values of C7 and R13 are determined by the operating frequency and by the resolver used. Values shown are for the Mark 4 Mod 0 resolver operating at 500 cps. (See sec. 2.2.)

2. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.

3. Amplification and phase margin were measured with both inputs open and with the combination of tube characteristics and supply voltages which resulted in the highest value of forward amplification.

PC 79 RESOLVER DRIVER

1. APPLICATION

PC 79 was designed to drive an ac resolver having compensating windings. It is an ac operational amplifier used as an isolation amplifier and employing feedback which includes the compensating winding of the resolver. With the resolver, it is useful as a computing element in problems involving coordinate conversion, coordinate rotation, and resolution of vectors when accuracies of 0.5 percent are sufficient. The component values given (p. 79–2) are for operation at 500 cps; operation at other frequencies requires change in six component values. (See section 2.2.)

2. DESIGN CONSIDERATIONS

Compensated resolvers are readily available with a functional accuracy of ± 0.1 percent. The use of a compensating winding for the feedback places the resolver excitation loss in the feedback loop. This results in a low over-all phase shift and a constant amplification, even when the resolver copper loss changes with temperature. In addition, by proper loading of the feedback winding, the effects of any load on the rotor can be compensated.

If the resolver is to be operated at a frequency other than 500 cps, the values of C1, C2, C7, R3, R6, and R13 must be changed. In addition, the values of C7 and R13 are a function of the input impedance of the resolver. When long leads are employed between the amplifier and the resolver, and/or when the trimming resistor, R12, is included in the resolver, the resistors R1, R2, and R7 should be changed to 100KΩ. In this case, R4 should also be 100KΩ, R3 8.2KΩ, and C1 5000$\mu\mu$f.

2.1 *Feedback*: An open loop amplification [1] of 300 is obtained by adjustment of the passive feedback network between the resolver compensating winding and the grid of V1. The only component of this network that is not determined by other considerations is the grid return of V1, since the values of the input and feedback resistances (R1, R2, R7, and R12) are determined by the application of the circuit. If the desired result were achieved by the selection of the value of R4 alone, the amplitude response would fall to unity at a frequency of 7500 cps or above, with the risk that additional stray capacitance might cause the circuit to oscillate at a frequency near this point.

The lag network, R3,C1, shapes the response so that the desired amplitude and phase characteristics are obtained. The equivalent circuit for the lag network, together with its amplitude and phase characteristics, is shown in figure 79–1. The desired response is obtained by choosing values for R3 and C1 that will cause only a small phase shift at the 500 cps operating frequency and at the upper crossover frequency of 7500 cps (the frequency at which the open loop amplification would be 1 if the amplification fell off at a constant rate of 12 db per octave). As a result of the lag network the amplification falls to 1 at about 7500 cps with a total phase shift of 120° using nominal tubes and supply voltages. (Fig. 79–3.)

Trimmer resistor R12 is used to compensate for the finite amplification of the amplifier and for the transformation ratio of the resolver compensating winding when it is less than 1. By proper selection of the trimmer resistor, the output to the resolver can be made almost exactly equal to the sum of the input voltages (assuming that the input and feedback resistors are equal).

If the transformation ratio of the resolver is 1 and R12 is zero, the output of the amplifier (input to the resolver) is

$$V_o = -\left(\frac{V_1}{R1} + \frac{V_2}{R2}\right) R7 \left(\frac{A'}{1+A'}\right)$$

[1] The open loop amplification is defined as the amplification around the complete loop from any point in the circuit back to the same point; for instance, from amplifier input back to amplifier input again.

where $A'=300=\frac{R_p}{R7}A$=open loop amplification defined in footnote 1.

A=voltage amplification between V1 grid and V2 plate

R_p=the parallel combination of R1, R2, R7, and the input impedance of the amplifier.

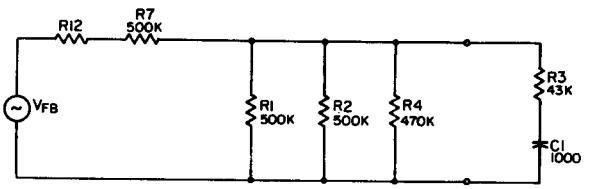
If R7 is now increased one three-hundredth by making R12=R7/300, R_p will be changed very little and $A'/(1+A')$ remains $300/301 \approx 299/300$. The output of the amplifier is now

$$V_o=-\left(\frac{V_1}{R1}+\frac{V_2}{R2}\right)\frac{301}{300}R7\frac{299}{300}$$

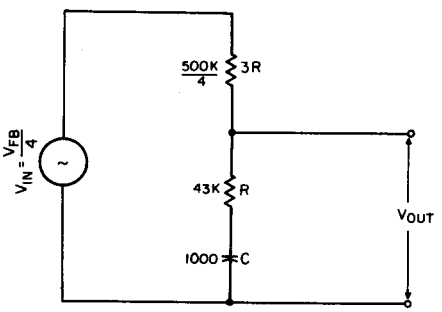
$$=-\left(V_1\frac{R7}{R1}+V_2\frac{R7}{R2}\right)\frac{300^2-1}{300^2}$$

The error has been reduced from 1/301 to about $1/300^2$. The compensation for the finite amplification of the amplifier has no effect on the stability of the amplification with changes in the open loop amplification, A'. In either case the open loop amplification would have to decrease 23% to cause a 0.1% decrease in the output voltage.

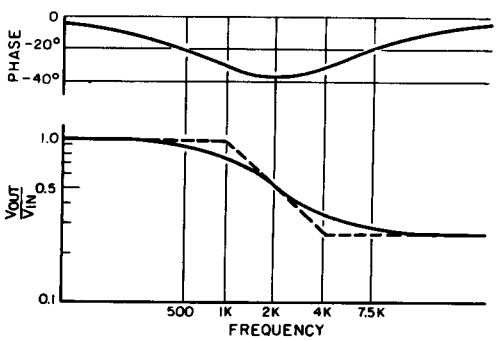
For a resolver transformation ratio of 1, R12 should be 1.6KΩ when R7 is 500KΩ, and 330Ω when R7 is 100KΩ. When the transformation ratio is less than 1, R12 must also increase R7 by the percentage that the transformation ratio is less than 1. For a transformation ratio of 0.98, R12 must be increased by an additional 2% of R7 to give R12=12KΩ when R7=500KΩ, and R12=2.4KΩ when R7=100KΩ. R12 need not be a precision resistor since its resistance is only a very small percent of the total feedback resistance. When a number of resolver drivers are to be used interchangeably with several resolvers, the usual procedure is to make the trimmer resistor a part of the resolver. The resolvers must be trimmed individually because even a 0.01 difference in transformation ratio can change the required trimmer resistance by 100%.



(a) FEEDBACK CIRCUIT



(b) EQUIVALENT CIRCUIT



(c) AMPLITUDE AND PHASE CHARACTERISTICS

Figure 79–1.—Effect of lag network, R3,C1, on phase and amplitude response.

2.2 *Amplifier:* The amplifier circuit is basically an ac operational amplifier with minor modifications to adapt it to the resolver load.

Capacitor C7 and resistor R13 are used to obtain a unity power factor load with a Q of approximately 4 at the operating frequency. The given values of C7 and R13 (see preferred circuit, p. 79–2) are for the Mark 4 Mod 0 resolver operating at a frequency of 500 cps. For other resolvers and/or for other operating frequencies, values must be calculated to obtain the Q of 4 and unity power factor at the operating frequency for the inductance and resistance of the resolver in use. Placing the

loading resistance in the capacitive branch of the circuit produces a phase response which reaches a maximum of less than 90° at a frequency about a decade above the operating frequency and then drops back to 0°. This lessens the possibility that additional stray capacitance at the higher frequencies will cause instability.

The cathode bypassing of V1 is ineffective at frequencies lower than 100 cps. This reduces the stage amplification by a factor of 4 at low frequencies and minimizes the possibility of low frequency oscillations. The value of the bypass capacitor, C2, is selected so that the angular frequency (1/R6,C2) is 0.2 of the operating frequency. The over-all effect on the phase response of the stage is similar to that of a lead network (fig. 79-2). The phase lead is about 20 degrees at the operating frequency, increases to a maximum of about 40 degrees between one

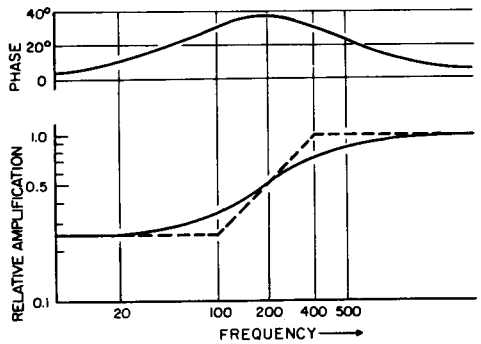


Figure 79-2.—Effect of cathode bypass capacitor, C2, on the phase and amplitude response of the first amplifier stage.

and two octaves below the operating frequency, and then falls to less than 10 degrees at the lower crossover frequency. The 20 degree lead at the operating frequency is offset by the 20 degree lag caused by the lag network, R3,C1.

3. PERFORMANCE

PC 79 was tested with the Norden-Ketay 105D2K size 15 resolver, and with minor modifications can be used with the American Electronics IR15W4-405 size 15 resolver. PC 79 can also be used with the American Electronics IR11W4-103 size 11 resolver, if R13 is changed to 240Ω and C7 is changed to 0.16μf.

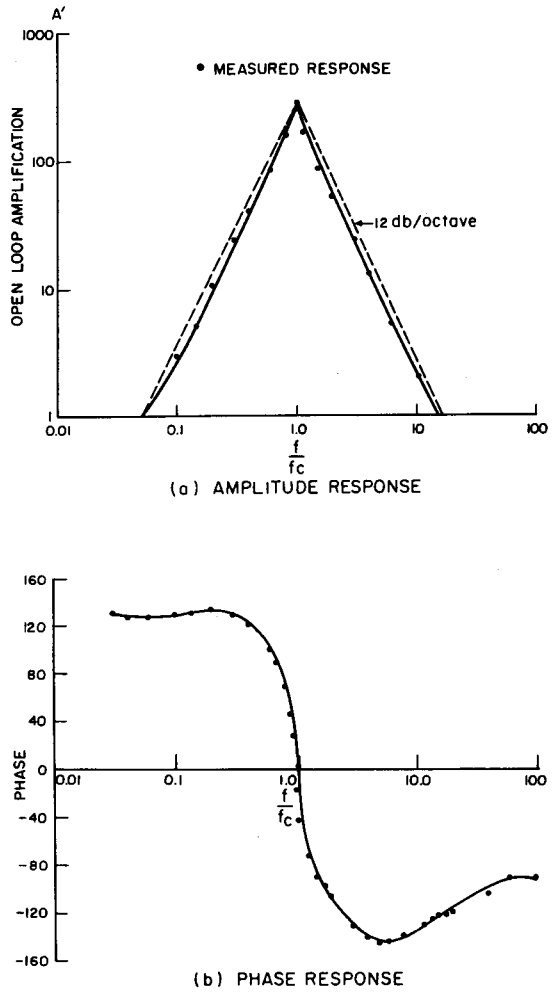


Figure 79-3.—Open loop characteristics of PC 79.

3.1 *Frequency Response:* The open loop amplification was measured by breaking the circuit at the connection to the feedback winding, inserting a signal in series with the feedback resistors, R7 and R12, and measuring the output across the resolver feedback winding. Both inputs were grounded during this measurement, representing the condition when voltage sources are connected to inputs V_1 and V_2. This is also the condition for the lowest value of open loop amplification using nominal components and voltages.

Figure 79-3 is a Bode diagram of the open loop amplification obtained under the above conditions; figure 79-4 shows the closed loop response. In the latter figure, the solid circles

show the measured values of the factor A′/(1+A′); the open circles are values calculated using the values of A′ obtained from figure 79–3. At frequencies of about 0.75 and 1.4 times the carrier frequency, the open loop amplification A′ is down by a factor of 2 and distortion appears in the output at high signal levels. These frequencies are well outside the normal operating range of the amplifier. Capacitor C4 is the principal contributor to the low frequency peak, while C6 and R13 account for the rise in the response at the higher frequencies. Decreasing the resistance of R13 increases the amplitude of the peak. Shielded leads between the amplifier and the resolver contribute little to the peaks.

The gain and phase margins were measured with both inputs open, and with the combination of tubes and supply voltages that resulted in the highest forward amplification. The errors, on the other hand, were determined for the lowest forward amplification by using tubes which had reached the minimum end-of-life transconductance permitted by MIL–E–1 and supply voltages which were 10% low. At the operating frequency, the forward amplification was reduced 37.5% by the low limit tubes and an additional 12.5% by the low supply voltages. The resulting change in the open loop amplification from both causes was calculated to be 0.35% based on a 50% change in a nominal open loop amplification of 300. Since the resolver accuracy is 0.1%, applications of PC 79 are limited to those in which 0.5% accuracy is sufficient.

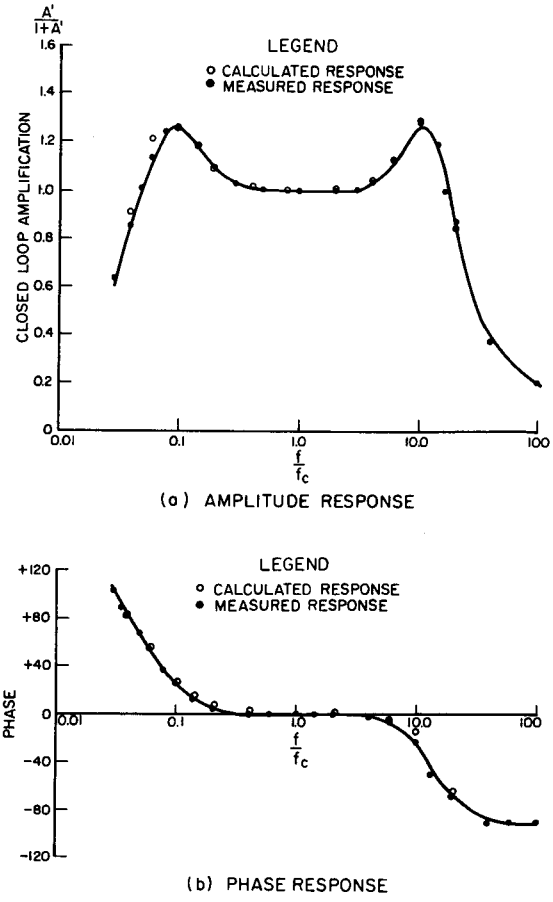


Figure 79–4.—Closed loop characteristics of PC 79. A Mark 4 Mod 0 resolver was used to complete the feedback loop.

3.2 *Error and Null Voltages:* The output of the resolver when compared with the input gives the performance indicated in figure 79–5. The comparison was made using the preferred circuit with voltage applied to input 1, with input 2 grounded, and with maximum coupling between stator and rotor. Under these conditions the input and output voltages are theoretically equal. The deviation of the output from the input is partly static error as a result of manufacturing tolerances and partly due to quadrature and harmonic components which are present even at null. The amplitude of these errors is a function of the resolver input voltage and may be the determining factor in selecting the operating voltage of the resolver. The solid lines in figure 79–5 are for the nominal operating frequency of 500 cps, and the dashed lines are for 475 cps. The curves given are for the 105D2K resolver; the results for other resolvers will differ.

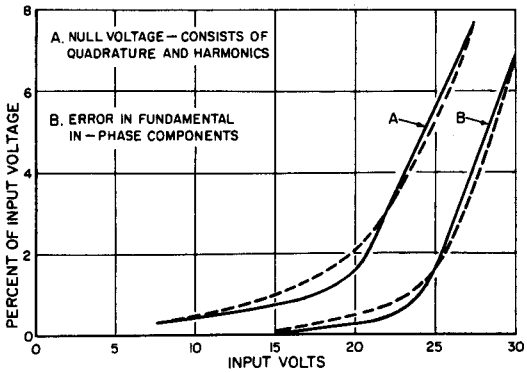


Figure 79-5.—Performance of PC 79 used with a Mark 4 Mod 0 resolver operating at 500 cps. The dashed curves show the effect of a 5% decrease in input frequency.

502632 O-59-2

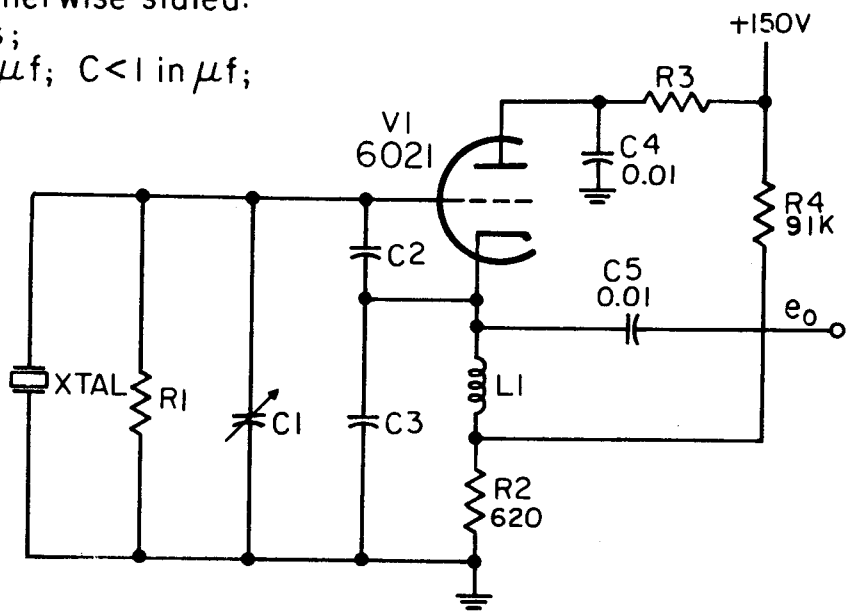
NBS PREFERRED CIRCUIT NO. 101

0.8 to 20 MC COLPITTS CRYSTAL OSCILLATOR

NBS PREFERRED CIRCUIT NO. 101

0.8 to 20 MC COLPITTS CRYSTAL OSCILLATOR

Unless otherwise stated:
R in ohms;
C > 1 in $\mu\mu$f; C < 1 in μf;
L in mh



Component data:

Preferred crystal types: CR–18/U, CR–36/U. (See Note 1.)

Frequency range mc	R1 Ω	R3 Ω	C1 $\mu\mu$f	C2 $\mu\mu$f	C3 $\mu\mu$f	C1′	C2′	C3′	L1 mh
						Distributed "C" $\mu\mu$f (See Note 2)			
0.8–5	560K	33K	10.7	15	100	6.3	2	12.5	7.0
3–11	47K	39K	12.4	15	33	6.3	2	12.5	0.8
5–20	33K	33K	8.4	24	24	6.3	2	12.5	0.3

R2, R4: ±10% limits; R1, R3: ±20% limits. C1, C2, C3: ±10% limits; C4, C5: ±20% limits, or guaranteed minimum value. (See Note 3.)

Power requirements:

150 volts dc at 4 ma (plate supply); 6.3 volts at 300 ma (heater supply).

Operating characteristics:

For output voltage and crystal dissipation as a function of crystal resistance, frequency, and oscillator tube transconductance, see figures 101–1 through 101–3. (See Notes 4 and 5.)

Factors affecting absolute frequency accuracy:	*CR–18/U* *ppm*	*CR–36/U* *ppm*
(a) Manufacturing tolerance (within temperature range)	50	20
(b) Frequency correlation (See Note 6)	10	10
(c) Frequency stability for 10% change in plate and heater voltage	<3	<3
(d) Frequency variation for a 10% change in a single capacitor	<8	<8
(e) Frequency variation for a 20% change in a single resistor	<1	<1

(For Notes, see next page)

NOTES:

1. CR-36/U is a temperature-controlled unit. (See MIL-C-3098B.)

2. The distributed capacitance values shown are typical of those obtained by use of conventional wiring in the test units. Lead dress, tube sockets versus direct lead soldering, etc., will cause these values to vary; therefore, they should be checked and the lumped capacitors C1, C2, and C3, shown in the circuit diagram, changed to keep the total capacitances the same as listed, i.e., the sum of C2+C2′ to remain constant. In most cases adjustment of C1 to keep C_t (defined in section 2.1) equal to 32 $\mu\mu$f will be satisfactory. Note that C3 is paralleled by 15 $\mu\mu$f of load capacitance.

3. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.

4. The crystal drive equals I^2R_e where I is the rms current through the crystal, and R_e is the crystal resistance as measured in the appropriate crystal impedance meter. (See MIL-C-3098B.) The current through the crystal can be equated to the current through the 32 $\mu\mu$f of capacitance which is in parallel with the crystal, since the crystal circuit is high Q. The current through the 32 $\mu\mu$f is E/X_c where E is the rms voltage across the crystal, and X_c is the capacitive reactance of 32 $\mu\mu$f at the operating frequency. The crystal drive therefore equals $(E/X_c)^2R_e$.

5. The output voltage is measured with a load of 10KΩ paralleled by 15 $\mu\mu$f.

6. Frequency correlation is defined as the difference between the circuit operating frequency (operating at 25° C with circuit values as shown in the diagram) and the antiresonant frequency of the crystal unit as measured in the appropriate crystal impedance meter. (See MIL-C-3098B.)

PC 101 0.8 to 20 MC COLPITTS CRYSTAL OSCILLATOR

1. APPLICATION

PC 101 provides the designer with a stable frequency source of minimal complexity. Operation at any frequency in the 0.8 to 20 mc range may be accomplished by substituting different crystals on a plug-in basis, with no retuning required. The twin-triode 6021 provides a triode section for use as a mixer, buffer, and/or frequency multiplier. Use of a single or twin-triode miniature or subminiature equivalent requires changes in the lumped capacitances to compensate for changes in tube and distributed capacitances. The electron-coupled pentode circuit of PC 102 should be used to obtain higher output, immunity from the effects of load changes, greater harmonic content, and better frequency correlation. However, this will increase circuit complexity, and may increase the physical size of a unit due to the use of a single tube per envelope.

2. DESIGN CONSIDERATIONS

2.1 *Symbols:*

(*a*) P_x: Power dissipated in the crystal unit, or crystal drive level.

(*b*) C_t: The total grid to ground capacitance, due to C1, C2, C3 and associated distributed and stray capacitance.

(*c*) R_t: The total crystal circuit resistance consisting of the sum of the crystal resistance as measured in the appropriate crystal impedance meter and the additional resistance connected in series with the crystal to simulate a higher resistance crystal.

2.2 *Crystal Circuit:* The crystal equivalent circuit consists of a very large inductance (in the order of henries), in series with a very small capacitance (in the order of hundredths of a micromicrofarad) and a resistance ranging from a minimum of 5 ohms at the high-frequency end of the circuit range to a maximum of 1000 ohms at the low-frequency end. In addition, due to the crystal holder, etc., there is a small capacitance in the order of 5 $\mu\mu$f[1] in parallel with the crystal. In the Colpitts circuit, the crystal operates at a frequency higher than the series resonant frequency (which is determined by the constants of the series arm alone) and lower than the parallel resonant frequency [2] (which is a function of the parallel capacitance and the inductance of the crystal together with the external parallel capacitance). This total external parallel capacitance is a fixed value for any given MIL crystal. The crystal, together with the associated parallel circuit capacitance, acts as an inductance whose effective reactance varies very rapidly with changes in frequency. The oscillator circuit adjusts its frequency so that the effective reactance of the crystal at the operating frequency is just enough for the loop gain to be 1 with a phase shift of 180° between input voltage (grid-cathode) and output voltage (plate-cathode). The crystal is tested for antiresonance with 32 $\mu\mu$f of external parallel capacitance. This specification allows the user to design a circuit which will oscillate at a frequency close to the antiresonant frequency of the crystal. In general, this frequency correlation should be better than 10 parts per million. The antiresonant frequency of the crystal can differ from the frequency stamped on the crystal holder by a maximum number of parts per million as specified in MIL-C-3098B for the particular crystal involved. This maximum deviation includes the combined effects of manufacturing tolerance and temperature coefficient within the temperature range for which the crystal is designed.

The effective series resistance of the crystal is a measure of the "activity" of the crystal. It is a controlling factor in the determination of output-voltage amplitude and crystal dissipation.

2.3 *Oscillator Configuration:* A Colpitts grounded plate circuit was chosen because it

[1] The maximum value of this capacitance is set by MIL specifications as 7 $\mu\mu$f.

[2] The parallel resonant frequency referred to is that frequency for which zero phase shift is measured when the crystal is inserted in the specified crystal impedance meter. (See MIL-C-3098B.)

allows frequency changing on a crystal plug-in basis, with greater stability and better frequency correlation than provided by the nearest alternative, the Miller oscillator. Use of the Colpitts circuit, however, results in sacrifice of output amplitude for the same magnitude of crystal dissipation obtained with the Miller oscillator.

The Colpitts oscillator is difficult to start when used with high resistance crystals. Adjustment of the capacitor voltage divider C2, C3 to insure starting tends to reduce output voltage or increase crystal dissipation. These effects can be mitigated by providing an initial negative bias to the oscillator tube. This negative bias reduces grid loading during initial oscillator buildup and allows oscillator operation with a more favorable capacitor divider ratio. The capacitor C1 in many applications is composed mainly of lead and switch capacitances when switches are used for frequency changing.

The voltage divider R2,R4 provides the initial bias to the oscillator tube. This circuit also increases frequency stability. The oscillator circuit without this fixed bias will experience a larger change in frequency as a function of a given change in plate voltage than will this circuit with a fixed bias. The improvement in frequency stability is an added advantage obtained from the use of a fixed bias. The mechanism involved is the reduction in the plate resistance of the tube with an increase in supply voltage which is counteracted by the increase in plate resistance caused by the increase in bias across the bias network R2, R4.

The choke L1 keeps the oscillator output from being loaded by the cathode resistor. It is chosen of sufficient size to resonate with C3 at a frequency lower than half the lowest frequency of the particular band in use. This insures negligible inductive effect on the capacitor divider C2, C3.

The range of crystal resistances allowed by MIL–C–3098B appears to be much wider than necessary in view of present manufacturing techniques. Because of this wide range, design compromises must be made in order to insure operation of the circuit with the entire range of crystal resistance allowed by specifications and yet keep crystal dissipation within the recommended limits.[3]

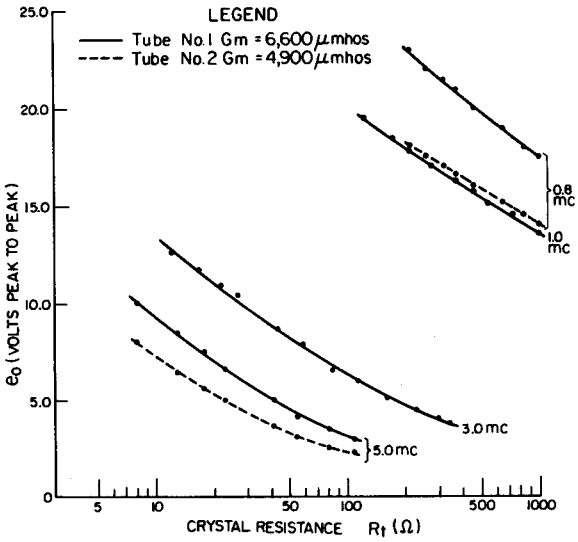
2.4 *Oscillator Tube:* The 6021 twin-triode has a medium μ (35) and sufficient transconductance (5400 μmhos) for use as the oscillator stage and as a buffer or frequency multiplier stage. It is a MIL preferred tube and is frequently used in associated circuits in the same type of equipment as would employ PC 101, thus allowing for a reduction of tube types in an equipment.

3. PERFORMANCE

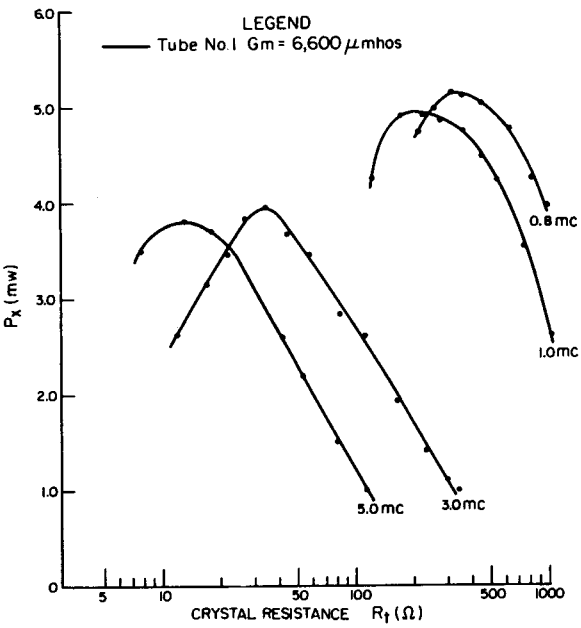
3.1 *Output Voltage Amplitude and Crystal Dissipation:* Figures 101–1 through 101–3 are graphs of output voltage and crystal drive level versus crystal resistance for the three frequency bands of PC 101. All voltages shown are peak to peak as measured on an oscilloscope. Typical waveforms for the frequency extremes of PC 101 are shown in figure 101-4. The essentially sinusoidal waveform of the higher frequency output is due to the lowered impedance of the RC load (10KΩ in parallel with 15 $\mu\mu$f) at these frequencies.

Because limit crystals were not available, the performance data were plotted using the lowest resistance crystals available and simulating higher resistance units by adding resistance in series with the crystal. The circuit used in making the measurements is shown in figure 101–5, where R_x is the added resistance. The validity of this simulation technique was checked by making measurements on two crystals, one a low resistance and the other a high resistance crystal. Resistance was added to the low resistance crystal to bring its resistance up to that of the high resistance unit, and the operation of the two crystals was compared in the test circuit of figure 101–5. The output voltage and computed crystal dissipation checked within 5%. Further checks were

[3] There is no restriction on crystal drive in MIL–C–3098B. These specifications serve merely to delineate acceptance test procedures. Recommended operating limits for crystals in military equipment are listed in section II of WADC Technical Report 56–156, ASTIA Document No. AD 110448, "Handbook of Piezoelectric Crystals for Radio Equipment Designers," Oct. 1956.



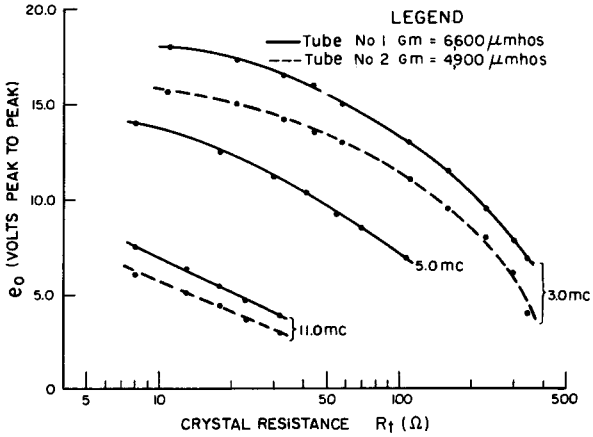
(a) Output voltage.



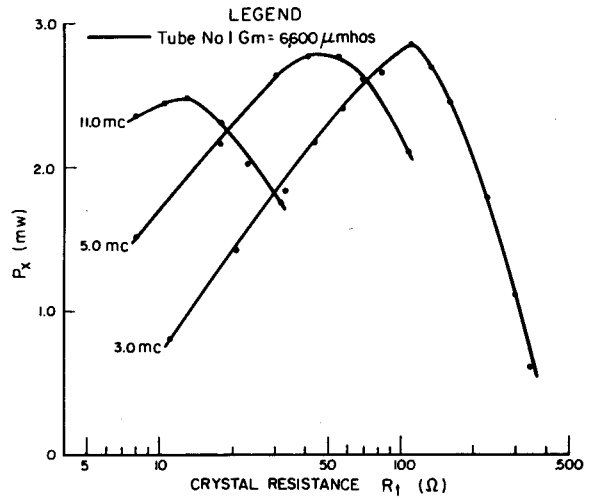
(b) Crystal dissipation.

Figure 101-1.—Operating characteristics as a function of crystal resistance, frequency, and tube transconductance for the low frequency band (0.8 to 5.0 mc).

made by inserting a crystal with a resistor in series with it in the appropriate crystal impedance meter (see MIL-C-3098B). The readings erred on the pessimistic side, i.e. the readings were higher than would be expected to result from the addition of the crystal and external



(a) Output voltage.

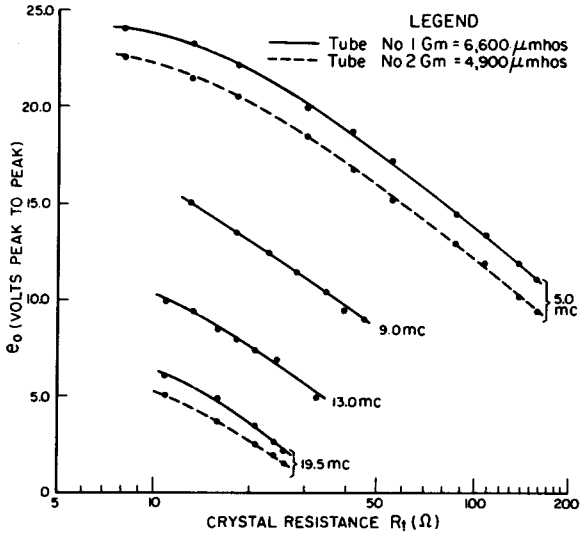


(b) Crystal dissipation.

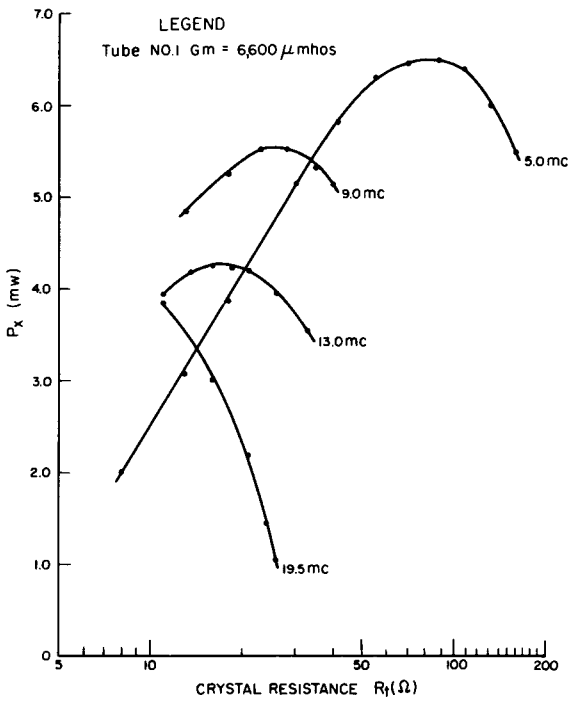
Figure 101-2.—Operating characteristics as a function of crystal resistance, frequency, and tube transconductance for the middle frequency band (3.0 to 11.0 mc).

resistance values. Here again the difference was less than 5%.

In the tests discussed above, the results of which are shown in figures 101-1(b), 101-2(b) and 101-3(b), all dissipation curves go through a peak, except at the high end of the high-frequency band. The peak indicates that the use of lower resistance crystals than were obtainable for these measurements will not result in greater than maximum recommended crystal dissipation (see footnote 3) at any frequency, with the possible exception of the high end of the high-frequency band.

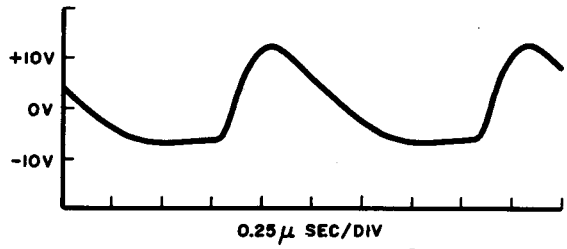


(a) Output voltage.

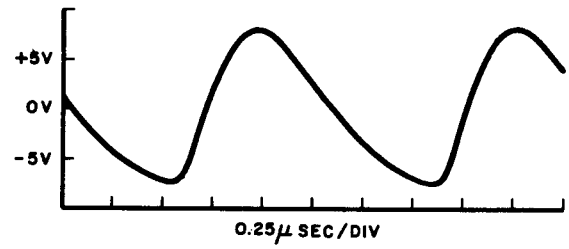


(b) Crystal dissipation.

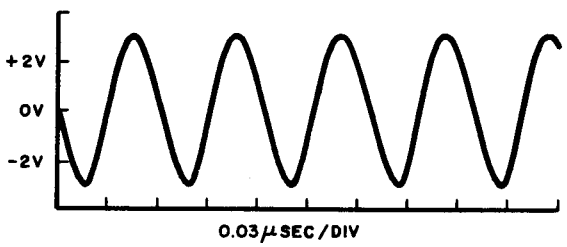
Figure 101–3.—Operating characteristics as a function of crystal resistance, frequency, and tube transconductance for the high frequency band (5.0 to 20 mc).



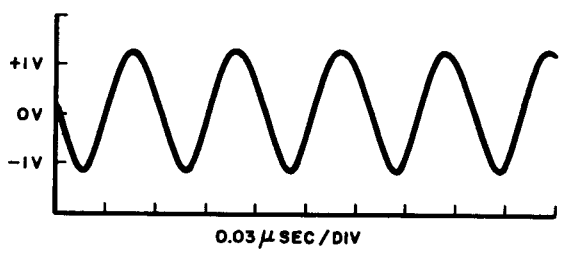
(a) 0.8 MC, R_f = 230Ω



(b) 0.8 MC, R_f = 1000Ω



(c) 19.5 MC, R_f = 11Ω



(d) 19.5 MC, R = 26Ω

Figure 101–4.—Output voltage waveforms across a 10KΩ resistive load.

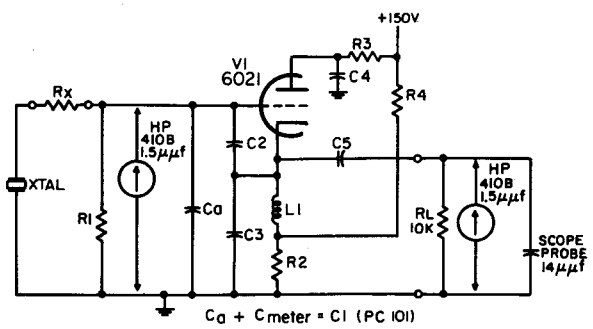


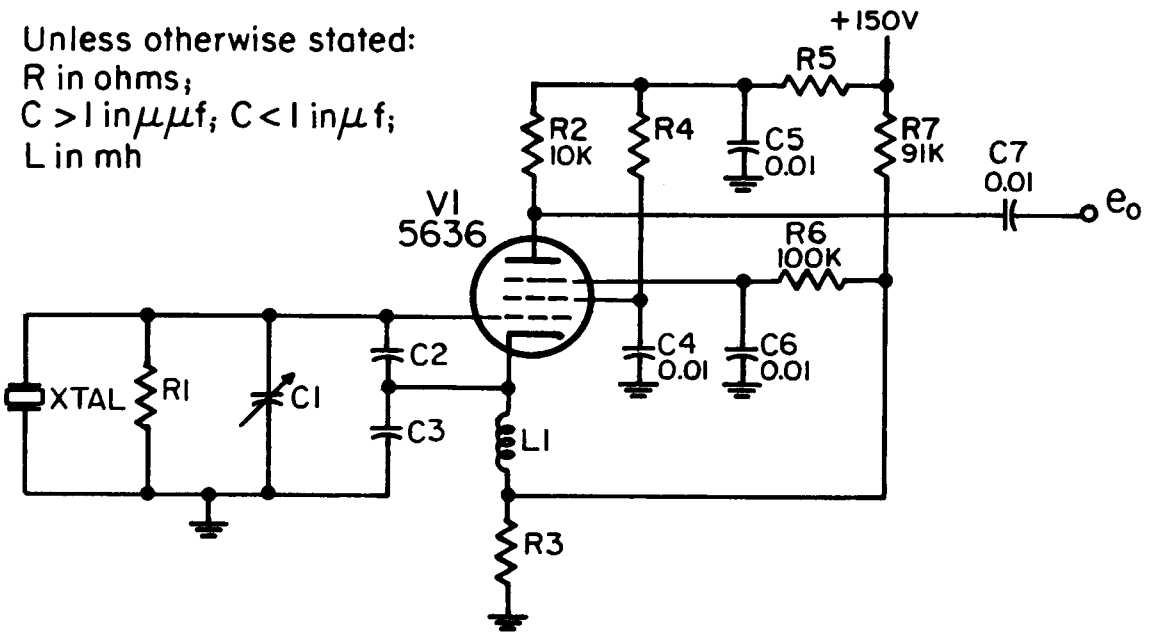
Figure 101-5.—Test circuit used for measuring the performance of PC 101. The crystal resistance R_t, figures 101-1 through 101-4, is equal to the crystal resistance R_c plus the added fixed resistor R_x.

In figures 101-1(a), 101-2(a), and 101-3(a) the solid lines represent data taken using a 6021 with a transconductance near the maximum permitted by MIL-E-1. Data were also taken at the high and low ends of each band using a low transconductance tube; these data, plotted as broken lines, indicate the deterioration of output voltage with decreased transconductance. Deterioration of output voltage with decreased transconductance for other frequencies within each band can be interpolated visually from this data. The crystal dissipation shown in figures 101-1(b), 101-2(b), and 101-3(b) was plotted for the high transconductance tube only, since maximum crystal dissipation would occur when the highest transconductance tube was used.

3.2 *Frequency Stability:* The value of the crystal oscillator as a system component is dependent on its frequency stability. Two major causes of frequency variation are changes in circuit component values and temperature. In general, the least critical components are resistors. For a $\pm 20\%$ variation in value of a single resistor, the frequency deviation is less than one part per million. For a $\pm 10\%$ change in a single capacitor, however, the frequency may change by approximately 8 ppm. Throughout the mean temperature range of $-55°$ C to $+90°$ C, the mean frequency of a typical CR-18/U crystal unit changes by about 15 ppm. This change, together with frequency variations caused by temperature changes of the component parts, can cause a total frequency deviation over the operating temperature range of as much as 35 ppm. For temperature-controlled crystal units, such as the CR-36/U, the total is less than 22 ppm.

NBS PREFERRED CIRCUIT NO. 102
0.8 to 20 MC ELECTRON-COUPLED COLPITTS CRYSTAL OSCILLATOR

NBS PREFERRED CIRCUIT NO. 102
0.8 to 20 MC ELECTRON-COUPLED COLPITTS CRYSTAL OSCILLATOR



Component data:

Preferred crystal types: CR–18/U, CR–36/U. (See Note 1.)

Frequency range mc	R1 Ω	R3 Ω	R4 Ω	R5 Ω	C1 μμf	C2 μμf	C3 μμf	C1′	C2′	C3′	L1 mh
								Distributed "C" μμf (See Note 2)			
0.8–5	330K	620	47K	12K	10.3	15	150	6.3	2	12.5	7.0
3–11	100K	620	68K	6.8K	8.7	18	100	6.3	2	12.5	0.8
5–20	47K	470	110K	150	8.6	22	47	6.3	2	12.5	0.3

R3, R7: ±10% limits; all other R: ±20% limits. C1,C2,C3: ±10% limits; all other C: ±20% limits, or guaranteed minimum value. (See Note 3.)

Power requirements:

150 volts dc at 4 ma (plate and screen supply); 6.3 volts at 150 ma (heater supply).

Operating characteristics:

For output voltage and crystal dissipation as a function of crystal resistance, frequency, and oscillator tube transconductance, see figures 102–1 through 102–3. (See Notes 4 and 5.)

Factors affecting absolute frequency accuracy:	*CR–18/U* *ppm*	*CR–36/U* *ppm*
(a) Manufacturing tolerance (within temperature range)	50	20
(b) Frequency correlation (see Note 6)	10	10
(c) Frequency stability for 10% change in plate and heater voltage	<3	<3
(d) Frequency variation for a 10% change in a single capacitor	<8	<8
(e) Frequency variation for a 20% change in a single resistor	<1	<1

(For Notes, see next page)

NOTES:

1. CR-36/U is a temperature-controlled unit. (See MIL-C-3098B.)

2. The distributed capacitance values shown are typical of those obtained by use of conventional wiring in the test units. Variation of capacitance due to lead dress, the difference in tube socket capacitance versus direct tube leads soldering, etc., will cause these values to vary; therefore, they should be checked and the lumped capacitors C1, C2, and C3, shown in the circuit diagram, changed to keep the total capacitances the same as listed, i.e., the sum of C2+C2′ to remain constant. In most cases adjustment of C1 to keep C_t (defined in section 2.1) equal to 32 $\mu\mu$f will be satisfactory.

3. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.

4. The crystal drive equals I^2R_e where I is the rms current through the crystal, and R_e is the crystal resistance as measured in the appropriate crystal impedance meter. (See MIL-C-3098B.) The current through the crystal can be equated to the current through the 32 $\mu\mu$f of capacitance which is in parallel with the crystal, since the crystal circuit is high Q. The current through the 32 $\mu\mu$f is E/X_c where E is the rms voltage across the crystal, and X_c is the capacitive reactance of 32 $\mu\mu$f at the operating frequency. The crystal drive therefore equals $(E/X_c)^2R_e$.

5. The output voltage is measured with a load of 10KΩ paralleled by 15 $\mu\mu$f.

6. Frequency correlation is defined as the difference between the circuit operating frequency (operating at 25° C with circuit values as shown in the diagram) and the antiresonant frequency of the crystal unit as measured in the appropriate crystal impedance meter. (See MIL-C-3098B.)

PC 102 0.8 to 20 MC ELECTRON-COUPLED COLPITTS CRYSTAL OSCILLATOR

1. APPLICATION

PC 102 provides the designer with a stable frequency source that is relatively immune to changes in output loading. Selection of this circuit is generally based on its ability to provide harmonics of the fundamental frequency to its load. This circuit also provides isolation of the oscillator section from the plate circuit output. Operation at any fundamental frequency in the 0.8 to 20 mc range is accomplished by substituting crystals on a plug-in basis. Tuned circuits are required for the selection of any particular harmonic. This oscillator is particularly useful in electronic equipment requiring operation on a number of separate channels.

2. DESIGN CONSIDERATIONS

2.1 Symbols:

(*a*) P_x: Power dissipated in the crystal unit, or crystal drive level.

(*b*) C_t: The total grid to ground capacitance, due to C1, C2, C3 and associated distributed and stray capacitance.

(*c*) R_t: The total crystal circuit resistance consisting of the sum of the crystal resistance as measured in the appropriate crystal impedance meter and the additional resistance connected in series with the crystal to simulate a higher resistance crystal.

2.2 *Crystal Circuit:* All considerations given in PC 101 apply to this circuit, as the oscillator portion is that of PC 101. Only deviations and additional performance characteristics will therefore be discussed here.

2.3 *Oscillator Configuration:* The Colpitts grounded plate circuit of PC 101 readily adapts itself to electron coupling, since the plate operates at ac ground potential. When a pentode tube is used, the screen grid operated at ac ground potential acts as the anode of the oscillator. The output voltage of PC 102, which is obtained from the pentode plate circuit, is a complex waveform of repetition rate equal to the fundamental frequency of the crystal unit, provided the plate is untuned. When a tuned circuit is added, the fundamental or harmonic of interest may be selected.

Overlapping frequency ranges are provided to assist the circuit designer in the selection of a single oscillator to operate over a range of frequencies without a change of circuit configuration.

2.4 *Oscillator Tube:* A 5636 subminiature pentode tube is used in PC 102. Equivalent miniature tubes such as the 5725/6AS6W miniature pentode tube may be used. Because the separate, externally-connected suppressor lead allows separate dc biasing of the suppressor, the decoupling between the oscillator and the output portion of the circuit is improved.[1] Use of an internally-connected suppressor would increase the reaction of output load changes on the oscillator frequency. A further consideration in the choice of the 5636 was the applicability of a pentode with a high transconductance suppressor to other portions of an equipment using PC 102. This tends to reduce the number of tube types present in an equipment and therefore aids logistic simplification. For each application of PC 102, the capacitors C1, C2, and C3 should be changed where necessary to compensate for distributed capacitances differing from the ones shown in the table on page 102-2. In many cases a variable C1 provides sufficient coverage.

3. PERFORMANCE

Figures 102-1 through 102-3 are graphs of output voltage and crystal drive level versus crystal resistance for the three frequency bands of PC 102. All voltages shown are peak to peak as measured on an oscilloscope.

Figure 102-4 shows typical output voltage waveforms across a 10KΩ load resistor at the frequency extremes covered by PC 102. Al-

[1] See discussion in Notes to the Preferred Circuits Manual, section 16.3(d).

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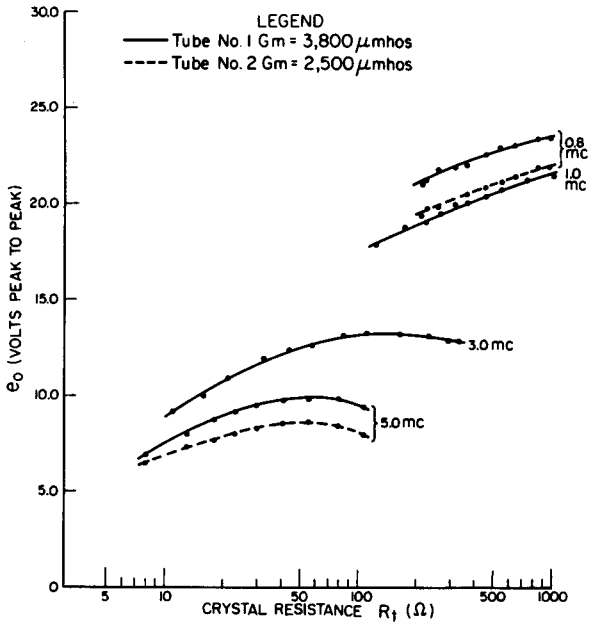
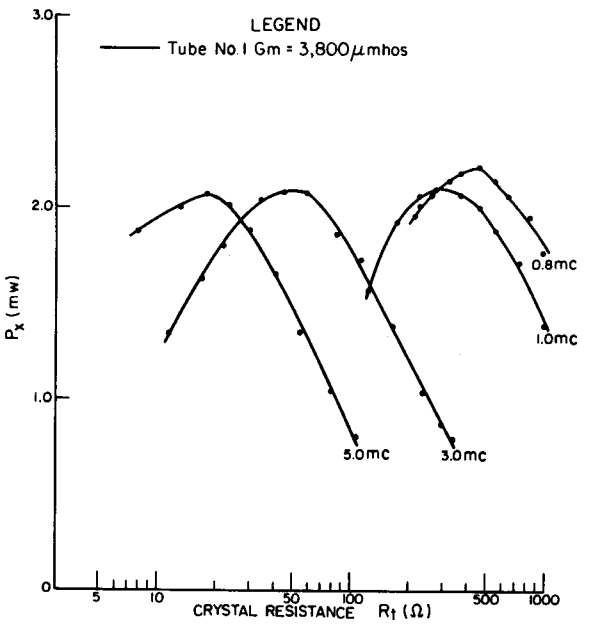


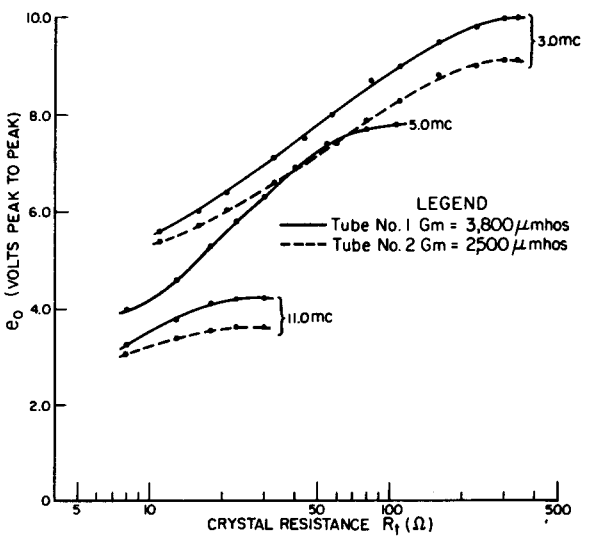
(a) Output voltage.



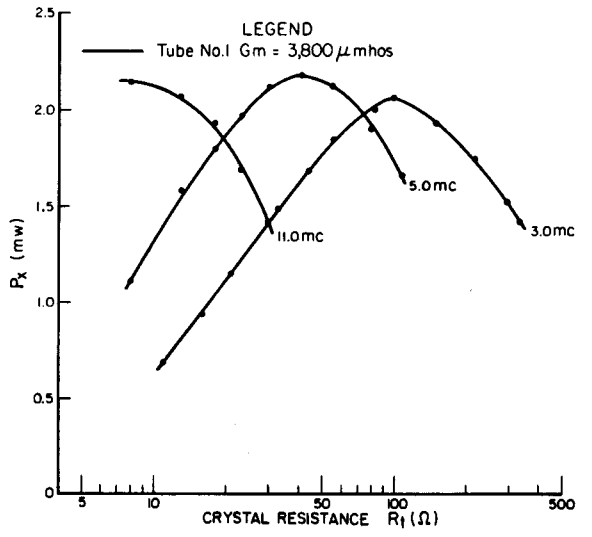
(b) Crystal dissipation.

Figure 102-1.—Operating characteristics as a function of crystal resistance, frequency, and tube transconductance for the low frequency band (0.8 to 5.0 mc).

though the output current at the high end of the high-frequency band is actually non-sinusoidal, it appears to approach a sinusoid when viewed on an oscilloscope, because the



(a) Output voltage.

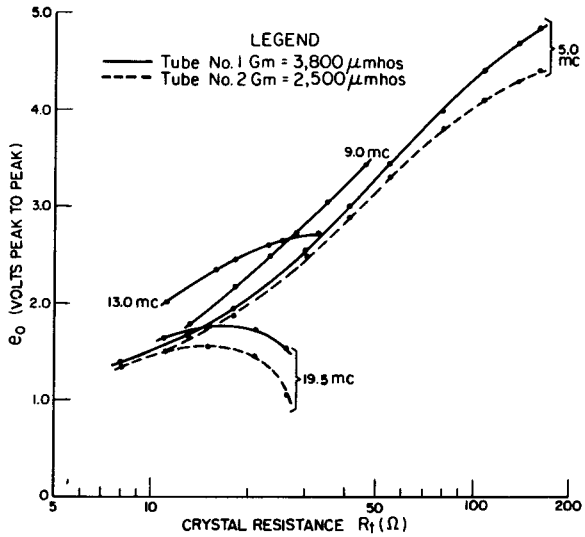


(b) Crystal dissipation.

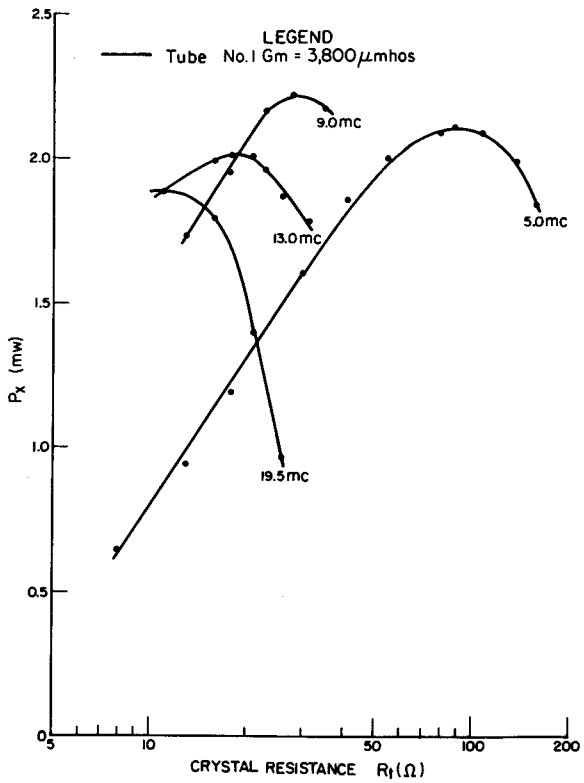
Figure 102-2.—Operating characteristics as a function of crystal resistance, frequency, and tube transconductance for the middle frequency band (3.0 to 11.0 mc).

higher harmonics are attenuated by the load capacitance. The test circuit used to make these measurements is shown in figure 102-9.

Figure 102-5 contains reproductions of the voltage waveforms measured across a 100 ohm resistor (RB in fig. 102-10). This resistor was inserted bteween the plate and the 10KΩ load resistor to reduce the effect of shunt capacitance and thereby provide a more precise representa-



(a) Output voltage.



(b) Crystal dissipation.

Figure 102-3.—Operating characteristics as a function of crystal resistance, frequency, and tube transconductance for the high frequency band (5.0 to 20 mc).

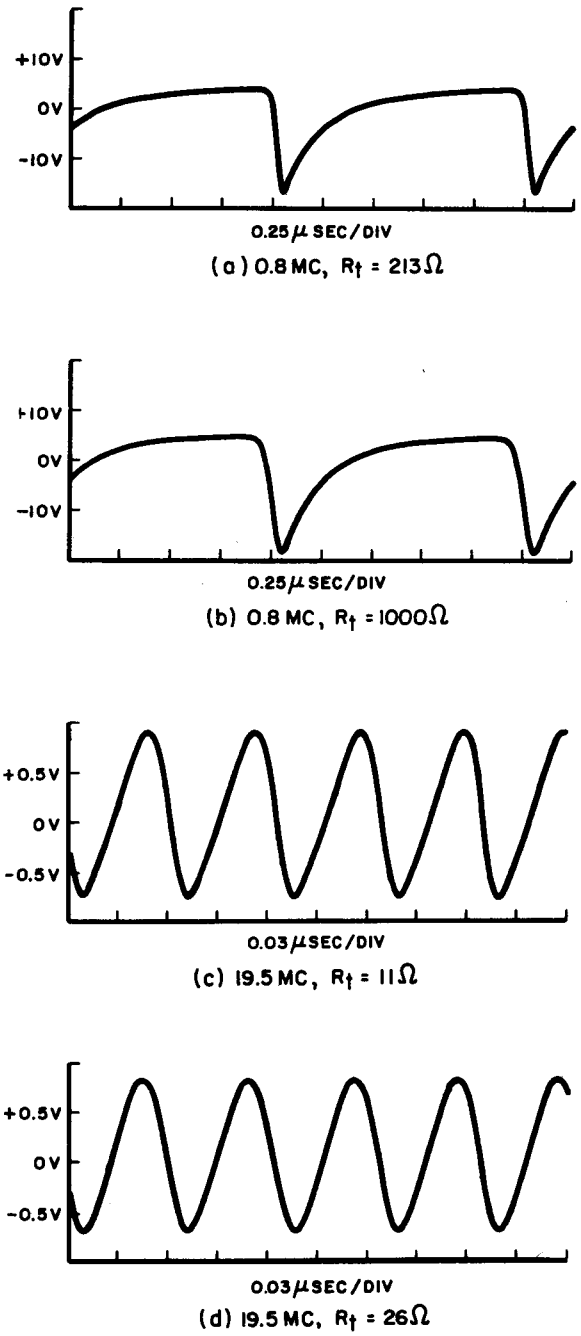


Figure 102-4.—Output voltage waveforms across a 10KΩ resistive load.

tion of the plate current waveform. The circuit arrangement used to make the measurements of plate current waveform is shown in figure 102-10.

The output voltage of each harmonic was measured by replacing the 10KΩ plate load resistor with a 5KΩ resonant impedance circuit tuned to that harmonic frequency. The har-

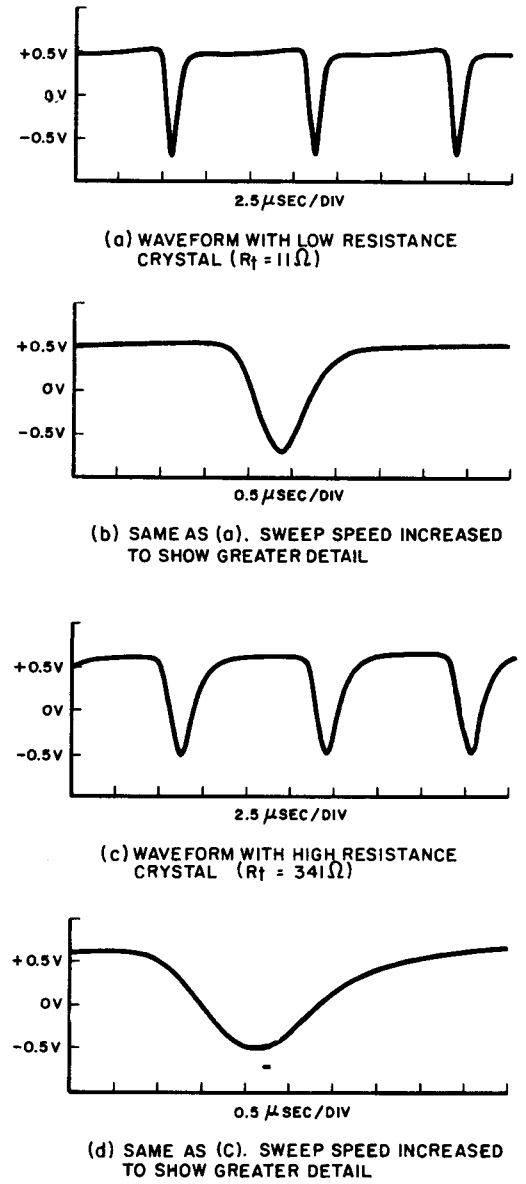


Figure 102–5.—Example of plate current waveform for midband 3 mc fundamental frequency showing the increased angle of current flow caused by an increase in crystal resistance.

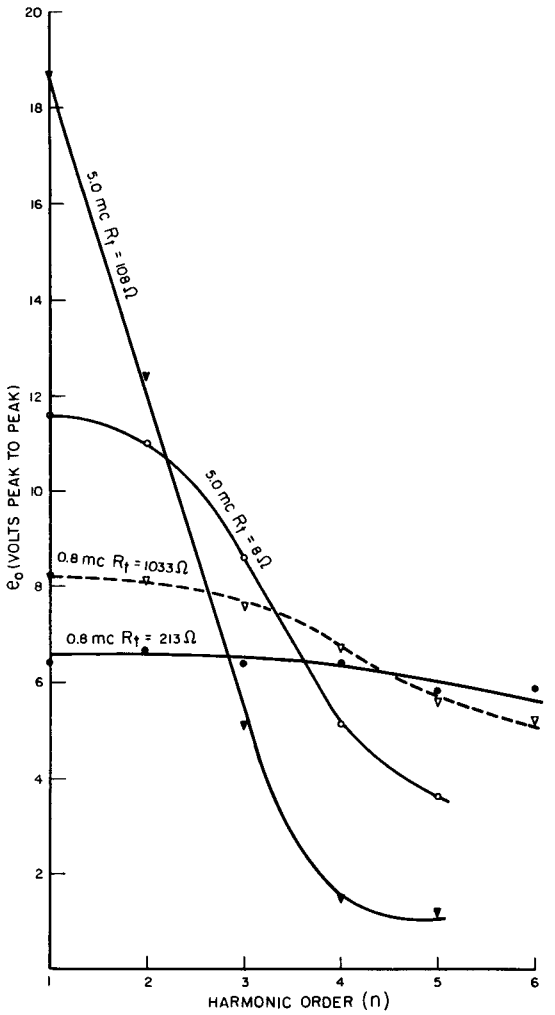


Figure 102–6.—Output voltage across a tuned plate load having a resonant impedance of 5000Ω for the low frequency band (0.8 to 5.0 mc).

monic voltage developed across each tuned circuit is plotted in figures 102–6 through 102–8 as a function of harmonic order, n, where n = 1 is the crystal fundamental frequency.

3.1 *Output Voltage (Resistive Load):* As in PC 101, high limit crystals were simulated by connecting resistors in series with low-resistance crystals. The circuit used in making the performance measurements is shown in figure 102–9, where R_x is the added resistance. In the tests made using PC 101, output across a 10KΩ load resistor decreased as crystal resistance increased. However, with PC 102, output voltage across a 10KΩ load resistor increases as crystal resistance increases. (See figs. 102–1(a), 102–2(a), and 102–3(a).) In each circuit the peak to peak voltage was measured. In PC 101, the output voltage is developed between cathode and ground, and the grid drive is developed across the crystal between grid and ground. This is a cathode follower type of output, and the output voltage is an

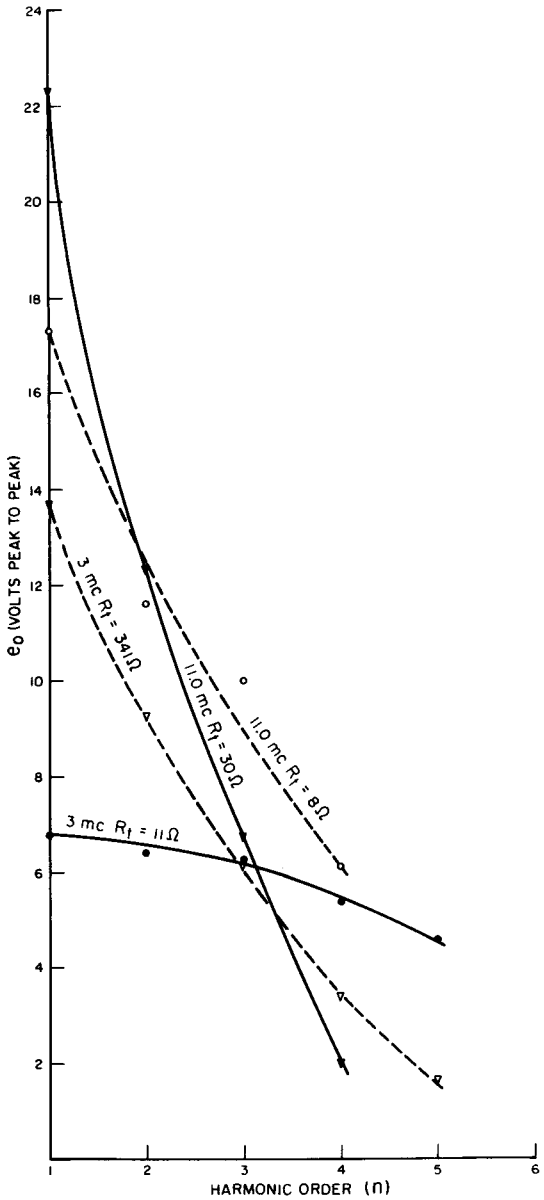


Figure 102-7.—Output voltage across a tuned plate load having a resonant impedance of 5000Ω for the middle frequency band (3.0 to 11.0 mc).

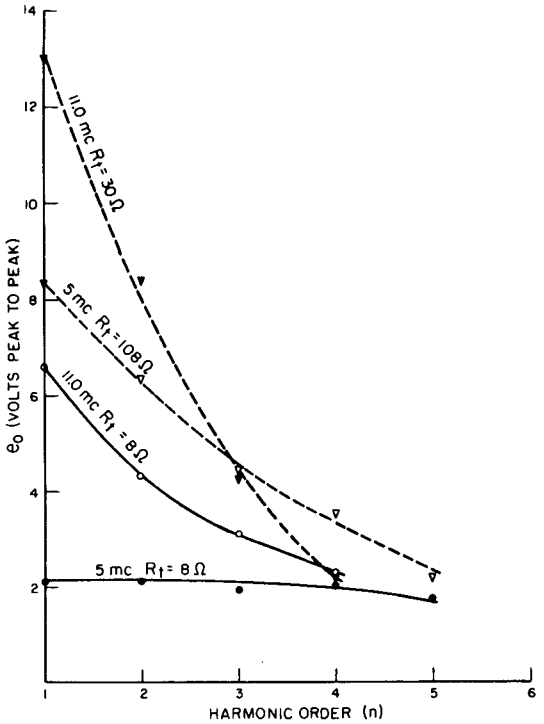


Figure 102-8.—Output voltage across a tuned plate load having a resonant impedance of 5000Ω for the high frequency band (5.0 to 20 mc).

essentially fixed percentage of the crystal voltage for any one frequency. It is not an exact fixed percentage, because changes in output voltage waveform do occur as a function of grid drive. In PC 102, however, the output voltage is a function of plate current flowing through the plate load impedance. When a low resistance crystal is used, the crystal voltage and consequently the grid drive are larger (as in PC 101) than when a high resistance crystal is used. However, the larger grid drive causes a higher grid leak bias and results in a small angle of current flow. (See fig. 102-5.) This smaller angle of current flow produces a current pulse in which the relative magnitude of the higher harmonics is larger than it is for the higher resistance crystal with the larger angle of current flow. Thus (see fig. 102-5), the peak current is greater for the low resistance crystal than it is for the high resistance crystal, although the peak to peak voltage across a 10KΩ load is lower (see figs. 102-1(a), 102-2(a), and 102-3(a). This is caused by the attenuation of the higher order harmonics of the current pulse through the 25 μμf (load plus distributed) parallel capacitance across the 10KΩ load resistor. The difference in harmonic content of the high and low resistance crystals for a given frequency is evident from the curves of figures 102-6, 102-7, and 102-8.

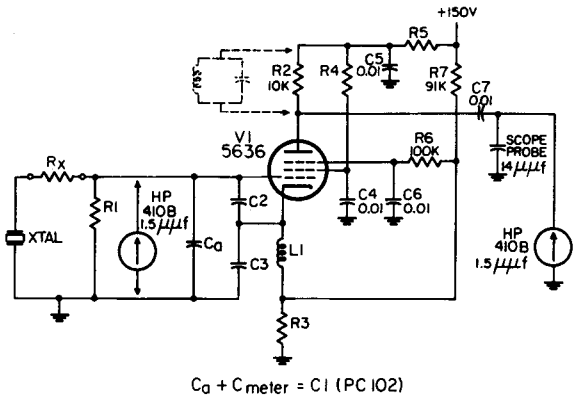


Figure 102–9.—Test circuit used for measuring the performance of PC 102. The crystal resistance R_t, figures 102–1 through 102–8, is equal to the crystal resistance R_e plus the added fixed resistor R_x.

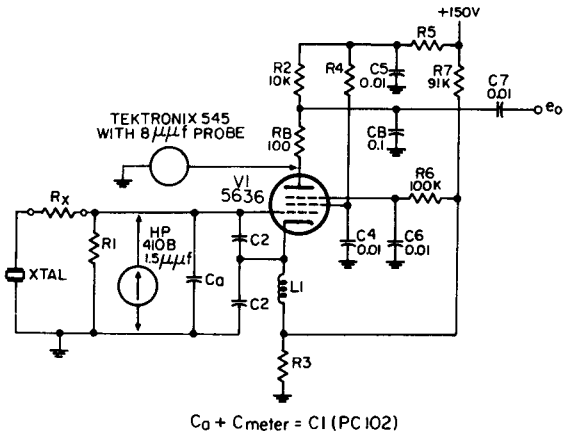


Figure 102–10.—Circuit used to obtain plate current waveforms shown in figure 102–5.

3.2 *Harmonic Output (Tuned Load):* Because of the widespread use of the Colpitts electron-coupled crystal oscillator as a source of harmonic voltages, measurements of output voltage generated across a tuned load were made for selected frequencies in all three bands of PC 102. The tuned circuits used for these measurements were selected to have an impedance in the vicinity of 5000 ohms. No attempt was made to build tuned circuits of exact impedance for each harmonic. Instead, the actual impedance in the circuit was measured using the parallel resistor method.[2] All output voltages were then normalized with respect to 5000 ohms, on the assumption that the pentode oscillator was a current generator and that therefore the output voltage was directly proportional to the impedance of the output tuned circuit for any given grid drive condition. The results of these measurements are shown in figures 102–6, 102–7, and 102–8, where the solid lines are graphs of a frequency with a low resistance crystal in the circuit, and the dotted lines show the results with a high resistance crystal in the circuit. The inversion of amplitude relations between the high and low frequency of each band as compared to the voltages measured across an output load resistor (see figures 102–1(a),102–2(a), and 102–3(a) is accounted for by the effect of the capacitance in parallel with the load resistor which bypasses more of the energy in the high frequency current pulses than in the low frequency current pulses.

3.3 *Crystal Dissipation:* As shown in figures 102–1(b), 102–2(b) and 102–3(b), the crystal dissipation does not exceed the recommended maximum[3] for the temperature-controlled crystal CR–36/U. All measurements on high resistance crystals were made by adding resistance in series with a low resistance crystal to simulate a higher resistance crystal.

[2] Assuming that the tuned circuit at resonance is resistive, the impedance of the tuned circuit equals $(e_1/e_2-1)R_p$, where e_1 is the output voltage with no resistor connected across the tuned circuit, and e_2 is the output voltage with a resistor R_p connected across the tuned circuit.

[3] 5 mw to 9,999.999 kc; 2.5 mw from 10,000 kc to 20,000 kc. For the CR–18/U, the maximum recommended drive level is 10 mw to 9,999.999 kc, and 5 mw from 10,000 kc to 20,000 kc. See WADC Technical Report 56–156, "Handbook of Piezoelectric Crystals for Radio Equipment Designers," October 1956, p. 464 (ASTIA Document No. AD 110448.)

PART 1
PREFERRED CIRCUITS MANUAL

B. TRANSISTOR CIRCUITS

NBS PREFERRED CIRCUIT NO. 201

SILICON TRANSISTOR VIDEO AMPLIFIER

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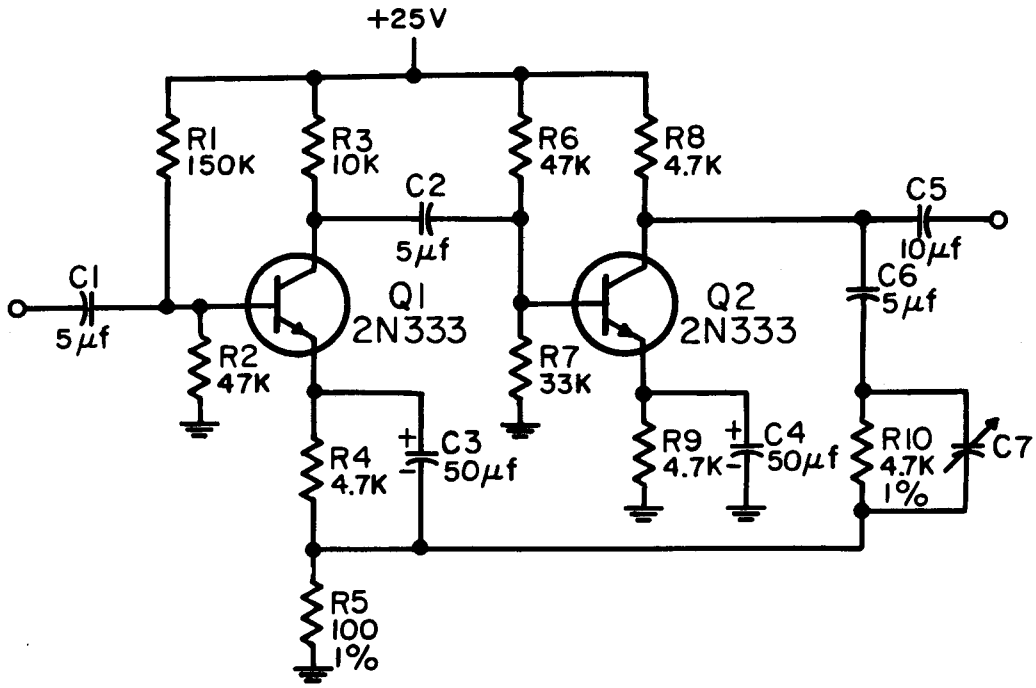
NBS PREFERRED CIRCUIT NO. 201

SILICON TRANSISTOR VIDEO AMPLIFIER



Components:

R5: Select for desired voltage amplification.

C7: Between 4 and 30 $\mu\mu$f, to be selected after total output capacitance is determined.

R5, R10: $\pm 1\%$ limits; all other R: $\pm 10\%$ limits. All C: $\pm 20\%$ limits. (Note 1)

Operating characteristics:		*R5:*	
	100 Ω	*220 Ω*	*470 Ω*
Voltage amplification	45	20	10
Rise time [2] (+150° C)	1.0 μsec	0.9 μsec	0.7 μsec
Rise time [2] (+25° C)	0.5 μsec	0.4 μsec	0.35 μsec
Droop for 500 μsec pulse (−50° C)	3.0%	1.5%	1.0%
Maximum output amplitude [3]	2 v peak	2 v peak	2 v peak
Maximum input amplitude [3]	45 mv peak	100 mv peak	200 mv peak
Input impedance	22 KΩ	27 KΩ	32 KΩ
Output impedance	250 Ω	210 Ω	180 Ω
Maximum amplification variation with transistor replacement. [4]	±5%	±3%	±2%
Maximum amplification variation with temperature. [4] at +150°C and −50°C Respectively	+5, −10%	+4, −7%	+2, −7%

Minimum load resistance: 10 KΩ.

Temperature range: −50° C to +150° C.

NOTES:

1. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified above. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.
2. Total output capacitance=30 $\mu\mu$f.
3. Plus and minus from ac zero level.
4. Load resistance=10 KΩ.

PC 201 SILICON TRANSISTOR VIDEO AMPLIFIER

1. APPLICATION

PC 201 is a high-gain intermediate-level (±2.0 volts maximum output) transistor video amplifier for use in applications where stability of gain and a wide temperature range are important. It is non-inverting, has an input impedance of 20KΩ, and will operate into loads of 10KΩ or larger. Impedance levels are such that it may be cascaded for additional voltage gain.

2. DESIGN CONSIDERATIONS

Silicon transistors are used to obtain a wide temperature range. Negative feedback of 20 db extends the frequency range and stabilizes the voltage amplification against temperature changes and transistor replacement. Selection of R5 provides for a choice of voltage gain.

Either raising the value of R5 or lowering the value of R10 will decrease the voltage amplification with only slight accompanying change in bandwidth. This situation results from the fact that changing either R5 or R10 in a direction to decrease voltage amplification decreases the open loop voltage gain, A_o, while increasing the feedback factor, B. Thus the change in magnitude of negative feedback, BA_o, is slight, resulting in only a slight increase in bandwidth at the lower gain. Changing R5 is preferred since it will not derate the maximum output voltage that may be obtained.

The major limitation on circuit bandwidth and temperature range is imposed by the transistor itself. The input impedance, current amplification and, to a lesser extent, the output impedance of the transistor all have an effect on the voltage amplification. The limitation is imposed because the variation of these parameters with frequency or with temperature is much more severe than the variation in component values. Since all three parameters are interdependent in determining voltage gain, there is no one parameter measurement which will gauge operation of the transistor at extreme temperatures or at high frequency. For this reason the alpha cutoff frequency, $f_{\alpha co}$, though a good indication of high frequency performance, is not directly related to the rise time that may be achieved with any particular transistor.

Resistors R4 and R9, in conjunction with the biasing resistors, serve to minimize the change in quiescent operating point accompanying temperature variation and transistor replacement. A ratio indicating the relative amount of stabilization may be computed for each stage with the value of unity indicating perfect operating point stabilization. The stabilization ratio for Q1 is

$$\frac{h_{fe}}{h_{fe}+1+\frac{1}{R4/R1+R4/R2}}$$

where h_{fe} is the common emitter forward current transfer ratio. A similar expression applies to Q2 with R9, R6, and R7 substituted for R4, R1, and R2. The stabilization ratios are 0.8 and 0.87 for Q1 and Q2 respectively.

The value of R8 is low enough so that the total capacitance of the output terminals is driven without a significant increase in rise time and yet high enough to provide sufficient open-loop gain for the circuit.

Capacitor C7 compensates for overshoot produced by the total capacitance at the output terminals and is to be selected after that capacitance is determined. Its value will be between 4 and 30 μμf for output capacitance values up to 100 μμf.

An important aspect of the circuit design is the ability to cascade feedback pairs for additional voltage amplification. This is possible due to the high input impedance and low output impedance resulting from negative voltage feedback.

3. PERFORMANCE

Voltage amplifications of 45, 20 or 10 are obtained for R5=100, 220 or 470Ω respectively. For each, an output extending plus and minus 2 volts from the average voltage of the waveform may be obtained.

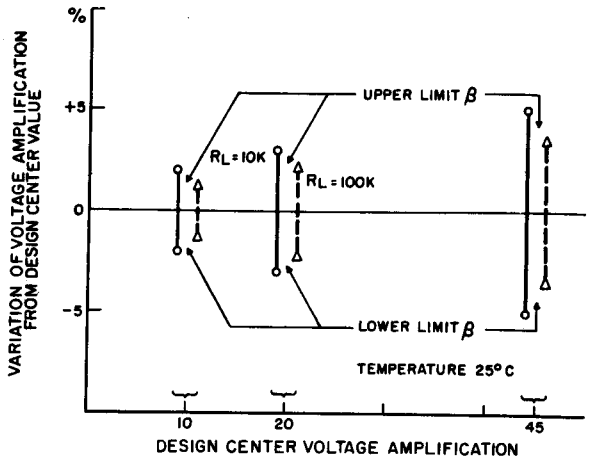


Figure 201–1—Variation of voltage amplification from design center value with transistor replacement

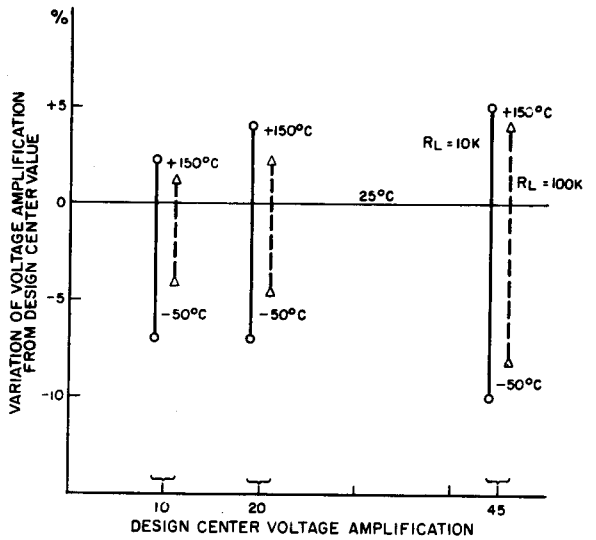


Figure 201–2—Variation of voltage amplification from design center value with temperature

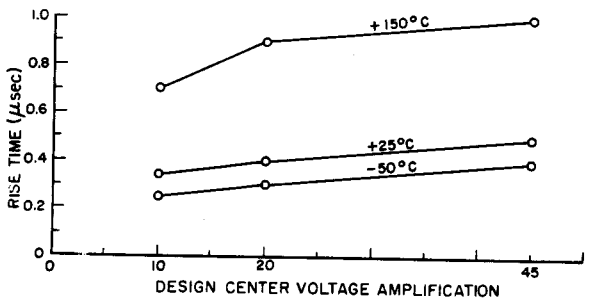


Figure 201–3—Maximum pulse rise time as a function of temperature and design center voltage amplification

For any 2N333 transistors within the specified limits of beta (18 to 40), the maximum variation of voltage amplification with transistor replacement is given in figure 201–1 for the three alternate values of voltage gain. Improved stabilization is obtained with higher values of load resistance. Replacement of transistor Q2 has considerably more effect on the voltage amplification than replacement of Q1. At 10KΩ load and R5=100Ω, maximum amplification variation with replacement of Q1 is only ±0.5%.

The maximum variation of voltage amplification with temperature is given in figure 201–2 for the three alternate values of voltage amplification. Here again, improved stabilization is obtained with higher values of load resistance. Voltage amplification variation with temperature is primarily due to transistor parameter variations. Relatively few 2N333 transistors have the poor temperature characteristics shown in figure 201–2. For the highest gain circuit, percentage variations of +2 and −6% would cover the great majority of cases with proportionately smaller changes for the lower gain circuits.

Though the circuit will operate into loads less than 10KΩ, the voltage amplification stabilization is poor due to reduced open-loop gain. As the load resistance is increased above 10KΩ, the open-loop gain becomes larger and the stabilization of voltage amplification is improved. Values of load equal to 100KΩ or larger appear as no load, beyond which the open-loop gain cannot be increased.

For R5=100Ω (voltage amplification of 45) the maximum droop, occurring at low temperature, is 3% for a 500 μsec pulse. At reduced gain the droop decreases to 1.5% for R5=220Ω and 1.0% for R5=470Ω.

The rise time of PC 201 will vary depending on the transistor in the output stage and the ambient temperature. Rise times given on the circuit sheet and in figure 201–3 are the worst that may be expected.

Output waveforms at 25° C, 150° C, and −50° C for two sample pairs of transistors are shown in figures 201–4 and 201–5. The

input is a 250 kc square wave having a rise time of .02 μsec. The waveforms of figure 201-4 have been compensated by C7 for overshoot, while those of figure 201-5 are the same waveforms not compensated. The two sample pairs chosen are not intended to represent the best or worst waveforms that may be obtained.

Supply voltage variations of ±10% will affect the voltage amplification by ±1%. Maximum current drain from the supply is 3.5 ma.

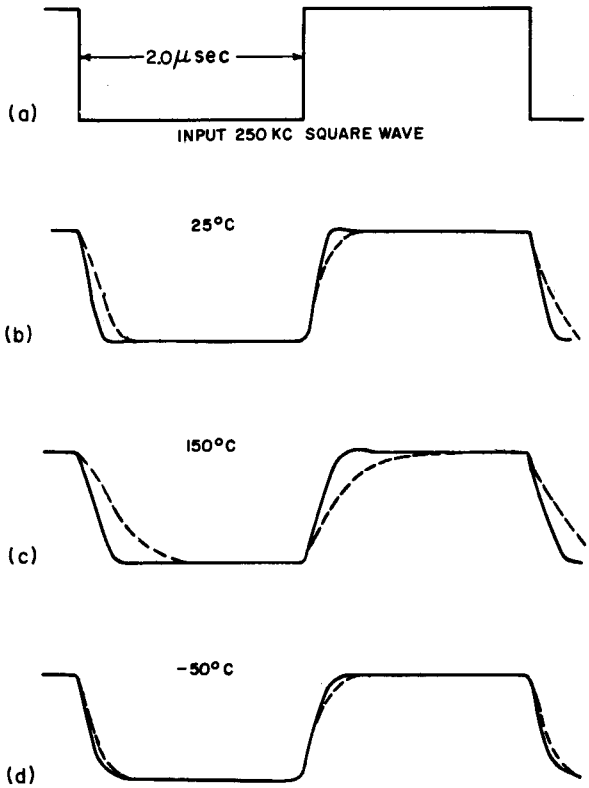


Figure 201-4—Waveforms of PC 201 for two sample pairs of transistors. R5=100Ω. Output=4 volts. Total output capacitance=30 μμf. Compensation for overshoot by C7

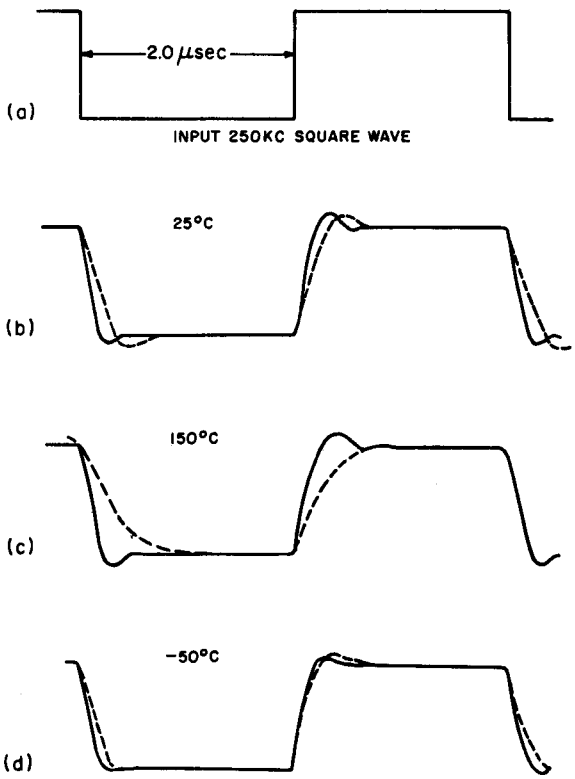


Figure 201-5—Waveforms of PC 201 for two sample pairs of transistors. R5=100Ω. Output=4 volts. Total output capacitance=30 μμf. No compensation for overshoot

NBS PREFERRED CIRCUIT NO. 202

TRANSISTORIZED 7 KV CRT POWER SUPPLY

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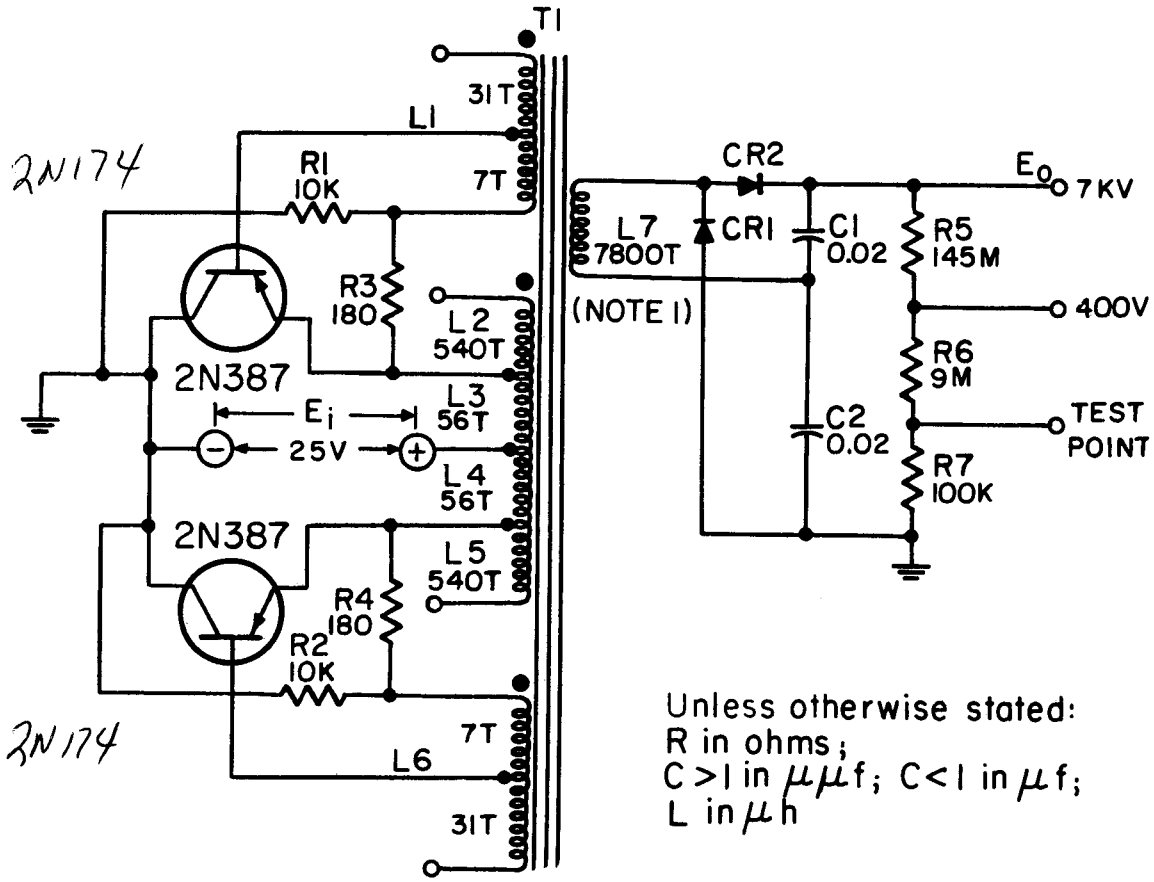
NBS PREFERRED CIRCUIT NO. 202

TRANSISTORIZED 7 KV CRT POWER SUPPLY



Components:

CR1 and CR2: Six 1N588 silicon diodes connected in series.

T1: See figure 202–1.

All R: ±10% limits. (Note 2)

All C: ±20% limits.

Operating characteristics:

Input voltage, E_i: 25 volts dc ±1%.

Output voltage, E_o: 7 kv dc.

Ripple (peak to peak): 12 volts at 100 μa. (See figure 202–4).
15 volts at 200 μa.

Operating frequency: ≈450 cps.

Operating temperature: −55° C to +71° C.

Power requirements:

Maximum input power: 220 ma at 25 volts for E_o=7 kv, I_o=200 μa.

NOTES:

1. Lead from inner end of secondary should be connected to the junction of C1 and C2 to keep the maximum voltage stress between the feedback and secondary windings to $E_o/2$.

2. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified above. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.

PC 202 TRANSISTORIZED 7 KV CRT POWER SUPPLY

1. APPLICATION

Preferred circuit 202 has been designed to provide the high voltage source for the screen grid and final anode of 5- to 12-inch magnetic deflection cathode-ray tubes in equipment where full or partial transistorization exists. It will operate in the ambient temperature range of −55 to 71° C.

2. DESIGN CONSIDERATIONS

2.1 *Circuit Choice:* A transistor full-wave dc to dc converter with the load connected between voltage source and emitter was chosen because the collectors can be physically attached to a grounded or chassis-connected heat sink. Further, this circuit can be used with the transformer-rectifier-filter package described in PC 6.

2.2 *Transistor Choice:* Type 2N387 transistors were used because they were the units in MIL–STD–701 (Navy) which most nearly met the voltage, power, and saturation resistance requirements of the circuit.

2.3 *High-Voltage Transformer:* The core of the high-voltage transformer (fig. 202–1) is made of nickel-iron U laminations. This material has a square-loop hysteresis curve and a high permeability which permits a minimum of primary turns for a given input voltage and flux density. For winding ease, the U lamination has advantages over the wound toroidal construction. Also, the toroidal construction is difficult because of the insulation requirements of the high-voltage winding. This insulation is more readily applied if layer-winding techniques are employed.

The transformer is so designed that it may be used either for tube or transistor operated supplies. The tube unit operates from a 300-volt supply, whereas the transistor unit will operate from a 25-volt supply. A voltage of 25 volts was chosen as the one most likely to become a standard regulated voltage for transistor use. The next higher voltage likely to become standard is 50 volts, and this is too high to provide any safety margin, even for transistors with a 100-volt peak inverse rating.

No attempt has been made to optimize the size and weight of the transformer shown in figure 202–1. The choice of number of turns and physical core size was a compromise between ease of construction, size, and weight, as opposed to power efficiency. If advanced construction techniques make possible a better transformer design, the improved transformer may be substituted without any circuit changes being required in PC 202.

The primary is wound in two sections. The inner section contains the major portion of the primary and is layer wound. The second section contains the portion of the primary designed for use with transistors and is bifilar wound to reduce overshoots caused by leakage inductance. The energy stored in the leakage inductance tends to dissipate via the off transistor, unless this energy can be closely coupled to a dissipative path through the transistor that is conducting. Bifilar winding provides this close coupling. The problem of leakage induced reverse emf is not as great in the case of tube oscillators, and the mitigating effect of the bifilar coupling is not as complete since the greater portion of the primary is not bifilar wound. The technique of using bifilar windings in one section of the primary does decrease overshoots, however, and creates but a nominal insulation problem. Complete bifilar winding

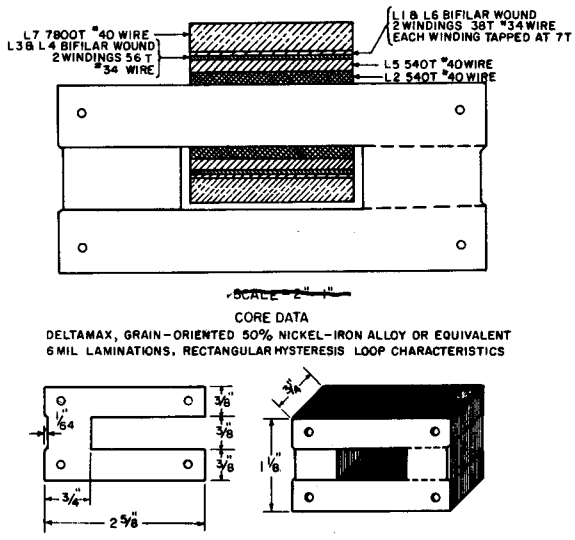


Figure 202–1.—Construction details of high voltage transformer

would create a greater insulation problem because of the larger difference in potential between the end turns. In the bifilar portion of the primary, larger wire is used for carrying the greater current in the lower voltage transistor case.

2.4 *Test point:* To allow measurement of the output voltage without special equipment, such as high-voltage probes, a tap is provided on the high-voltage bleeder for connecting a microammeter between the test point and ground. The resistance of the microammeter will be very small with respect to the 100,000-ohm portion of the bleeder resistor; therefore, such connection is physically equivalent to inserting the microammeter in series with the 154 megohm bleeder. Since the 154 megohm bleeder will not be made up of precision resistors, the case containing transformer, rectifier, filter, and bleeder must have the current in microamperes corresponding to 7 kv printed on it. This calibration would take place in final test, and therefore the inscription on the case does not unduly complicate unit production.

2.5 *Screen Grid Voltage:* A second tap on the high voltage bleeder provides 400 volts for the screen grid of the cathode-ray tubes.

2.6 *Theory of Operation:* If a perfect voltage source were connected in series with a perfect inductor and a switch, then with the switch closed the voltage across the inductor would remain constant with time and would be equal to the potential of the voltage source. The current through the inductor would rise linearly with time at such a rate that the change of flux linkages as a function of time would be equal to the source voltage.

In a physical circuit, the voltage source has resistance; the switch can be approximated by a transistor which is biased on, and which has a nonlinear resistance. Further, the inductor, if air core, has resistance; if iron core, it has resistance plus nonlinear inductance. Under these conditions, the voltage across the inductor will no longer be constant, and the rate of change of current with time will be nonlinear. This nonlinearity can be accentuated by using a square-loop core which saturates sharply, and by inductively coupling the main source of transistor forward bias from this inductor. The inductor has now become a transformer. The addition of a second transistor and a duplicate pair of windings makes a full-wave device. By adding a fifth winding, means are provided for isolating a load from the input in addition to effecting an impedance transformation.

In a circuit such as the one described (see fig. 202–2), when the voltage source is initially switched on, one of the two transistors will conduct more heavily than the other. This unbalanced current flow is caused by dissimilarities in the two halves of the circuit. The base windings L2 and L4 are so connected that, once having started, the unbalance will regeneratively increase until one transistor is biased on and the other biased off. Under these conditions, the approximate equivalent circuit of figure 202–3 may be used, since L3, L4, and Q2 are effectively out of the circuit. Here a parallel resistor, R_p, is connected across a perfect inductor, L. In series with this combination are a voltage source, V, and a resistor,

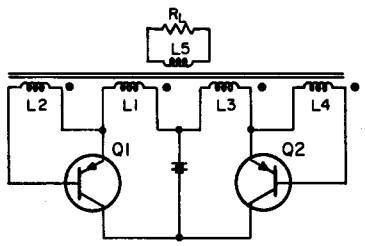


Figure 202–2.—Simplified circuit diagram of PC 202

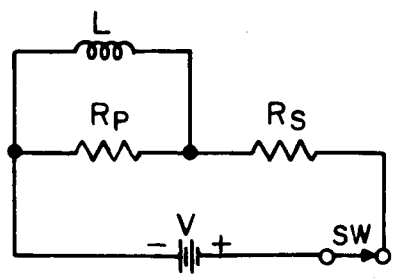


Figure 202–3.—Circuit equivalent to PC 202 when one transistor is on and the other off

R_s. R_p represents the sum of the transformer losses and load power, while R_s represents the sum of the source and switch (transistor) losses. If an imperfect inductor, an imperfect voltage source, and an imperfect switch are used, closing the switch will cause an initial rise in current. This will be followed by an approximately linear current rise, varying at a rate that keeps $L(di/dt)$ equal to V minus IR_s. Since IR_s increases with I, the magnitude of di/dt will decrease with time if L remains constant. When the integral of the instantaneous induced emf, e, times the differential time, dt,* reaches the saturation flux density of the core, the inductance of the coil drops sharply. This allows a rapid current rise in the coil. The core saturation also reduces the base emitter drive of the transistor, since it is mainly derived from an inductively coupled coil (such as L2, figure 202–2). The coefficient of coupling of L1 and L2 is drastically reduced by the saturation of the transformer core. The circuit will no longer be capable of maintaining an increasing di/dt, because the transistor will be called on to pass a rapidly increasing current when its base drive has decreased sharply; therefore di/dt will begin to decrease. The resultant emf will be in such a direction as to back bias the base of the transistor which was on, and forward bias the base of the transistor which was off. The reversal of direction of $d\phi/dt$ due to the decreasing di/dt will proceed regeneratively and switch the transistor which was initially biased on, to a biased off state. It will simultaneously switch the transistor which was biased off to a biased on state. The process will now repeat itself.

2.7 *Operation With One Transistor Inoperative:* Under some conditions of failure of one transistor, PC 202 will continue to operate, but with reduced output voltage. These failure conditions are those which cause an open circuit in one of the junctions. A short circuit between junctions will overload the circuit and stop oscillations. Failure of one transistor during a mission will cause increased indicator tube deflection, but the change will be small and may not be noticed by the operator. Further, because the transistors are not designed for quick interchange, replacement during a mission is unlikely. However, because the transistors operate far below maximum dissipation ratings, operation with a single transistor should suffice until the next maintenance check.

2.8 *Regulation*: In general, the regulation of the supply (fig. 202–4) will be sufficient for most uses with no additional circuitry required. For reduction of output ripple and output impedance, additional capacitance may be added across the cathode-ray tube input. The output voltage stability can be improved by the use of a regulator in the collector circuit of the transistors, but such a regulator becomes rather complex if stability better than that provided by PC 202 is desired.

3. MEASURED PERFORMANCE

High-voltage power supplies of the dc to dc converter type such as PC 202 have a bleeder resistor connected across the output as an integral part of the circuit. This resistor is usually encapsulated, along with the output filter capacitors and associated parts. With this in mind all load currents measured below are exclusive of the bleeder current.

3.1 *Output Characteristics as a Function of Load Current:* Electromagnetic cathode-ray tube final-anode currents, in general, average less than 100 μa. The curves for PC 202 (figs. 202–4, 202–5) are plotted considerably beyond this point to demonstrate operating characteristics at extended current ranges.

The relationship between output voltage and current is shown in figure 202–4. The change in output voltage for a change in load current of 100 μa is less than 2%.

When one transistor is disconnected, the frequency of the oscillation increases by a factor of approximately three, and the variation of output voltage as a function of load current is increased. Under these conditions, the average variation is approximately 9% for a variation of load current of 100 μa. The output voltage plotted in figure 202–5 was measured

* $\int edt$ is the best measure of the total flux linkages in the core at any instant, since the nonlinearity of the core does not enter the equation as it does when ampere turns are used.

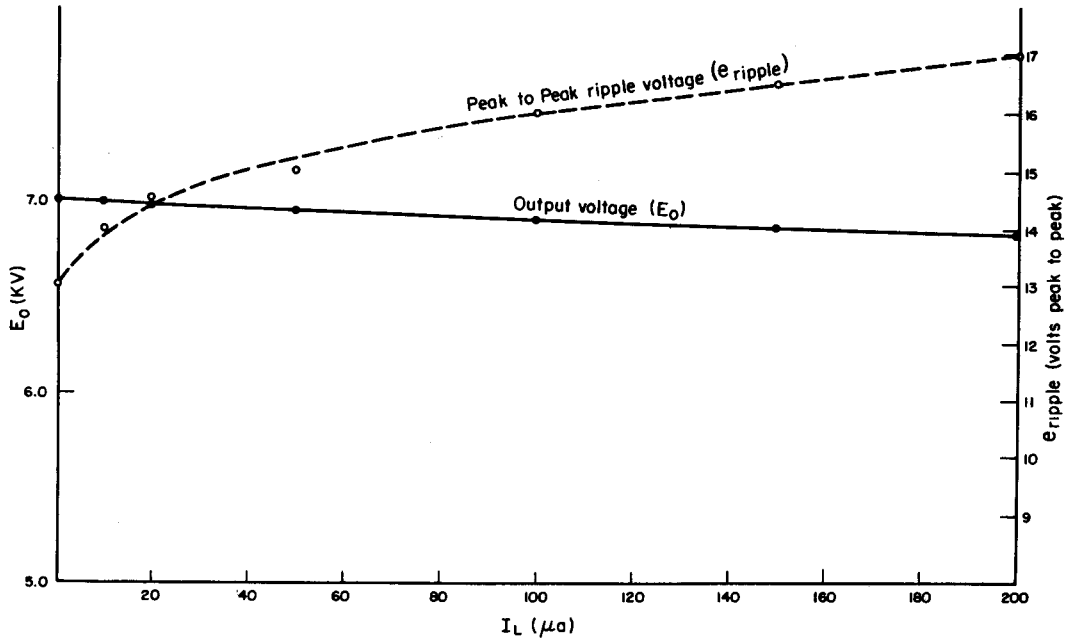


Figure 202–4.—Normal output of PC 202

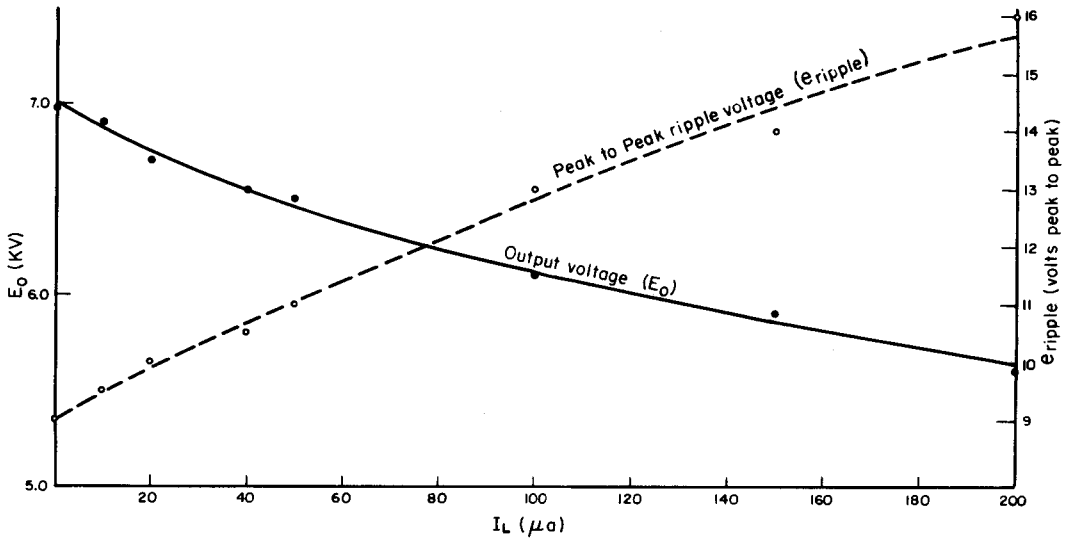
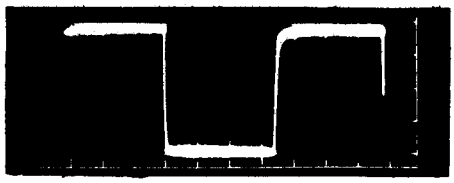


Figure 202–5.—Output of PC 202 when one transistor is open

by setting the output voltage with both transistors operating to 7 kv for no-load conditions and then disconnecting one transistor. Under the no-load condition, there was a change in output of less than 50 volts in 7 kv.

3.2 *Effect of Variations of Transistor Parameters:* The parameters of most interest for the operation of PC 202 are the on-resistance of the transistor and the input impedance, h_{IE}, in the grounded emitter configuration. The 2N387 has a rated input impedance of 60 ohms, max but this is in series with a 180-ohm resistor; therefore, variations in value of two to one in h_{IE} have negligible effect on the operation of the transistor. The voltage across the collector emitter terminals, with an input voltage of 3

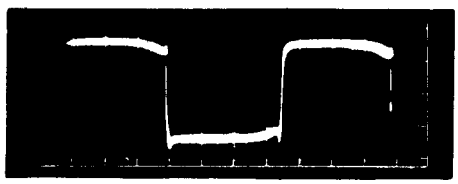


←——SWEEP
0.3 milliseconds/div.

(a) Emitter-collector voltage vs. time for load current of 35 μa

←——SWEEP
0.3 milliseconds/div.

(b) Emitter-collector voltage vs. time for load current of 35 μa (Y axis expanded to show overshoot)



←——SWEEP
0.3 milliseconds/div.

(c) Base-emitter voltage vs. time for load current of 35 μa

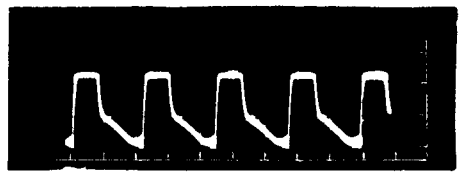
Figure 202-6.—Waveforms for PC 202, normal operation

volts to the transistor, varies from 60 to 90 mv for a collector current of 200 ma. This is the typical operating condition of the transistor when in the on condition, and this voltage drop is small (less than $\frac{1}{10}$ volt) compared to the drops in the other portions of the collector emitter loop. Under these conditions, variations of two to one in this drop will effect the output voltage by less than 50 volts in 7 kv.

3.3 *Pertinent waveforms:* Oscillographic displays of emitter to collector voltage versus time are shown in figure 202-6. The time scale runs from right to left. Figure 202-6(a) shows the normal emitter collector waveform, while in (b) the voltage scale is expanded to illustrate the overshoot. It can be seen that the overshoot is less than 2 volts in magnitude. This

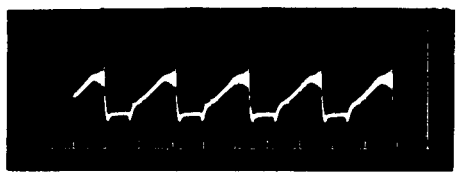
←——SWEEP
0.3 milliseconds/div.

(a) Voltage vs. time across points E and C, figure 202-8



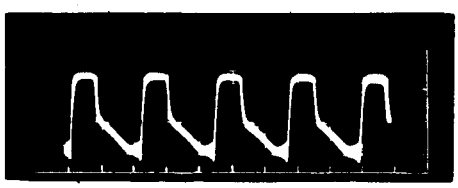
←——SWEEP
0.3 milliseconds/div.

(b) Voltage vs. time across points E′ and C′, figure 202-8



←——SWEEP
0.3 milliseconds/div.

(c) Voltage vs. time across points E and B, figure 202-8



←——SWEEP
0.3 milliseconds/div.

(d) Voltage vs. time across points E′ and B′, figure 202-8

Figure 202-7.—Waveforms for PC 202 with one transistor removed from the circuit

small overshoot, which is achieved by the bifilar winding of both primary and feedback coils, provides an adequate safety factor since the transistor used has a peak rating of 80 volts with the base biased off. The base emitter waveform is shown in (c).

The waveforms shown in figure 202-7 were observed using PC 202 after removal of one transistor. These waveforms show operating

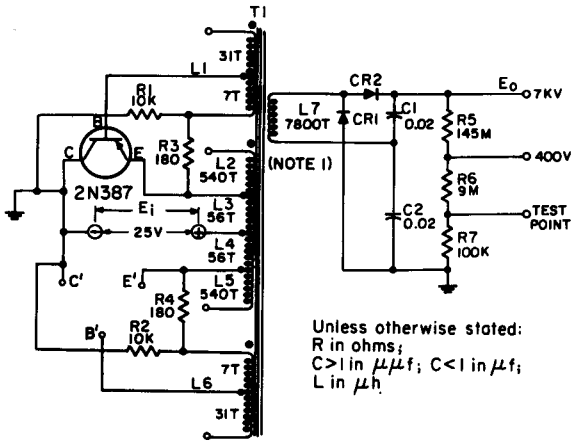
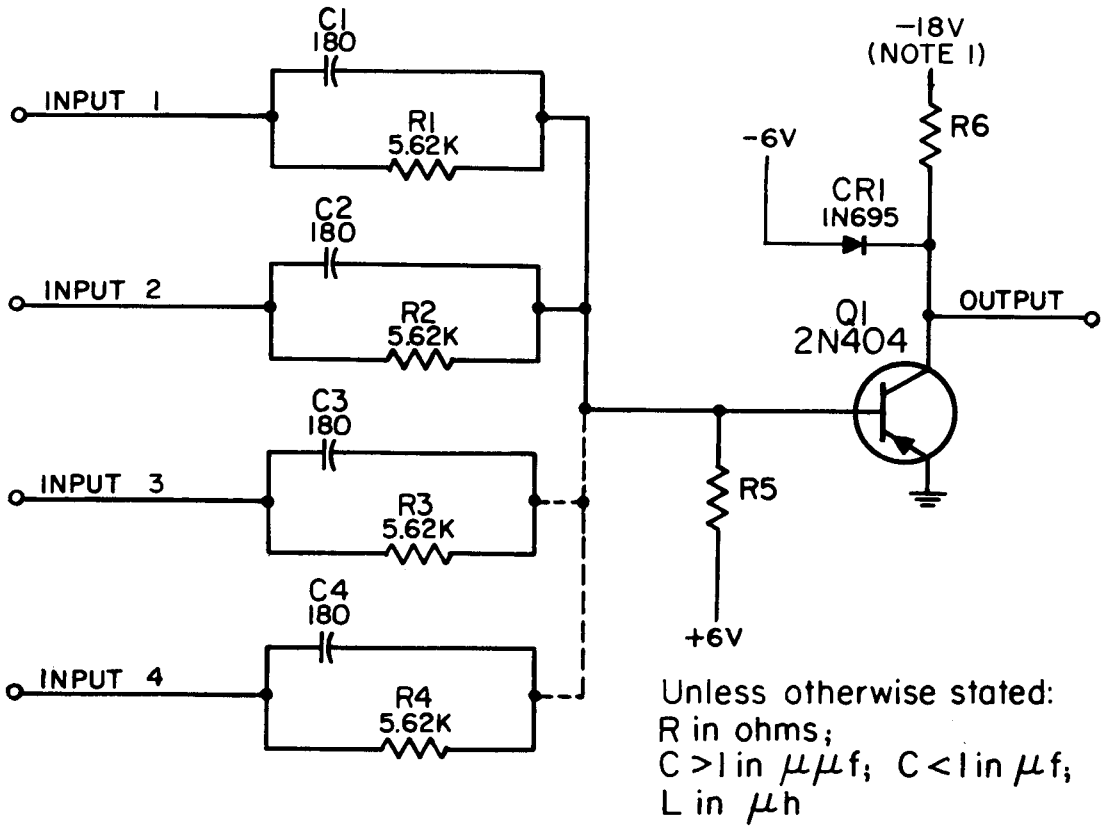


Figure 202–8.—PC 202 with one transistor removed

conditions with one transistor disabled. The circuit under these conditions is shown in figure 202–8. The emitter, base, and collector of the operating transistor are labeled E, B, and C, respectively, while the terminals to which the removed transistor had been connected are labeled with primes. In figure 202–7 (c), the base voltage clipping due to the flow of base current is obvious when compared to the open circuit measurements of (d). The top waveform, (a), which shows the variation of voltage across the emitter-collector of the transistor remaining in the circuit of figure 202–8, can best be understood by starting at point A on the curve. At this point, the voltage from emitter to collector is approximately equal to the supply voltage. Because the base is forward biased by the voltage divider R1,R3, current begins to flow in the collector-emitter circuit and the transistor turns rapidly on as it did when there were two transistors in the circuit. However, with only one transistor operating, the core is not starting from negative saturation, but from a point near zero flux density, and the flat portion of the curve is much shorter than for normal operation with two transistors. When the core saturates and the rate of change of flux reverses, the base emitter voltage reverses and biases the single operating transistor from "on" to "off". The energy stored in the transformer now dissipates via the coupled secondary load and allows the back emf across the transistor to drop toward the supply potential, as shown by the diagonal portion of the waveform. At this point there is insufficient reverse bias to overcome the forward bias supplied by the voltage divider R1,R3, and the cycle repeats.

NBS PREFERRED CIRCUIT NO. 210
NOR GATE, GENERAL PURPOSE, 2 AND 4 INPUT

NBS PREFERRED CIRCUIT NO. 210
NOR GATE, GENERAL PURPOSE, 2 AND 4 INPUT



Components:

	2 Input Gate	*4 Input Gate*
R5:	26.1KΩ	21.5KΩ
R6:	2.15KΩ	2.61KΩ

Maximum power dissipation: R1, R2, R3, R4, R5: 8 mw; R6: 200 mw.
Limits (these are not tolerances; see note 2): All R: ±5%. All C: ±10%.

Operating characteristics:

Temperature range: −30° C to +60° C.
Input impedance: One "G" load. (See section 2.3.)
Input signal characteristics:
Level (Note 3):
Logical "1": −6.2 volts ±10% at 1.2 ma maximum.
Logical "0": −0.15 volts.
Pulse (Note 4):
Polarity: Positive or negative.
Amplitude: 6 volts ±10%.
Width at 50% amplitude: 0.8 μsec minimum; 5 μsec maximum.
Rise time (Note 5): ≤0.2 μsec.

(Specifications continued on next page)

Operating characteristics: (Continued)
Switching characteristics (note 6):

Input signal	Output signal
Level change from 0 v to −6 v with rise time of 1.4 μsec.	Level change from −6 to 0 v. Turn-on time (Note 7): 1.6 μsec max. Delay time: 0.9 μsec. max. Rise time: 0.7 μsec max.
Level change from −6 v to 0 v with rise time of 0.5 μsec.	Level change from 0 v to −6 v. Turn-off time (Note 8): 1.3 μsec max. Storage time: 0.4 μsec max. Rise time: 0.9 μsec max.
Negative-going pulse with rise time of 0.2 μsec.	Positive-going pulse. Turn-on time: 0.35 μsec max. Delay time: 0.15 μsec max. Rise time: 0.2 μsec max.
Positive-going pulse with rise time of 0.2 μsec.	Negative-going pulse. Turn-off time: 0.35 μsec max. Storage time: 0.15 μsec max. Rise time: 0.2 μsec max.

Maximum load: (See section 2.3.)

Circuit	Type of output			
	Direct current	Level	Positive pulse	Negative pulse
2 input gate	4 ma at −6.2 v ±10%.	Maximum of 4 loads, no more than 2 of which are F loads.	4 loads F or G	One G load only.
4 input gate	3.5 ma at −6.2 v ±10%.	Maximum of 3 loads, no more than 2 of which are F loads.	3 loads F or G	One G load only.

Power requirements:

Voltages	Current	
	2 Input gate	4 Input gate
−18 v ±10%	9.5 ma	8 ma
−6 v ±10%	9.5 ma	8 ma
+6 v ±10%	0.27 ma	0.33 ma

(For notes, see next page)

NOTES:

1. The −18 volt supply is obtained by connecting a −12 volt source in series with the −6 volt supply. (See section 2.4.)

2. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified. Thus the term "limits" includes the initial tolerance plus the drifts caused by environmental changes or aging.

3. The minimum duration of a level is 5 μsec.

4. Positive pulses are referenced to −6.2 volts ±10%. Negative pulses are referenced to ground (actually about −0.15 volt).

5. Rise time is used in the usual pulse sense to mean the time required for the leading edge of the waveform to change from 10% to 90% of its maximum amplitude.

6. Maximum switching times were obtained by operating the circuit with the worst combination of limit transistors, components, supply voltages, and temperature. The load in each case was maximum for that type of operation.

7. The turn-on time is the time required for the collector voltage to complete the first 90% of its total amplitude change when the transistor is turned on. It is measured from the instant that the signal applied to the transistor to turn it on completes 10% of its amplitude change, and includes the delay time (the time required for the first 10% change in collector voltage) and the rise time (the time required for the voltage change from 10% to 90%).

8. The turn-off time is the time required for the collector voltage to complete the first 90% of its total amplitude change when the transistor is turned off. It is measured from the instant that the signal applied to the transistor to turn it off completes 10% of its amplitude change, and includes the storage time (the time required for the first 10% change in collector voltage) and the rise time (the time required for the voltage change from 10% to 90%).

PC 210 NOR GATE, GENERAL PURPOSE, 2 AND 4 INPUT

1. APPLICATION

PC 210 performs the general purpose AND, OR, and inversion functions in a compatible set of digital logic circuits [1] for use in computer, control, and communication equipment operating within the temperature limits of −30 and +60° C. It can be used as (1) an AND gate for positive levels, or positive-going pulses; (2) an OR gate for negative levels, or negative-going pulses; and (3) an inverter for positive or negative-going pulses or levels. It cannot be used as an AND gate for pulses when a spurious output pulse can cause errors; under these conditions, PC 211, the pulse gate, must be used. (See sec. 2.2.)

2. DESIGN CONSIDERATIONS

From the logistic and maintenance standpoints, it is impractical to design a different NOR gate [2] for every possible number of inputs. The usual solution is to select a multiple input gate as the standard building block. If more inputs are required, they can be formed by combination of the standard building blocks. If fewer inputs are required, the unused terminals are grounded. PC 210 is designed for two- and four-input circuits since this system offers maximum flexibility for gate operation. When PC 210 is used as an inverter, the two-input circuit is used with one input grounded. Thus one circuit is capable of performing three of the five basic computer functions.

2.1 *Circuit Configuration:* A single-transistor common-emitter amplifier operating as a NOR gate was chosen for the general purpose gate function. When the circuit is used as an AND gate, the transistor is normally on and cannot be turned off unless all the inputs are simultaneously at their most positive voltage (zero volts). When the circuit is operating as an OR gate, the transistor is normally off and can be turned on by any of the inputs which change from zero to a −6 volt level. If more than one of the inputs is driven negative, the transistor is driven deeper into saturation, but the output signal is unaffected. PC 210 can be used as an inverter by using the 2-input gate and grounding the unused input.

The output is clamped to −6 volts in the OFF state by diode CR1 and to ground in the ON state by the saturated transistor. The positive 6-volt bias supply, together with the resistor R5, provides a current bias which prevents I_{CBO} flow in the base region during cut-off condition, and therefore prevents I_{CBO} multiplication. The clamped operation using CR1 standardizes the magnitude of the output pulses and levels.

Clamped operation also increases the speed of the ON to OFF transition in two ways. First, limiting the maximum magnitude of the input signal by clamped-driving circuits limits the number of the minority carriers stored in the base of the driven circuit. This in turn allows the minority carriers to be cleared out of the base more rapidly in the ON to OFF transition, and therefore decreases storage time.[3] Second, the rise time of the output voltage is decreased because the voltage change is limited by the clamp to the initial portion of an exponential waveform.

The change from a 2-input to a 4-input gate is accomplished by changing the resistance of R5 and R6 and adding two RC input circuits. When PC 210 is used as an inverter for positive-going signls, the AND gate output-loading restrictions apply. When it is used as an inverter for negative-going signals, the OR gate output-loading restrictions apply.

2.2 *AND Circuit Operation:* During AND gate operation a spurious pulse can appear at the output.[4] Assume all inputs to the gate are initially at −6 volts and then one input is driven positive. A positive transient will feed through the input capacitor and drive minority carriers out of the base region. In transistors

[1] See also Preferred Circuits 211 through 216.

[2] A NOR gate is a circuit which is capable of operating either as an AND gate or as an OR gate. For a glossary of digital computer terms see Notes to the Preferred Circuits Manual, section 17.

[3] For a definition of storage time, see note 8, p. 210–4.

[4] A. I. Pressman, *Design of Transistorized Circuits for Digital Computers*, John F. Rider, Inc., N.Y., 1959, pp. 210–212.

with low minority-carrier storage characteristics, this depletion of minority carriers will cause the transistor to turn off temporarily, and a spurious output pulse will result. The magnitude and duration of this unwanted output pulse could be reduced if the input capacitor were reduced in magnitude to limit the minority carrier removal during the transient. Use of a smaller capacitor, however, would prevent a pulse from turning the transistor on under worst operating conditions when the circuit was being used as an OR gate or as an inverter for negative-going pulses.

The spurious output pulses cause no difficulty when the output of the AND gate is eventually directed to the resistive input of a bistable multivibrator, such as PC 212. The resistive inputs are integrating networks with a time constant sufficient to prevent the maximum amplitude and duration of the spurious pulses from causing an unwanted signal. If the AND function must be performed on a mixture of levels and pulses and the gate output must drive a load other than the resistor inputs a, c, e, or g of PC 212, the pulse gate, PC 211, must be used.

2.3 *Input Impedances and Loads:* The maximum load that can be driven by any of the digital circuits is determined by the effect of the load on the rise time of the output signal. To simplify the loading rules, the input impedance and maximum load for each circuit of the set of digital logic circuits, PC 210 through PC 216, are abitrarily given in terms of "F" and "G" loads. The "G" (gate) load is equivalent to the input impedance of PC 210; the "F" (flip-flop) load is derived from the input impedance of the bistable miltivibrator, PC 212.

The equivalent circuit of each of these loads is shown in figure 210–1. The actual load impedance may vary somewhat from the equivalent circuit describing it; however, allowances were made for this in formulating the loading rules. The two forms of the "F" load represent the two methods of coupling into the flip-flop. Because the transistor loads the junction of the resistor and capacitor in the actual input circuit of the flip-flop, the "F" load is a less accurate approximation than the "G" load.

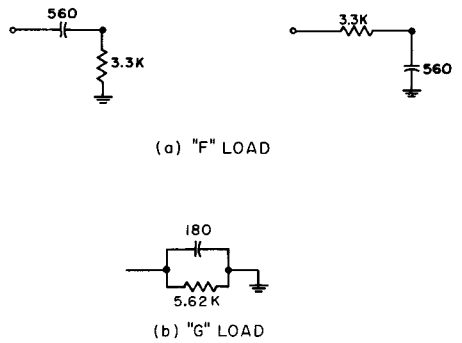


Figure 210–1.—Equivalent circuits of loads and input impedances.

2.4 *Power Supplies*: The −18 volt supply should be obtained by connecting the positive side of a 12 volt floating source to the −6 volt supply. In this way the clamping diode current can be maintained when the transistor is biased off without causing reverse current flow in the −6 volt supply. If the −18 volts is supplied from a separate source and the transistor is off, the clamping diode current will be maintained by a current from the −18 volt supply flowing in the reverse direction through the −6 volt supply, because the two supplies will be connected in series opposition.

Supply voltages should not deviate more than 10% from the nominal values of 6 volts, −6 volts, and −18 volts. The noise level on the −6 volt supply must not exceed 1.7 volts in peak magnitude to prevent spurious triggering of loads such as bistable multivibrator PC 212

When PC 210 is used in a system, additional filtering of power leads is required to keep external and system induced noise to tolerable levels. This problem is discussed at length in Notes to the Preferred Circuits Manual, section 17.

3. PERFORMANCE

Input and output waveforms for typical operation of the general purpose NOR gate, PC 210, are shown in figures 210–2 and 210–3. All traces were obtained at a sweep speed of 0.2 μsec per centimeter. Only the two-input gate operation is illustrated since the waveforms for the four-input version do not differ significantly from those shown.

Figure 210–2 shows the output of PC 210 when the input is a positive pulse. Since the

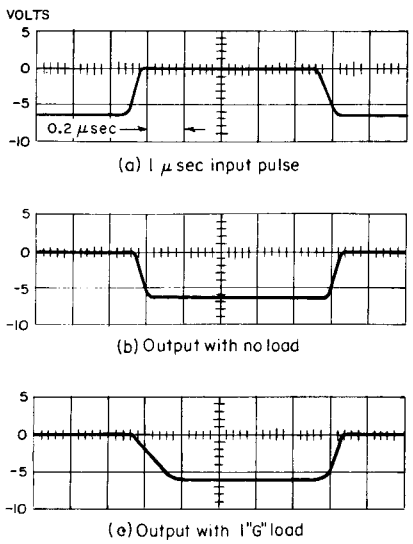


Figure 210-2.—Typical waveforms for 2 input gate with positive input signal.

input waveform is not significantly affected by output loading, only one input trace is illustrated. Maximum output loading is determined by the deterioration permissible in the rise time of the output waveform. The rise time in turn is determined by the time constant of the circuit consisting of the load in parallel with the transistor collector resistor, since the transistor is off during this transition. Comparison of waveforms (b) and (c) shows that the output waveform rise time deteriorates rapidly, although with 1 "G" load, it is within the specified 0.2 μsec maximum.

For a negative input pulse (figure 210-3), the leading edge of the output waveform is generated by the discharge of the load capacitor through the transistor. The rise times are faster than they are with positive inputs, since the resistance in parallel with the load now includes the saturation resistance of the transistor, but they are more dependent on transistor characteristics, such as the saturation resistance, beta, and delay time. As indicated

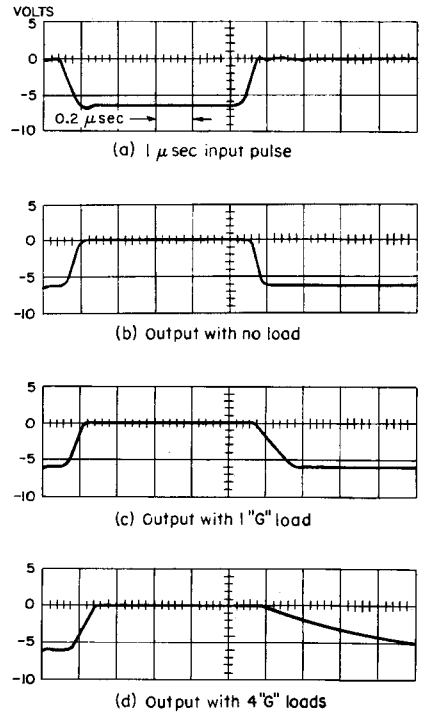
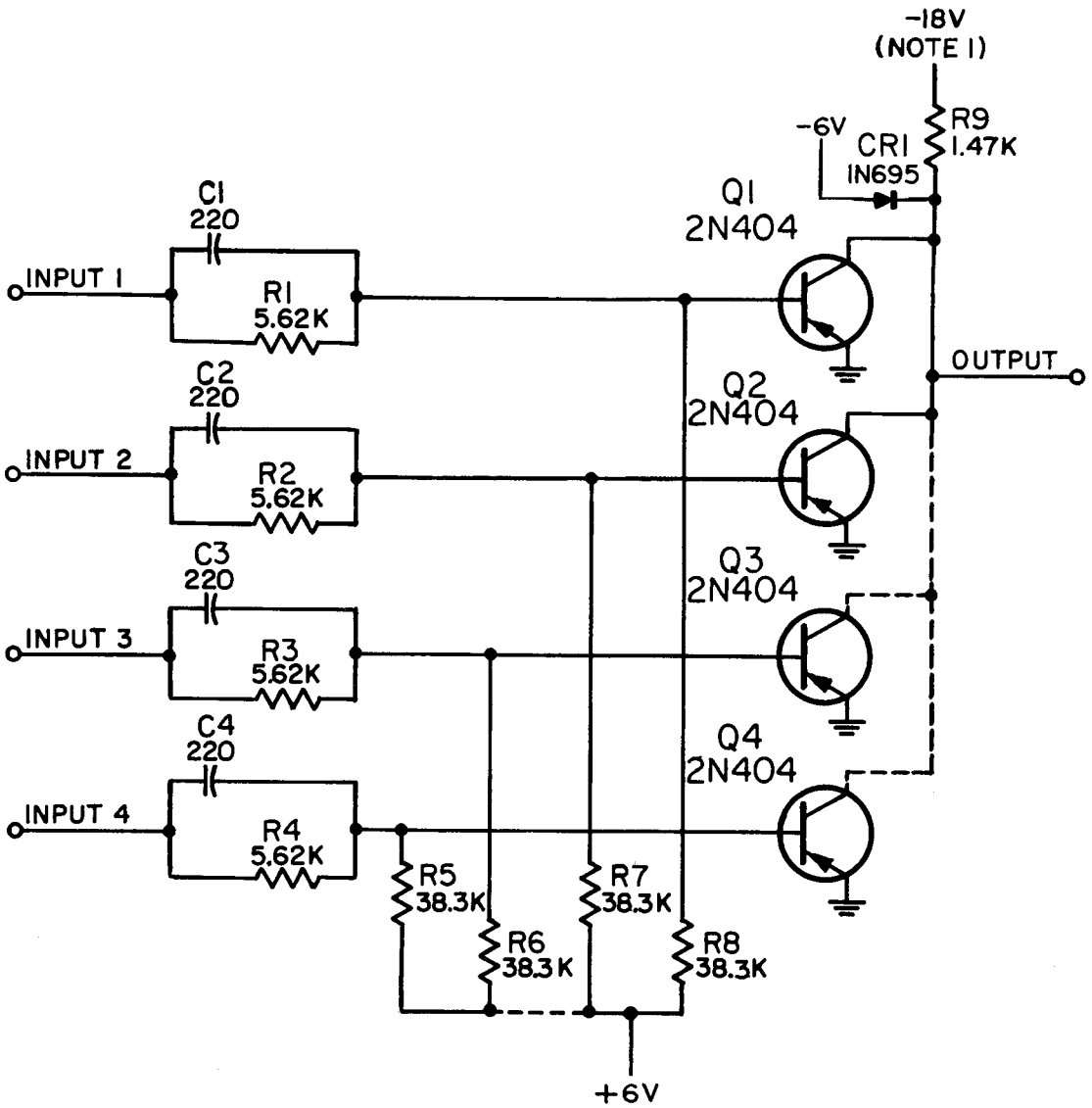


Figure 210-3.—Typical waveforms for 2 input gate with negative input signal.

in (d), the rise time with 4 "G" loads is still within the 0.2 μsec maximum. The trailing edge of the output waveforms illustrates the increase in turn-off time as the load on the circuit is increased.

NBS PREFERRED CIRCUIT NO. 211
NOR GATE, PULSE, 2 AND 4 INPUT

NBS PREFERRED CIRCUIT NO. 211
NOR GATE, PULSE, 2 AND 4 INPUT



Unless otherwise stated; R in ohms; C>1 in $\mu\mu$f; C<1 in μf; L in μh

Components:

Maximum power dissipation: R1, R2, R3, R4: 8 mw; R5, R6, R7, R8: 2 mw; R9: 300 mw.
Limits (these are not tolerances; see note 2): All R: $\pm 5\%$. All C: $\pm 10\%$.

(Specifications continued on next page)

Operating characteristics:

Temperature range: −30° C to +60° C.

Input impedance: One "G" load. (See section 2.1)

Input signal characteristics:

Level (Note 3):

Logical "1": −6.2 volts ±10% at 1.2 ma maximum.

Logical "0": −0.15 volts.

Pulse (Note 4):

Polarity: Positive or negative.

Amplitude: 6 volts ±10%.

Width at 50% amplitude: 0.8 μsec minimum; 5 μsec maximum.

Rise time (Note 5): ≤0.2 μsec.

Switching characteristics (Note 6):

Input signal	Output signal
Level change from 0 v to −6 v with rise time of 1.4 μsec.	Level change from −6 to 0 v. Turn-on time (Note 7): 1.6 μsec max. Delay time: 0.9 μsec max. Rise time: 0.7 μsec max.
Level change from −6 v to 0 v with rise time of 0.5 μsec.	Level change from 0 v to −6 v. Turn-off time (Note 8): 1.2 μsec max. Storage time: 0.4 μsec max. Rise time: 0.8 μsec max.
Negative-going pulse with rise time of 0.2 μsec.	Positive-going pulse. Turn-on time: 0.35 μsec max. Delay time: 0.15 μsec max. Rise time: 0.2 μsec max.
Positive-going pulse with rise time of 0.2 μsec.	Negative-going pulse. Turn-off time: 0.33 μsec max. Storage time: 0.15 μsec max. Rise time: 0.18 μsec max.

Maximum load: (See section 2.1.)

Circuit	Type of output			
	Direct current	Level	Positive pulse	Negative pulse
2 and 4 input gates.	6 ma at −6.2 v ±10%.	Maximum of 4 loads, no more than 2 of which are F loads.	Maximum of 4 loads, no more than 2 of which are F loads.	One G load only.

(Specifications continued on next page)

548679 O—60——3

Power requirements:

Voltages	Current	
	2 Input gate	4 Input gate
−18 v ±10%--	14 ma	14 ma
−6 v ±10%--	14 ma	14 ma
+6 v ±10%--	0.35 ma	0.7 ma

NOTES:

1. The −18 volt supply is obtained by connecting a −12 volt source in series with the −6 volt supply. (See section 2.2.)

2. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified. Thus the term "limits" includes the initial tolerance plus the drifts caused by environmental changes or aging.

3. The minimum duration of a level is 5 μsec.

4. Positive pulses are referenced to −6.2 volts ±10%. Negative pulses are referenced to ground (actually about −0.15 volt).

5. Rise time is used in the usual pulse sense to mean the time required for the leading edge of the waveform to change from 10% to 90% of its maximum amplitude.

6. Maximum switching times were obtained by operating the circuit with the worst combination of limit transistors, components, supply voltages, and temperature. The load in each case was maximum for that type of operation.

7. The turn-on time is the time required for the collector voltage to complete the first 90% of its total amplitude change when the transistor is turned on. It is measured from the instant that the signal applied to the transistor to turn it on completes 10% of its amplitude change, and includes the delay time (the time required for the first 10% change in collector voltage) and the rise time (the time required for the voltage change from 10% to 90%).

8. The turn-off time is the time required for the collector voltage to complete the first 90% of its total amplitude change when the transistor is turned off. It is measured from the instant that the signal applied to the transistor to turn it off completes 10% of its amplitude change, and includes the storage time (the time required for the first 10% change in collector voltage) and the rise time (the time required for the voltage change from 10% to 90%).

PC 211 NOR GATE, PULSE, 2 AND 4 INPUT

1. APPLICATION

PC 211 is a special purpose NOR gate designed for use in computer, control, and communication equipment operating within the temperature limits of −30 and +60° C. It is used only for the AND operation when the general purpose NOR gate, PC 210, would prove unsatisfactory due to the possible occurrence of spurious pulses in the output. PC 211 should not be used as an OR gate or for inversion because in these applications it offers no advantage over PC 210 and is wasteful of transistors and power.

2. DESIGN CONSIDERATIONS

PC 211 is similar to PC 210 except that it employs one transistor per input. It is similar to all the circuits of the digital logic set [1] in that current bias is used to prevent I_{CBO} flow in the base region, and clamped operation is used to obtain the benefits of standardization of the output voltage amplitude and speed up of the ON to OFF transition.

The value of the speed-up capacitors in the input circuits of the transistors has been increased to 220 $\mu\mu$f from the 180 $\mu\mu$f used in PC 210. This increases the turn-off speed and compensates for the effect of the output capacitance of the additional transistors. It also increases the load presented to the driving circuit, but this is offset by the decrease in the number of input RC circuits to one per transistor. Hence, the input impedance of PC 211 is the same as that of PC 210.

When PC 211 is used as an AND gate, spurious output pulses are prevented because the output terminal is clamped to ground if any of the transistors are conducting. If all inputs are at the −6 volt level and one input changes to the zero volt level, the transistor associated with that input will be cut off, but all the other transistors will remain on in saturation and the output voltage will not change.

2.1 *Input Impedances and Loads:* The maximum load that can be driven by any of the digital circuits is determined by the effect of the load on the rise time of the output signal. To simplify the loading rules, the input impedance and maximum load for each circuit of the set of digital logic circuits, PC 210 through PC 216, are arbitrarily given in terms of "F" and "G" loads. The "F" (flip-flop) load is derived from the input impedance of the bistable multivibrator, PC 212. The "G" (gate) load is equivalent to the input impedance of the general purpose NOR gate, PC 210.

The equivalent circuit of each of these loads is shown in figure 211-1. The actual load impedance may vary somewhat from the equivalent circuit describing it. Allowances were made for this, however, in formulating the output loading rules. The two forms of the "F" load represent the two methods of coupling into the flip-flop. Because the transistor loads the junction of the resistor and capacitor in the actual input circuit of the flip-flop, the "F" load is a less accurate approximation than the "G" load.

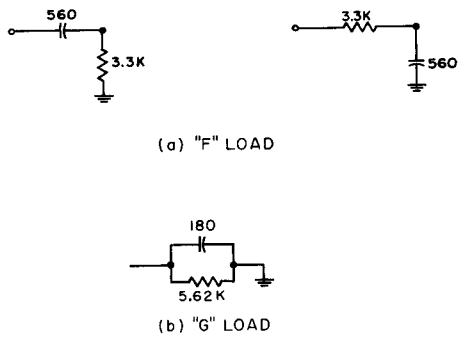


Figure 211-1.—Equivalent circuits of loads and input impedances.

2.2 *Power Supplies:* The −18 volt supply should be obtained by connecting the positive side of a 12-volt floating source to the −6 volt supply. In this way the clamping diode current can be maintained when the transistor is biased off without causing reverse current flow in the −6 volt supply. If the −18 volts is supplied from a separate source and the transistor is off, the clamping diode current will be maintained by a current from the −18 volt supply flowing in the reverse direction through the −6-volt supply,

[1] See also Preferred Circuits 210 through 216 and Notes to the Preferred Circuits Manual, section 17.

because the two supplies will be connected in series opposition.

Supply voltages should not deviate more than 10% from the nominal values of 6 volts, −6 volts, and −18 volts. The noise level on the −6 volt supply must not exceed 1.7 volts in peak magnitude to prevent spurious triggering of loads such as bistable multivibrator PC 212.

When PC 211 is used in a system, additional filtering of power leads is required to keep external and system induced noise to tolerable levels. This problem is discussed at length in Notes to the Preferred Circuits Manual, section 17.

3. PERFORMANCE

The performance of PC 211 as an AND gate is illustrated by figure 211–2. Only waveforms for the two-input gate are shown, since the performance of the four-input version is not signficantly different. No curves of the OR operation are included, because PC 211 is not intended for such use. All traces were obtained at a sweep speed of 0.2 μsec per centimeter.

Only one input signal is shown in trace (a), since the input signal is not significantly affected by output loading. The traces of the output signals for no load and 1 "G" load (traces (b) and (c) respectively) do not differ significantly from those of PC 210 when used as an AND gate.

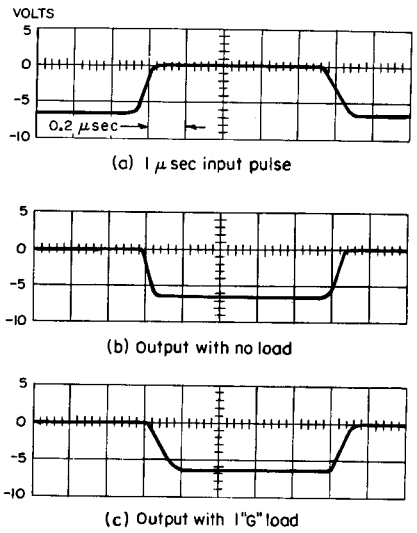
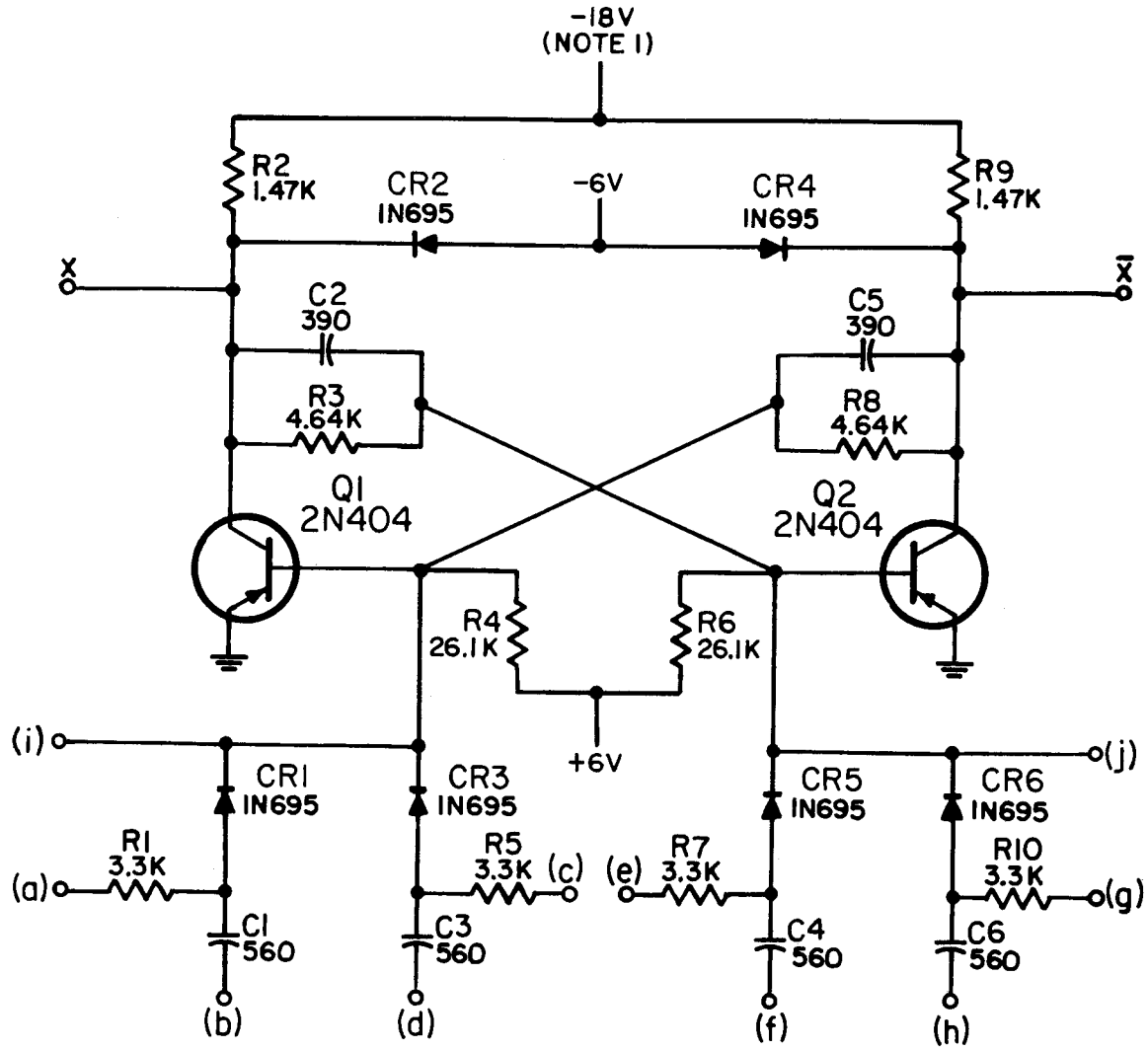


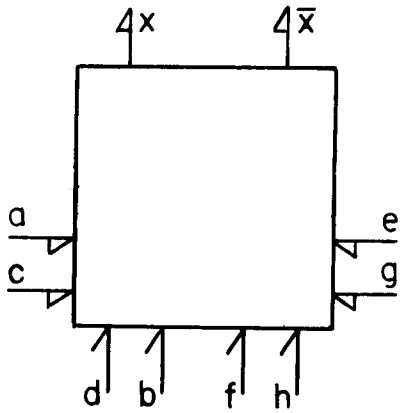
Figure 211–2.—Typical waveforms for 2-input AND gate.

NBS PREFERRED CIRCUIT NO. 212
MULTIVIBRATOR, BISTABLE (150 KC)

NBS PREFERRED CIRCUIT NO. 212
MULTIVIBRATOR, BISTABLE (150 KC)



Unless otherwise stated: R in ohms; C>1 in $\mu\mu$f; C<1 in μf; L in μh



Symbol for PC 212

(For specifications, see next page)

Components:

Maximum power dissipation: R1, R4, R5, R6, R7, R10: <5 mw; R3, R8: 10 mw; R2, R9: 0.25 watt.

Limits (these are not tolerances; see note 2): R1, R5, R7, R10: ±20%; all other R: ±5%. All C: ±10%.

Operating characteristics:

Temperature range: −30° C to +60° C.

Maximum operating rate: 150 kc. (See section 2.2.)

Input impedance: One "F" load. (See section 2.4.)

Input signal characteristics (terminals *b*, *d*, *f*, and *h*):

Polarity: Positive.

Amplitude: 6 volts reference to −6.2 volts ±10%.

Rise time: ≤0.4 μsec.

Width at 50% amplitude: 0.8 μsec minimum.

Switching and output characteristics under worst operating conditions:

Output	Level change	Maximum switching time (note 3)	Maximum load
Collector of transistor switching from off to on.	−6 v to 0 v	Turn on time (note 4): 0.9 μsec. Delay time: 0.5 μsec. Rise time: 0.4 μsec.	4 RC loads, type "F" or "G." (See section 2.4.)
Collector of transistor switching from on to off.	0 v to −6 v	Turn off time (note 5): 1.6 μsec. Storage time: 0.2 μsec. Rise time: 1.4 μsec.	4 RC loads, type "F" or "G." (See section 2.4.) DC load: 5 ma ±10%.

Power requirements:

−18 volts ±10% at 24 ma.

−6 volts ±10% at 24 ma.

+6 volts ±10% at 0.5 ma.

NOTES:

1. The −18 volt supply is obtained by connecting a −12 volt source in series with the −6 volt supply. (See section 2.5.)

2. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.

3. Maximum switching times were obtained by operating the circuit with the worst combination of limit transistors, components, supply voltages, and temperature, and with 4 loads connected to each output. See figures 212-6 and 212-7 for the effects of the load.

4. The turn-on time is the time required for the collector voltage to complete the first 90% of its total amplitude change when the transistor is turned on. It is measured from the instant that the signal applied to the transistor to turn it on completes 10% of its amplitude change, and includes the delay time (the time required for the first 10% change in collector voltage) and the rise time (the time required for the voltage change from 10% to 90%).

5. The turn-off time is the time required for the collector voltage to complete the first 90% of its total amplitude change when the transistor is turned off. It is measured from the instant that the signal applied to the transistor to turn it off completes 10% of its amplitude change, and includes the storage time (the time required for the first 10% change in collector voltage) and the rise time (the time required for the voltage change from 10% to 90%).

PC 212 MULTIVIBRATOR, BISTABLE (150 KC)

1. APPLICATION

PC 212 is a bistable multivibrator designed as the storage element in a compatible set of digital logic circuits [1] for use in computer, control, and communications equipment operating within the temperature limits of −30 and +60° C. It operates in conjunction with input diode gates which are an integral part of the circuit. For maximum versatility, direct connection is also provided to the base of each transistor. PC 212 can be used as a counter and as a serial or parallel shift register at operating rates up to 150 kc under maximum load.

2. DESIGN CONSIDERATIONS

PC 212 consists of two grounded-emitter amplifiers, similar to the circuit of PC 210, with the output of each tied to the input of the other. The transistors are stabilized against I_{CBO} multiplication by resistors returned to a positive 6-volt potential. One output is clamped to −6 volts by diodes CR2 or CR4 and the other to ground (maximum −0.15 volts) by the saturated ON transistor. The diode gates, CR1, R1, C1; CR3, R5, C3; CR5, R7, C4; and CR6, R10, C6, are an integral part of the circuit.

2.1 *Circuit Operation*: Operation of the circuit is best described if it is assumed that the circuit is in a quiescent state, with Q1 off and Q2 on. The voltage at the collector of Q1 is then −6.2 volts (6 volts clamping plus the drop of −0.2 volts across diode CR2). This voltage causes sufficient current to flow through R3 from the base of Q2 to keep Q2 in saturation. Since Q2 is saturated, its collector is approximately at ground potential, and Q1 is held in the OFF condition by the positive bias (approximately 1 volt) applied to its base by the divider R4, R8.

To change the state of the multivibrator, a positive-going pulse is applied to the base of the ON transistor, Q2. After a delay caused by the base storage of minority carriers, Q2 begins to turn off, and the voltage at its collector begins to fall at a rate determined primarily by the RC network (which includes all loads) tied to its collector. This negative voltage change at the collector of Q2 is coupled back to the base of Q1 through the feedback network, C5, R8, and initiates the turn-on process in Q1. After a delay which depends on the characteristics of the transistor, the voltage at the collector of Q1 starts to rise, and the change is coupled to the base of Q2. The transition then proceeds regeneratively until Q1 is on and Q2 is off. Since the switching is not completely regenerative, the input pulse generator must provide a sink for the minority carriers stored in the base of Q2 and must maintain the base of Q2 at ground potential until Q2 has begun to turn off.

2.2 *Diode Gates:* The diodes connected to the transistor bases offer low resistance paths to positive-going input signals and discriminate against negative-going waveforms. The diodes may be primed, i.e., biased to allow easy flow of forward current, by bringing the associated resistive input connection (*a*, *c*, *e*, or *g*) to ground potential. They can be inhibited, i.e., biased to prevent the flow of forward current, by lowering the voltage at the resistive input to −6 volts. (The actual voltage is −6.2 volts ±10%, and the ground potential may be as large as −0.15 volts. For brevity, however, these values are referred to as −6 volts and ground potential.) The 1.85 μsec time constant of the diode gates determines the maximum operating rate of the multivibrator. More than three time constants are allowed for the gates to settle at the fastest operating rate (150 kc).

2.3 *Binary cells:* The binary cell is the elementary storage unit of a digital computer. The common binary cell connections discussed in this section are illustrated by means of block diagrams which are labeled to correspond with PC 212. The nomenclature used is taken from *Logical Design of Digital Computers.* [2]

The response of a binary cell to a positive pulse depends on the condition of both the diode gate and the multivibrator at the time that

[1] See also Preferred Circuits 210 through 216 and Notes to the Preferred Circuits Manual, section 17.

[2] M. Phister, *Logical Design of Digital Computers*, John Wiley and Sons, Inc., New York, 1958.

the pulse is applied. A positive trigger applied to one of the pulse inputs of PC 212 (*b*, *d*, *f*, or *h*) will cause the multivibrator to change states only if the diode gate is primed, and if the associated transistor is in the ON state. The ON transistor may be identified in figures 212–1 through 212–4 as the one with the "0" output.

(*a*) T connection: When the T connection, figure 212–1, is used, the multivibrator changes state once for each positive pulse applied to the T input. One of the diode gates, *ab* or *ef*, is always primed because of the connection of the resistive inputs *a* and *e* to the outputs X and $\overline{X}$, respectively. If the cell is originally in the "1" state,[3] as shown in the figure, a positive pulse put into T will flow through *f*, because the associated diode is primed by connection to the "0" output at $\overline{X}$, and the diode gate *ab* is inhibited by connection to the "1" output at X. This pulse will cause the multivibrator to change state and in so doing will prime the diode gate *ab* so that the binary is ready for the next pulse. Diode gates *cd* and *gh* are not needed in the T connection and are inhibited by connection to the −6 volt source to prevent spurious signals or pickup at *d* and *h* from interfering with the operation of the cell.

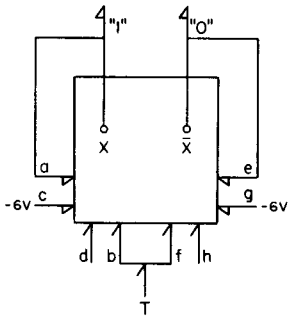


Figure 212–1.—T connection.

(*b*) RS connection: In the RS connection, shown in figure 212–2, both the *cd* and *gh* gates are always primed, and positive input pulses must be directed to the proper gate to cause the cell to change state. If the counter is in the "1" state as shown, a positive pulse directed to the *h* input will cause the cell to change to the zero state, but a positive signal directed to the *d* terminal will have no effect. Once the counter changes to the "0" state a positive pulse must be directed to the *d* input to again put the binary in the "1" state. The R input, terminal *h*, is the reset input since it is used to place the binary cell in the "0" state. The S input, terminal *d*, is the set input since it is used to place the binary in the "1" state. If positive pulses arrive simultaneously at the R and S inputs, the action of the multivibrator is not predictable.

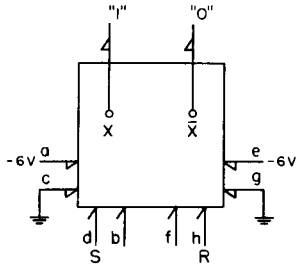


Figure 212–2.—RS connection.

(*c*) JK connection: If positive pulses can arrive simultaneously at both sides of the multivibrator, the JK connection, figure 212–3, is used. This is merely a T connection with separate trigger inputs. As in the RS connection, positive input pulses must be directed to the proper input to cause the binary cell to change its state, but only the input which is connected to the base of the ON transistor is primed. Therefore, if positive pulses come into both the J and K inputs simultaneously, only the ON transistor will receive the pulse, and the binary will change states. The JK connection is used in preference to the RS connection only when simultaneous pulses at the set and reset inputs must be dealt with.

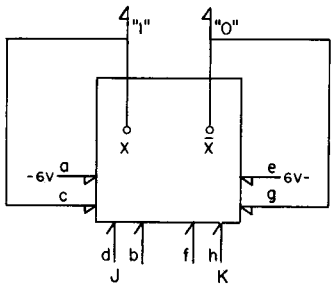


Figure 212–3.—JK connection.

[3] The output of a binary cell is said to be "1" when the indicating output (X output of PC 212) is "1" (−6 volts) and "0" when the indicating output is "0"

(*d*) RST connection: The RST connection (fig. 212-4) is the usual binary cell connection for a digital counter bit and is discussed in detail in section 4.1. It may be triggered by positive pulses directed to the T terminal, or by set and reset pulses directed in the proper order to the S and R terminals. The JKT connection can be formed by connecting the *c* and *g* terminals to the X and $\overline{X}$ outputs,

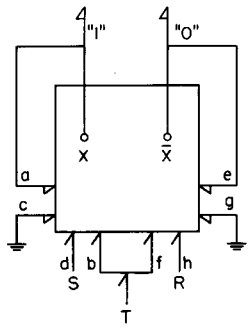


Figure 212-4.—RST connection.

respectively, instead of to ground as shown in figure 212-4. Since this constitutes double loading on the outputs, this connection is not ordinarily used.

2.4 *Input Impedances and Loads:* The maximum load that can be driven by any of the digital circuits is determined by the effect of the load on the rise time of the output signal. To simplify the loading rules, the input impedance and maximum load for each circuit of the set of digital logic circuits, PC 210 through PC 216, are arbitrarily given in terms of "F" and "G" loads. The "F" (flip-flop) load is derived from the input impedance of the bistable multivibrator, PC 212. The "G" (gate) load is equivalent to the input impedance of the general purpose NOR gate, PC 210.

The equivalent circuit of each of these loads is shown in figure 212-5. The actual load impedance may vary somewhat from the equivalent circuit describing it. Allowances were made for this, however, in formulating the output loading rules. The two forms of the "F" load represent the two methods of coupling into the flip-flop. Because the transistor loads the junction of the resistor and capacitor in the actual input circuit of the flip-flop, the "F" load is a less accurate approximation than the "G" load.

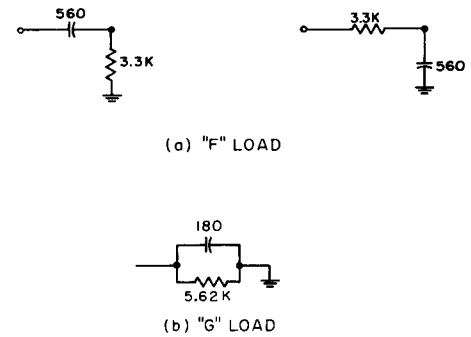


Figure 212-5.—Equivalent circuits of loads and input impedances.

2.5 *Power Supplies:* The −18 volt supply should be obtained by connecting the positive side of a 12-volt floating source to the −6 volt supply. In this way the clamping diode current can be maintained when the transistor is biased off without causing reverse current flow in the −6 volt supply. If the −18 volts is supplied from a separate source and the transistor is off, the clamping diode current will be maintained by a current from the −18 volt supply flowing in the reverse direction through the −6 volt supply, because the two supplies will be connected in series opposition.

Supply voltages should not deviate more than 10% from the nominal values of 6 volts, −6 volts, and −18 volts. The noise level on the −6 volt supply must not exceed 1.7 volts in peak magnitude to prevent spurious triggering of loads, such as other bistable multivibrators.

When PC 212 is used in a system, additional filtering of power leads is required to keep external and system induced noise to tolerable levels. This problem is discussed at length in Notes to the Preferred Circuits Manual, section 17.

3. PERFORMANCE

Figures 212-6 through 212-9 illustrate the effect of load on the performance of PC 212. All waveforms were taken at a sweep speed of 0.2 μsec per centimeter with a vertical scale of 5 volts per centimeter.

Figure 212–6 shows the waveforms at the indicating output, X, for several load combinations when the binary is being switched from 0 to 1. Under these conditions transistor Q1 is turned off by the input signal, and the voltage at its collector, which is the X output, changes from ground to −6 volts. The capacitive load on the collector must charge through a resistance roughly equivalent to the parallel combination of the load resistance, R2, and R3. The rise time of the output waveform is principally determined by the time required to charge this capacitance, and as can be seen by comparing traces b with c and d with e, the rise time of the X output for the 0 to 1 transition is a function of the load on X and is relatively unaffected by the load on $\overline{X}$.

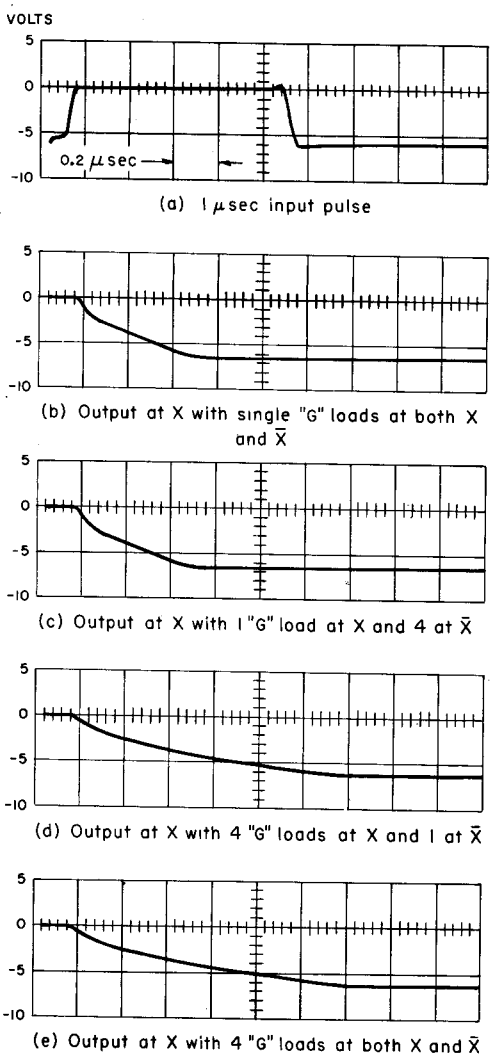


Figure 212–6.—Effects of the loads on PC 212 on the 0 to 1 transition at the X output.

Figure 212–7 shows the waveforms at the indicating output when the binary is being switched from 1 to 0, for the same load combinations as in figure 212–6. In this case Q1 is turned on by Q2, and the load on the collector of Q2, the $\overline{X}$ output, has a significant effect on the output at X, as can be seen by comparing traces b with c and d with e.

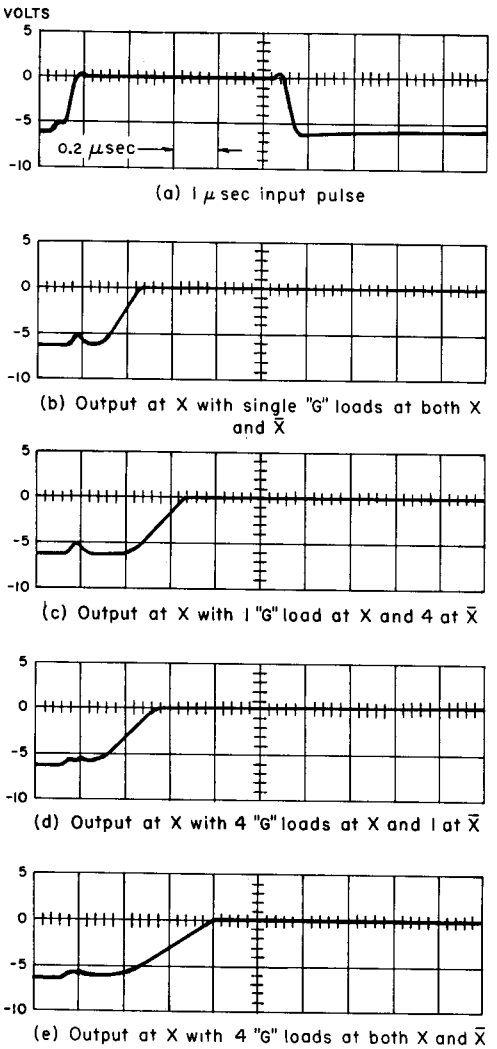


Figure 212–7.—Effects of the loads on PC 212 on the 1 to 0 transition at the X output.

The switching sequence for the 1 to 0 transition at the X output is shown in figures 212–8 and 212–9. The input pulse is applied to transistor Q2 which turns off. Q2 collector

($\overline{X}$ output) voltage falls to −6 volts relatively slowly because the capacitance connected to the collector must charge through the equivalent resistance mentioned above. By contrast, the rise of Q1 collector voltage is more rapid because the saturation resistance of the transistor furnishes an additional discharge path for the load capacitance, but there is considerable delay in the turn-on of Q1 because the base drive comes from the slowly changing collector voltage of Q2. When four "G" loads are connected to the $\overline{X}$ output (fig. 212–9), the rise time of the waveform at $\overline{X}$ is further increased, causing further delay in the turn-on of Q1. Since the load on the X output has not changed, the increase in the turn-on time of Q1 is mostly caused by the increase in delay time.

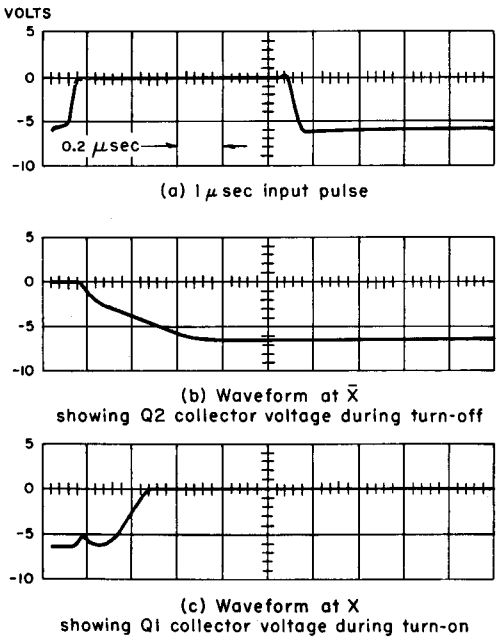


Figure 212–8.—Switching sequence showing the resetting of PC 212 with single "G" loads at both X and $\overline{X}$.

Although these waveforms (figs. 212–6—212–9) illustrate the effect of load on the waveform at the indicating output, similar results would be obtained at the $\overline{X}$ output. In general, the delay and rise times of the output waveform at a given output are proportional to the load on that output during the 0 to 1 transition, but are primarily controlled by the load on the other output during the 1 to 0 transition.

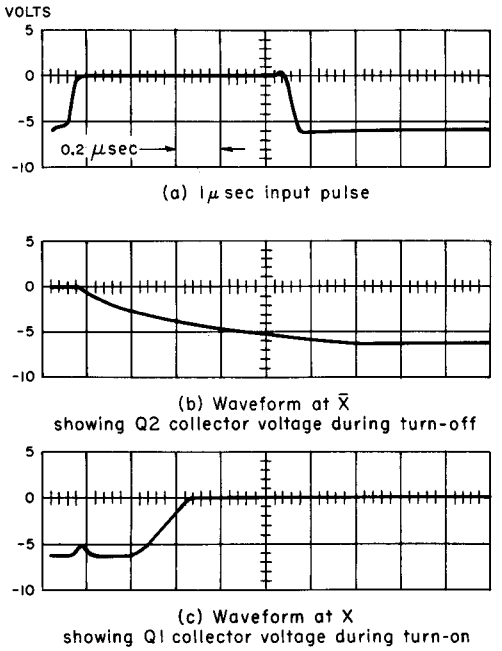


Figure 212–9.—Switching sequence showing the resetting of PC 212 with 4 "G" loads at both X and $\overline{X}$.

4. EXAMPLES OF USE

PC 212 when connected as a binary cell can indicate a "1" or a "0" and can store 1 "bit" of information; "n" such circuits can be connected in tandem to form an n-bit register to store n bits of information or an n-bit counter to count from 0 to $(2^n)-1$.

4.1 *Counters:* Four binary cells of the RST type connected as a 4-bit counter are shown in figure 212–10. The pulses to be counted are fed into the counter through the trigger (T) input of the first counter, and the indicating output of each counter except the last is fed to the trigger input of the succeeding binary. The output of the last binary may be used, for instance, to initiate the eighth or sixteenth step in a given process; or the counter may be used to count items, in which case a visual indication of the count can be had by connecting an indicator, such as PC 216, to the X terminal of each binary. Depending on the system logic, the set level and reset level connections may be primed by connecting them to ground, or they

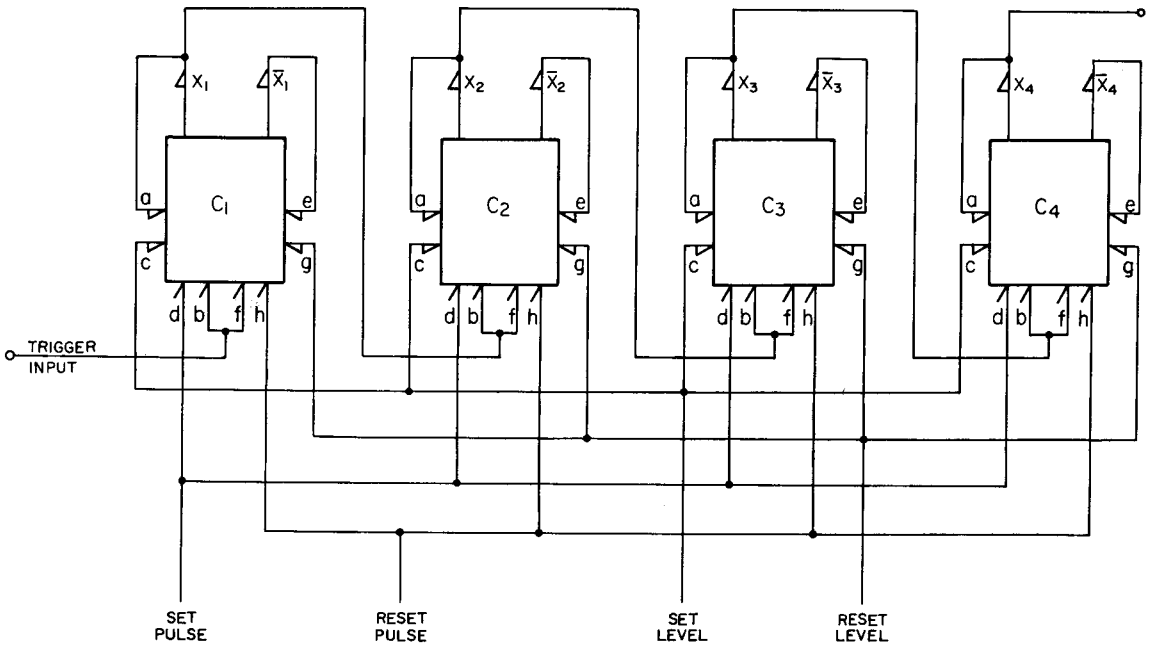


Figure 212–10.—Connections for a 4-bit binary counter.

may be connected to external logic which will inhibit them until a set or reset pulse is due to arrive.

To illustrate the operation, assume that the set and reset levels have been grounded and that a reset pulse has been put into the counter so that all the indicating outputs read "0". The first positive pulse to enter the trigger input will cause the X output of binary C1 to change from "0" to "1". This change will be coupled to the trigger input of C2, but since it is negative-going, it will have no effect on C2. When the second positive trigger pulse enters the trigger input, however, the indicating output of C1 will change from "1" to "0", and this positive-going change will cause C2 to change from "0" to "1". This change in C2 output will be coupled to the input of C3 but will not affect C3 since it is negative-going. This sequence of events will be repeated for every positive pulse or positive change of voltage at the trigger input, with each succeeding binary changing state once for every two changes of state of the preceding one. Fifteen positive input pulses or level changes would be required to cause all the binaries in figure 212–10 to read "1"

4.2 *Shift Registers:* A group of binary cells may be connected in tandem to form a shift register, which is a device capable of retaining information in the form of an ordered set of characters and of displacing that information one or more places to the left or right. Information can be inserted in such a register in parallel, i.e., in all cells simultaneously, or it can be inserted serially, in which case one bit is inserted in the first cell, then shifted to the second cell and a second bit inserted in the first cell, and the process continued until an ordered set of data has been inserted in the register. Data contained in a shift register, whether initially inserted in parallel or in serial form, can be shifted out serially when so required.

When PC 212 is used to form a shift register, a modified T connection is used, as shown in figure 212–11. The capacitive inputs of one set and one reset gate are connected together to form a common trigger terminal as in the T connection, but the resistive inputs associated with each of these gates are primed or inhibited in accordance with the data to be inserted in the cell. The input data is applied to the level gates, *a* and *e*, and is registered in the cell by the shift pulse which is applied to the common

trigger input. For proper operation, the inputs at *a* and *e* must be different, that is, if the level at *a* is "1", the level at *e* must be "0", and vice versa.

Since the function of the shift register binary is to store information, it must duplicate at its output the signal applied to the input terminals. When triggered, it must change

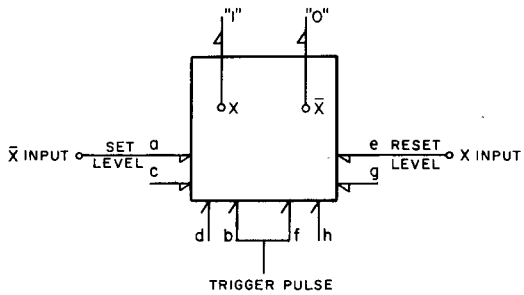


Figure 212–11.—Modified T connection used for shift register.

state if the input and output are different, but must remain in the same state if the input and output are the same, and the proper action must be determined by the level inputs. If the output of the cell is "1", as indicated in figure 212–11, and a "0" is to be shifted in, the reset side of the binary must be primed so that the trigger pulse will cause the binary to change from "1" to "0". This can be accomplished by directing the "0" to be shifted into the reset level input, terminal *e*. If a "1" is to be shifted in, it must be directed to the reset side of the binary to inhibit the reset gate and prevent a change in state. If at the same time a "0" is directed to the set level input, terminal *a*, the set gate will be primed but no change in the state of the binary will occur because this directs the trigger pulse to the OFF transistor.

If the output of the register binary is originally "0", on the other hand, and a "1" is to be shifted in, a "0" level must be directed to the set input so that the shift pulse will cause the binary to change from "0" to "1". If, at the same time, the "1" to be shifted in is directed to the reset input, it will not prevent the required change in state of the binary. If a "0" is to be shifted in, it must be directed to the reset input so that the shift pulse will be directed to the OFF transistor, preventing a change in state of the binary. Correct operation of the register binary will be obtained, therefore, if the indicating output of the driving circuit is connected to the reset side, and the opposite signal connected to the set side of the register binary.

To connect several binary cells to form a shift register, the set level of each cell is connected to the $\overline{X}$ output of the previous cell, and the reset level is connected to the X output. If the data is to be registered serially, the input to the first cell is connected to logic external to the register (a NOR gate, a second register, etc.), care being taken to continue the cross connection of set and reset level inputs as was done between cells. In the case of parallel input, however, the resistive inputs to the gates of *each* cell of the register are connected to the inserting logic. For example, if the inserted information comes from a binary counter, the reset input to each cell of the shift register is connected to the indicating output of the same ordered cell of the counter, and each set input of the register is connected to the non-indicating output of the counter. Although information may be shifted into the register either serially or in parallel, it is usually shifted out serially.

Figure 212–12 shows a two-stage shift register connected for both serial and parallel operation. The modified T connection using gates *ab* and *ef* is used for the serial shift. The trigger terminals formed by connecting terminals *b* and *f* of each of the cells are all

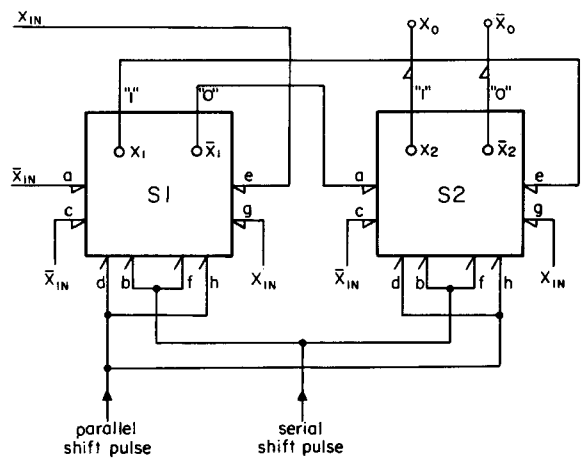


Figure 212–12.—Two-stage shift register.

connected together to form the serial shift pulse terminal, since the shift pulse is applied to all cells simultaneously. Now, however, use is made of the two extra gates of each cell *cd* and *gh* to form an additional modified T connection. The resistive inputs of each of these gates may be connected to individual cells of the data source so that data can be shifted into S1 and S2 simultaneously when a parallel shift pulse is applied.

In a shift register, the shift pulse is applied to all cells of the register simultaneously. When the register is operating serially, each cell must register the output of the preceding cell as it was prior to the shift pulse, even though this output may also be changing as the driving cell responds to the shift pulse. This is made possible by the time delay associated with the level inputs to the cell gates, which delay prevents the prime or inhibit signals on the gate diodes from changing materially during the transition period following the application of the shift pulse. The shift pulse, which is capacitively coupled to the gate diodes, has a maximum rise time of 0.4 μsec. The integrating network associated with the level input of each diode gate has a time constant of 1.85 μsec, which is sufficient to prevent a significant change in level magnitude during the transition time.

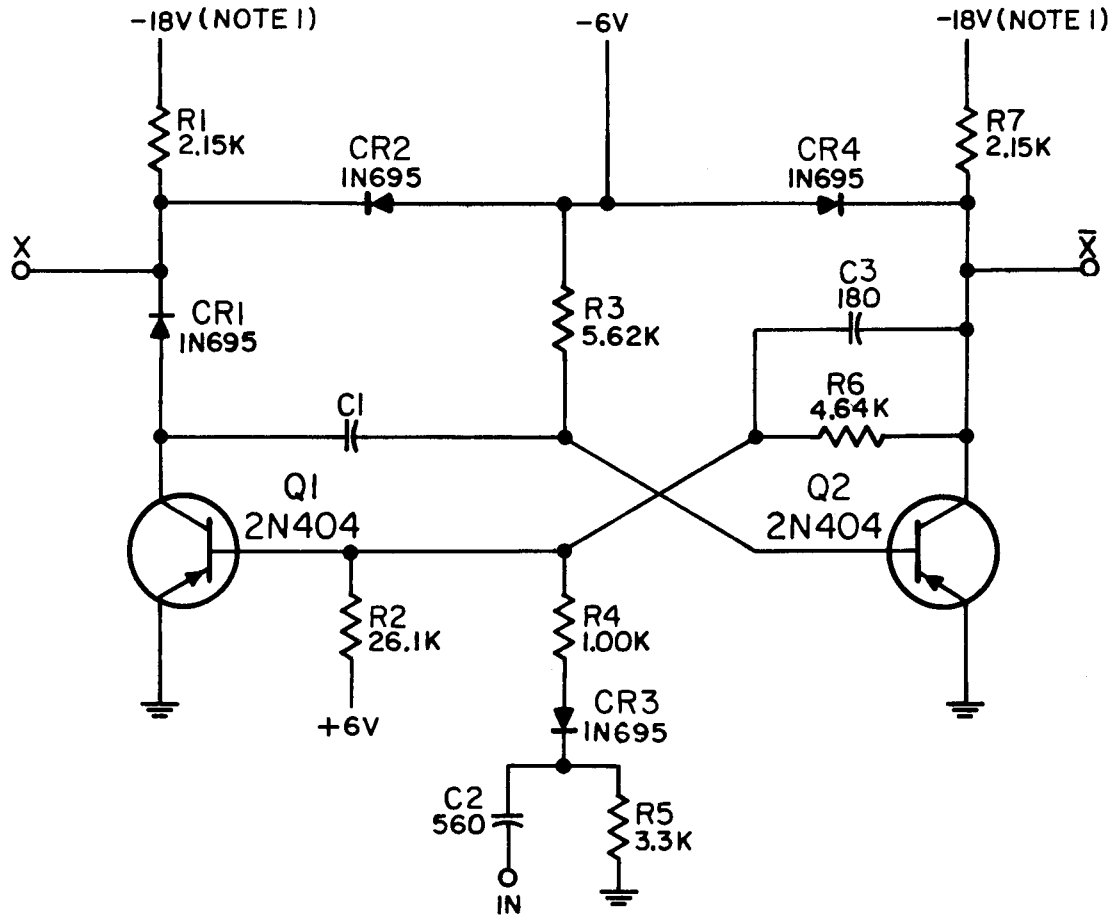
4.3 *Circuit Modifications:* The basic circuit of PC 212 can be modified to allow manual setting of individual cells in a logical array, or of entire registers or groups of registers. A normally closed switch inserted in the emitter of Q2 permits resetting of the binary by opening the switch. Since several emitters can be returned to ground through the same switch, this method permits resetting of several binaries simultaneously. The binaries can be set by placing the switch in the emitter of Q1.

Individual binaries can be set or reset by using a manually-operated, normally-open switch to temporarily ground the collector of Q2 or Q1. This is feasible because PC 212 can operate without damage to the circuit when either collector is temporarily grounded.

NBS PREFERRED CIRCUIT NO. 213
MULTIVIBRATOR, MONOSTABLE

548679 O—60——4

NBS PREFERRED CIRCUIT NO. 213
MULTIVIBRATOR, MONOSTABLE



Unless otherwise stated; R in ohms; C > 1 in $\mu\mu$f; C < 1 in μf; L in μh

Components:

C1 ($\mu\mu$f) = $\dfrac{\text{Total time delay } (\mu\text{sec})}{3.9 \times 10^{-3}}$

Maximum power dissipation: R2, R4, R5, R6: <10 mw; R3: 12 mw; R1, R7: 180 mw.
Limits (these are not tolerances; see note 2): R5: ±20%; all other R: ±5%. C1: ±5%; all other C: ±10%.

Operating characteristics:

Temperature range: −30° C to +60° C.
Total time delay (Note 3): 2 μsec to 0.1 second.
Recovery time: Approximately 25% of total time delay.
Input impedance: One "F" load. (See section 2.3.)
Input pulse characteristics:
Polarity: Negative.
Amplitude: 6 volts ±10% referenced to ground.
Rise time (Note 4): ≤0.4 μsec.
Width at 50% amplitude: 0.5 μsec minimum.

(Specifications continued on next page)

Operating characteristics—*Continued*

Switching characteristics with maximum load attached:

Output	Maximum switching time (note 5)
X	Turn-on time (note 6): 0.7 μsec. Delay time: 0.3 μsec. Rise time: 0.4 μsec. Turn-off time (note 7): $8.9 \times 10^8 \times C1$ μsec + 0.1 μsec. Storage time: 0.1 μsec. Fall time: $8.9 \times 10^8 \times C1$ μsec.
$\overline{X}$	Turn-off time: See section 3.3. Storage time: 0.2 μsec. Rise time: See section 3.3. Turn-on time: 1.0 μsec (note 8). Delay time: 0.5 μsec. Fall time: 0.5 μsec.

Maximum output load:

Output	Direct current	RC load
X	4 ma at −6.2 volts ±10%	Not used.
$\overline{X}$	3 ma at −6.2 volts ±10%	2 "F" or "G".

Power requirements:

−18 volts ±10% at 10 ma
−6 volts ±10% at 10 ma
+6 volts ±10% at 0.25 ma

NOTES:

1. The −18 volt supply is obtained by connecting a −12 volt source in series with the −6 volt supply. (See section 2.4.)

2. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.

3. The total time delay is a function of R3, C1 and is the time interval between the points where the leading edge of the input signal and the trailing edge of the output signal have completed 10% of their total amplitude change. (See section 3.1.)

4. Rise time is used in the usual pulse sense to mean the time required for the leading edge of the waveform to change from 10% to 90% of its maximum amplitude; fall time is the time required for the trailing edge of the waveform to decrease from 90% to 10% of its maximum amplitude.

5. The maximum switching times were obtained by operating the circuit with the worst combination of limit transistors, components, supply voltages, and temperature. Two RC loads were connected to the $\overline{X}$ output during these measurements.

(Notes continued on next page)

6. The turn-on time is the time required for the collector voltage to complete the first 90% of its total amplitude change when the transistor is turned on. It is measured from the instant that the signal applied to the transistor to turn it on completes 10% of its amplitude change, and includes the delay time (the time required for the first 10% change in collector voltage) and the rise time (the time required for the voltage change from 10% to 90%).

7. The turn-off time is the time required for the collector voltage to complete the first 90% of its total amplitude change when the transistor is turned off. It is measured from the instant that the signal applied to the transistor to turn it off completes 10% of its amplitude change, and includes the storage time (the time required for the first 10% change in collector voltage) and the fall time (the time required for the voltage change from 10% to 90%).

8. In this case the signal which turns the transistor on is the negative portion of the base waveform (fig. 213–4(e)). The fall time is measured, therefore, from the point where the negative portion of Q2 base voltage first reaches 10% of its final amplitude.

PC 213 MULTIVIBRATOR, MONOSTABLE

1. APPLICATION

PC 213 is a monostable multivibrator designed to perform the delay function in a compatible set of digital logic circuits [1] for use in computer, control, and communications equipment operating within the temperature limits of −30 and +60° C. Delays between 2 microseconds and 100 milliseconds can be obtained by selection of feedback capacitor C1. The timing resistor, R3, may be replaced by a variable resistor to provide adjustment of the time delay.

2. DESIGN CONSIDERATIONS

2.1 *Circuit Configuration:* PC 213 consists of two cross-coupled common-emitter circuits. It differs from the bistable multivibrator, PC 212, mainly in the cross-coupling network configuration. PC 213 is stable in only one state, because the coupling from the collector of Q1 to the base of Q2 is achieved by means of a capacitor rather than a parallel RC network. Connection of the base of Q2 to the −6 volt supply through R3 causes Q2 to remain on in saturation in the absence of external signals. As in other circuits of this group, the collector of the OFF transistor is clamped to −6 volts by diode CR2 or CR4.

Diode CR1 clips any positive-going noise peaks on the −6 volt supply and prevents them from feeding through CR2 and coupling through C1 into the base of Q2. Since Q2 is normally on, a positive pulse at the base might turn it off. Hence, CR1 is connected with a polarity which discriminates against positive pulses, but at the same time does not interfere with transistor current flow through the collector of Q1.

Diode CR3, capacitor C2, and resistor R5 comprise a diode gate similar to the gates used in the bistable multivibrator, PC 212. The chief difference is the polarity of the diode connection in PC 213, which allows a negative-going waveform to go through the gate but discriminates against positive signals. Resistor R4 reduces the loading on the driving circuit when transistor Q1 is turned on by the input signal, and also increases the ability of the circuit to discriminate against noise.

2.2 *Circuit Operation:* In the stable state Q1 is off, Q2 is in saturation, and C1 is charged via CR1 and the emitter-base diode of Q2 to a potential of 6 volts. Application of a negative-going input voltage drives the base of Q1 negative with respect to ground and thus causes a current to flow in the base-emitter circuit of Q1 which will charge the base.[2,3] The time taken to charge the base is quite small. At the end of this period, collector current begins to flow, and the potential at Q1 collector rises toward ground.

As the potential at the collector of Q1 rises, it is impressed on the base of Q2 via C1. When Q1 saturates, it clamps one side of C1 to ground. Since C1 has had no time to discharge, the other side impresses a positive voltage with respect to ground on the base of Q2. This voltage acts to drive the minority carriers out of the base of Q2 and to turn it off. Although the +6 volts impressed on the base causes Q2 to come out of saturation rapidly, the voltage at the collector of Q2 falls at a rate primarily determined by the effective capacitance of the collector load. The negative voltage at the collector of Q2 is applied to the base of Q1 and keeps Q1 on until Q2 is turned back on by the discharge of C1.

Q2 is kept off by the potential applied to its base, but this potential falls from +6 volts toward −6 volts as C1 discharges through R3. When the voltage at the base of Q2 goes slightly negative with respect to ground, the base-emitter circuit of Q2 begins to conduct and collector current starts to flow. The voltage at the collector of Q2 rises toward ground and is applied to the base of Q1, turning it off.

With Q1 off and Q2 on, one side of C1 is

[1] See also Preferred Circuits 210 through 216.

[2] R. Beaufoy and J. J. Sparkes, "The Junction Transistor as a Charge-Controlled Device," *ATE Journal*, Vol. 13, No. 4, Oct. 1957, pp 310–327. (Automatic Telephone and Electric Co., Strowger Works, Liverpool 7, England.)

[3] R. S. Ledley, *Digital Computer and Control Engineering*, McGraw-Hill, New York, 1960, pp. 658–667.

connected to ground via the base-emitter diode of Q2, and the other side is connected to the −18 volt supply through CR1 and R1. CR2 is back biased until the negative potential at the collector of Q1 reaches −6 volts. The recovery time of the circuit is a function of the time required to charge C1 through R1. Since C1 also controls the time delay, the recovery time is related to the delay time and is about 25% of the total delay time if R3 is a fixed resistor of the value shown. The recovery time must be added to the total delay time to determine the maximum operating rate of the circuit. At the conclusion of the recovery time, Q1 is off, Q2 is on, and the circuit has returned to its initial stable state.

The sequence of these events is shown by the waveforms in figure 213–1. The time delay generated by PC 213 begins when the leading edge of the input pulse reaches 10% of its peak amplitude, and ends when the trailing edge of the output waveform has completed 10% of its change. The waveform at the base of Q2 is the basic timing waveform determined by the values of R3 and C1. The beginning of this waveform, as well as the leading edge of the output voltage waveform, is delayed from the leading edge of the input pulse by the delay time[4] of Q1. The delay time of Q2,[5] which ends after the trailing edge of the output waveform has completed 10% of its change, also contributes to the total time delay. The time required to complete both the trailing edge of the output waveform (Q2 collector) and the trailing edge of Q1 collector waveform is a function of the loads attached to each of these collectors. Although Q1 has turned off before the completion of the output waveform, its collector voltage falls at a rate determined by the time required to recharge C1 through R1 and the emitter-base diode of Q2. This determines the recovery time of the circuit but does not affect the time delay.

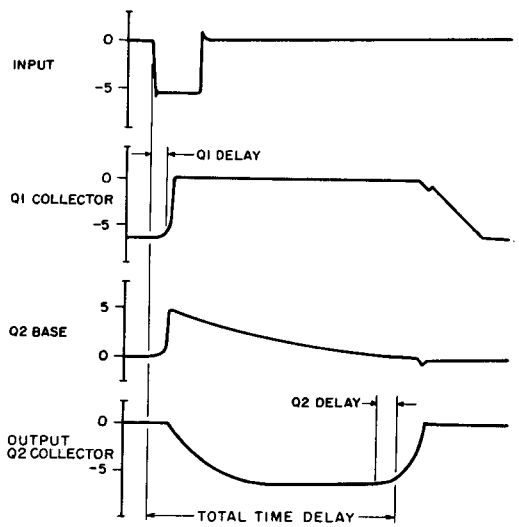


Figure 213–1.—Operation of time delay multivibrator.

[4] For a definition of delay time, see note 6, p. 213–4. For a glossary of digital computer terms, see Notes to the Preferred Circuits Manual, section 17.5.

[5] See note 8, p. 213–4.

2.3 *Input Impedances and Loads:* The maximum load that can be driven by any of the digital circuits is determined by the effect of the load on the rise time of the output signal. To simplify the loading rules, the input impedance and maximum load for each circuit of the set of digital logic circuits, PC 210 through 216, are arbitrarily given in terms of "F" and "G" loads. The "F" (flip-flop) load is derived from the input impedance of the bistable multivibrator, PC 212; the "G" (gate) load is equivalent to the input impedance of the general purpose NOR gate, PC 210.

The equivalent circuit of each of these loads is shown in figure 213–2. The actual load impedance may vary somewhat from the equivalent circuit describing it. Allowances were made for this, however, in formulating the output loading rules. The two forms of the "F" load represent the two methods of coupling

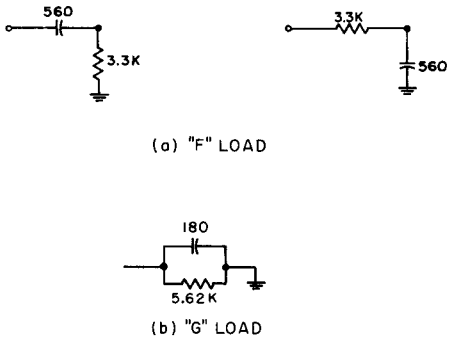


Figure 213–2.—Equivalent circuits of loads and input impedances.

into the flip-flop. Because the transistor loads the junction of the resistor and capacitor in the actual input circuit of the flip-flop, the "F" load is a less accurate approximation than the "G" load.

2.4 *Power Supplies:* The −18 volt supply should be obtained by connecting the positive side of a 12-volt floating source to the −6 volt supply. In this way the clamping diode current can be maintained when the transistor is biased off without causing reverse current flow in the −6 volt supply. If the −18 volts is supplied from a separate source and the transistor is off, the clamping diode current will be maintained by a current from the −18 volt supply flowing in the reverse direction through the −6 volt supply, because the two supplies will be connected in series opposition.

Supply voltages should not deviate more than 10% from the nominal values of 6 volts, −6 volts, and −18 volts. The noise level on the −6 volt supply must not exceed 1.7 volts in peak magnitude to prevent spurious triggering of loads such as bistable multivibrator PC 212.

When PC 213 is used in a system, additional filtering of power leads is required to keep external and system induced noise to tolerable levels. This problem is discussed at length in Notes to the Preferred Circuits Manual, section 17.

3. PERFORMANCE

3.1 *Factors Affecting Time Delay Accuracy:* Three principal sources of error in the total delay time are as follows:

(1) The delay times of the two transistors Q1 and Q2. The effect of delay time is discussed in section 2.2 where it is shown that the time interval between the beginning of the input pulse and the end of the output waveform includes the delay time of the transistors as well as the basic time interval determined by R3, C1.

(2) Variation in the input characteristics of Q2. The principal characteristics of Q2 which affect the delay are the storage time and I_{CBO} characteristic. During the storage time of Q2, which begins at the same time that C1 begins to discharge, a portion of the charge from C1 flows into the base of Q2 to neutralize the minority carriers stored there during saturation. This charge subtracts from the initial charge of C1 and shortens the total delay. The back resistance of the emitter-base diode of Q2 is in parallel with R3 so that I_{CBO} current flow further shortens the time delay. These are the principal sources of error for time delays less than 10 μsec. They cause a variation in the total time delay of from ±10% at 2 μsec to ±6 % at 10 μsec. In the range from 10 to 100 μsec (where the effect of delay time is negligible) the variation is less than 6%.

(3) Variations in the values of R3 and C1. The actual time delay varies directly with variations in R3 and C1. The variations due to the initial tolerance of the components plus the changes caused by temperature and time add an additional ±10% variation to the total time delay, under the worst conditions. If R3 is made adjustable, and C1 is selected to have a temperature coefficient opposite that of R3, this additional deviation can be held to ±2%, or less.

3.2 *Input Signal Requirements:* As indicated by the waveforms in figure 213-1, the initiation of the timing cycle is non-regenerative. The input signal, therefore, must supply sufficient charge to turn Q1 on. The combinations of input-signal width and amplitude required for reliable triggering when all components affecting triggering sensitivity are at their worst-case limits are shown in figure 213-3. The 0.5 μsec minimum pulse width specified on page 213-2 is based on a minimum

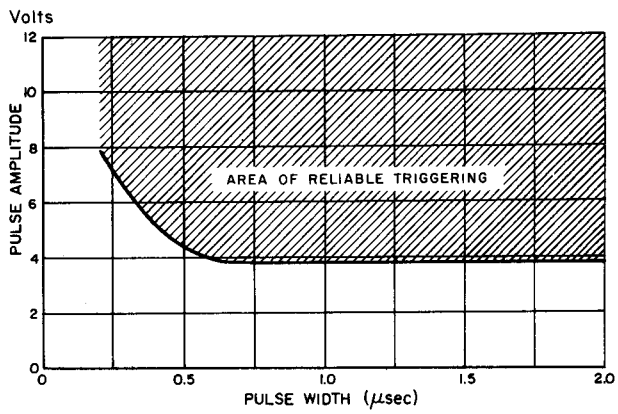


Figure 213-3.—Trigger requirements.

amplitude of 5.4 volts (6 volts—10%) and on the consideration that the effective amplitude may be reduced by noise on the —6 volt supply

3.3 *Typical Waveforms:* Typical waveforms are shown in figure 213–4 (a) through (f) and are discussed in the corresponding paragraph below. All of the waveforms were made at a sweep speed of 1 μsec per centimeter.

(a) Input pulse. A negative 1 μsec pulse of approximately 6 volts amplitude is applied as a trigger. The pulse width must be greater than the turn-on time of Q1 to assure proper triggering.

(b) Voltage at anode of gate diode, CR3.

(c) Voltage at the base of Q1. Prior to the application of the trigger, the base of Q1 is maintained slightly positive by the bias supply. The base is driven negative by the trigger, causing Q1 to turn on. When Q1 turns on, it causes Q2 to turn off, and the potential from the collector of Q2, applied via the voltage divider R6, R2 keeps Q1 on. At the completion of the cycle, the charge stored in C3 provides a current source necessary for fast replacement of the minority carriers stored in the base of Q1. When Q1 turns off, the discharge of C3 causes the base to be momentarily driven positive.

(d) Voltage at the collector of Q1. Initially, Q1 is biased off, and the collector is clamped at —6 volts by diode CR2. When a negative pulse is applied to the base of Q1, its collector voltage rises with a time constant which is a function of the individual transistor. The delay between the initiation of the input pulse and the rise of Q1 collector voltage adds to the total time delay. At the end of the cycle, when the voltage at the base of Q1 becomes positive, Q1 begins to turn off. The turn-off time is a function of the storage characteristics of Q1, but does not affect the total time delay. The voltage at the output terminal X is the same as that at the collector of Q1 except for less than 0.1 volt difference in amplitude caused by the voltage drop in diode CR1.

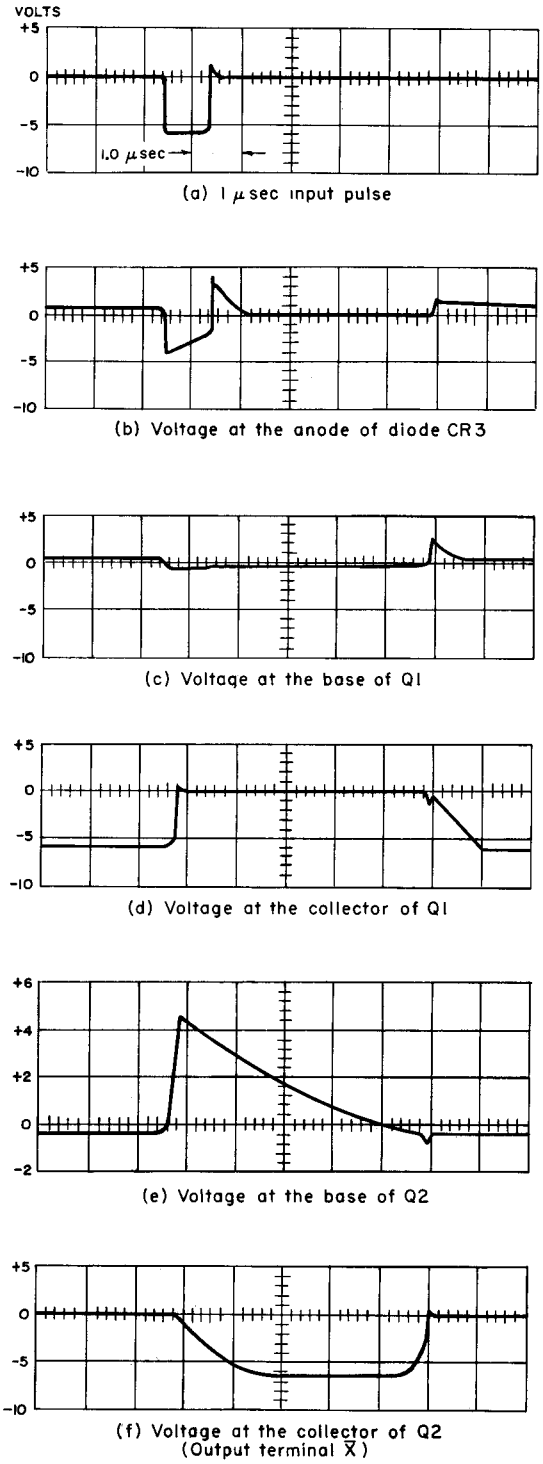


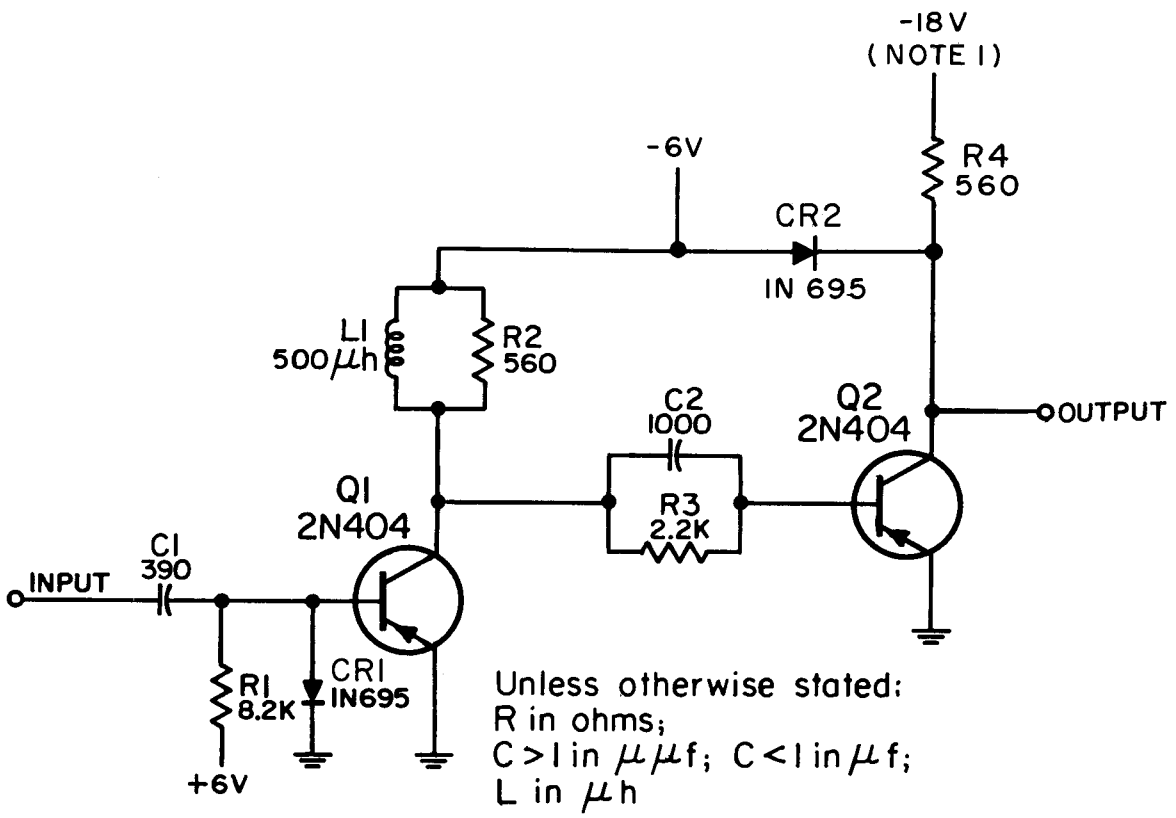
Figure 213–4.—Typical waveforms.

(e) Voltage at the base of Q2. Initially Q2 is on, and the base voltage is clamped at approximately −0.4 volt by its base-emitter diode. When Q1 collector voltage rises, the voltage at the base of Q2 follows because of the capacitor C1 connecting the two points. The charge drawn by the base of Q2 during turn-off partly accounts for the attenuation of the peak magnitude of the waveform at the base of Q2 with respect to the change in Q1 collector voltage. Following the completion of Q1 turn-on, the voltage at the base of Q2 is derived from the charged capacitor C1 which now has its negative plate clamped to ground by the saturated transistor Q1. The base potential of Q2 decreases as C1 discharges from approximately +6 volts toward −6 volts through R3. When the potential reaches zero volts, Q2 enters the conductive region. From this point on there is a definite bend in the waveform caused by the decreasing input impedance of the base of Q2.

(f) Voltage at the collector of Q2. Initially Q2 is in saturation, and its collector is about 0.1 volt negative with respect to ground. The load capacitance connected to the collector (two "G" loads in this case) slows the rise of the leading edge of the waveform but does not affect the total time delay. The delay characteristics of Q2 do affect the total time delay, since it is this delay which determines how quickly Q2 will enter the conductive region once its base goes negative.

NBS PREFERRED CIRCUIT NO. 214
PULSE SHAPER

NBS PREFERRED CIRCUIT NO. 214
PULSE SHAPER



Components:

Maximum power dissipation: R1: <10 mw; R2: 80 mw; R3: 45 mw; R4: 700 mw.
Limits (these are not tolerances; see note 2): R1, R4: ±5%; R2, R3: ±20%. All C: ±10%.
L1: ±10%.

Operating characteristics:

Temperature range: −30°C to +60°C.
Input impedance: Two "G" loads. (See section 2.3.)
Input pulse characteristics:
Polarity: Negative.
Minimum amplitude: 6 volts ±10% referenced to ground.
Width at 50% amplitude: 0.8 μsec minimum.
Rise time (Note 3): ≤1.0 μsec.

Operating characteristics—*Continued*

Output pulse width: 0.8 to 1.4 μsec; nominal 1.0 μsec.

Switching characteristics:

Signal	Maximum no. of loads	Maximum switching time (note 4)
Pulse	4 "F" or "G"	Turn-off time (note 5): 0.7 μsec. Storage time: 0.5 μsec. Rise time: 0.2 μsec.
Level	8 "F" or "G"	Turn-off time: 0.9 μsec. Storage time: 0.5 μsec. Rise time: 0.4 μsec.

Maximum dc load: 15 ma at −6.2 volts ±10%.

Power requirements:

−18 volts ±10% at 45 ma.
−6 volts ±10% at 48 ma.
+6 volts ±10% at 1 ma.

NOTES:

1. The −18 volt supply is obtained by connecting a −12 volt source in series with the −6 volt supply. (See section 2.4.)

2. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified. Thus the term "limits" includes the initial tolerance plus the drifts caused by environmental changes or aging.

3. Rise time is used in the usual pulse sense to mean the time required for the leading edge of the waveform to change from 10% to 90% of its maximum amplitude.

4. Maximum switching times were obtained by operating the circuit with the worst combination of limit transistors, components, supply voltages, and temperature.

5. The turn-off time is the time required for the collector voltage to complete the first 90% of its total amplitude change when the transistor is turned off. It is measured from the instant that the signal applied to the transistor to turn it off completes 10% of its amplitude change, and includes the storage time (time required for the first 10% change in collector voltage) and the rise time (the time required for the voltage change from 10% to 90%).

PC 214 PULSE SHAPER

1. APPLICATION

PC 214 is a pulse forming and shaping circuit designed for use in computer, control, and communication equipment operating within the temperature range of −30 to +60° C.[1] It is generally used in conjunction with the monostable multivibrator, PC 213, to form a 1-μsec pulse at the conclusion of the delay period. It is also used to reshape a pulse which has suffered deterioration by passage through a long chain of gates, or it may be used to produce a 1-μsec pulse whose leading edge coincides with the trailing edge of a positive pulse, thus delaying the output by the width of the input pulse.

2. DESIGN CONSIDERATIONS

PC 214 consists of two grounded emitter amplifiers. The first stage, which employs an RL collector load, performs the primary shaping function and controls the pulse width. The output stage, an overdriven amplifier, serves as a buffer-power amplifier, and in addition squares off the trailing edge of the output. The output pulse width is primarily determined by the values of L1 and C1 but is also affected by the transistor characteristics, as well as the characteristics of diode CR1, the resistance of R1, and bias voltage changes. Within the temperature and component limits for which the circuit is designed, the pulse width may vary from a minimum of 0.8 μsec to a maximum of 1.4 μsec.

2.1 *Circuit Operation:* In the quiescent state, transistor Q1 is biased off by the positive voltage at the junction of the voltage divider, R1, CR1. The voltage at the collector of Q1 is approximately that of the −6 volt supply, since the drop through L1 caused by the I_{CBO} of Q1 and the base current of Q2 is negligible. Transistor Q2 is biased on by the potential applied from the −6 volt supply via the 2.2KΩ resistor, R3. C2 is charged to a potential of 6 volts.

When a negative signal is applied to the input terminal of PC 214, it biases CR1 off, turns Q1 on, and causes charging current to flow into capacitor C1 via the emitter-base diode of Q1. A small current will also flow into C1 from the positive 6-volt supply through R1. The base of Q1 is heavily overdriven by the component of C1 charging current that flows through its emitter-base diode, and the transistor is forced deeply into saturation.

The voltage at the collector of Q1 rises sharply to ground potential as the transistor is driven into saturation. Since the collector of the saturated transistor is maintained near ground potential, the −6 volt supply potential is impressed across the load which consists of L1 and R2 in parallel. If a constant voltage is to be maintained across an inductor, however, the source must be capable of supplying a constantly increasing current, since the voltage across the inductor is proportional to the rate of change of current through it. To maintain an essentially constant voltage across L1, therefore, the collector current of the transistor must increase at a constant rate. This is possible in spite of the decreasing base current, because although the base current is decreasing, it is more than sufficient to keep the transistor in saturation. Under these conditions the collector current is limited by the impedance of the load, and not by the transistor itself.

After approximately one microsecond the collector current has increased so much that the base drive is no longer sufficient to keep the transistor in saturation. If the collector current were to remain constant from this point on, the voltage across the load would drop to zero at a rate determined by the time constant L1/R2. Actually, the collector current decreases somewhat during this time, so that the trailing edge of the pulse at Q1 collector falls more rapidly than would be predicted from the time constant of the load circuit alone. When, as a result of the decreasing voltage across the load, the voltage at Q1 collector reaches approximately −6 volts, Q2 turns on. The voltage at the collector of Q1 continues to change, however, because of the discharge of the energy stored in L1.

The waveform at the collector of Q1 is not satisfactory as an output, primarily because of the negative overshoot at the trailing edge. The addition of the second stage, using Q2 as

[1] See also Preferred Circuits 210 through 216.

an overdriven amplifier, eliminates the overshoot, provides a low impedance output, and isolates the timing elements from the load. The base of Q2 is connected to the collector of Q1 by resistor R3 and capacitor C2, which is initially charged to a potential of 6 volts with its positive side grounded through the emitter-base diode of Q2. When Q1 is turned on by the leading edge of the input signal, the base of Q2 is driven positive causing Q2 to turn off rapidly. The time constant of the interstage network, R3, C2, is long enough to maintain the bias on the base and keep Q2 off until Q1 collector voltage again drops to approximately −6 volts. At this time the base of Q2 is driven negative, turning Q2 on and providing an additional discharge path for the remaining energy stored in L1. The overdrive caused by the discharge of L1 through the emitter-base diode of Q2 decreases Q2 delay time and improves the trailing edge of the output pulse.

2.2 *Output Pulse Width:* The output pulse width of PC 214 may be reduced if the input signal does not meet the minimum requirements. In addition, the output pulse width may vary from 0.8 to 1.4 μsec with changes in some of the circuit parameters. In general, a decrease in Q1 collector current flow, or a decrease in the charging rate of the capacitor C1, will widen the pulse, and an increase will have the opposite effect. Several of the factors which affect the pulse width and their effect are listed in table 214–1.

TABLE 214–1.—*Factors Affecting Pulse Width*

Physical change	Effect	Reason
Increase C1	Widen pulse	Takes longer to charge C1.
Increase R1	Widen pulse	Reduces portion of C1 charging current which comes from +6 volt supply.
Decrease +6 volt potential.	Widen pulse	Reduces portion of C1 charging current which comes from bias supply.
Increase Q1 Beta	Widen pulse	Reduces base current needed to sustain given collector current flow.
Increase L1	Widen pulse	Decreases rate of increase of collector current during ON time.
Increase the storage characteristics of Q1.	Widen pulse	Widens the output pulse because it has little effect on the leading edge, but delays the trailing edge. Q1 is initially biased off. Its turn on is rapid and not significantly affected by the transistor storage characteristics. Its turn off, which initiates the trailing edge of the output pulse, is slower, however, and depends on the storage time of the transistor.
Increase the storage characteristics of Q2.	Narrow pulse	Narrows the output pulse because it delays the leading edge but has little effect on the trailing edge. The turn off of Q2, which forms the leading edge of the output pulse, is a function of the storage characteristics of the transistor. The effect of the storage characteristics on the turn on of Q2 is minimized by the large signal applied to the base to turn the transistor on.

2.3 *Input Impedances and Loads:* The maximum load that can be driven by any of the digital circuits is determined by the effect of the load on the rise time of the output signal. The input impedance and maximum load for each circuit of the set of digital logic circuits, PC 210 through PC 216, are arbitrarily given in terms of "F" and "G" loads to simplify the loading rules. The "F" (flip-flop) load is derived from the input impedance of the multivibrator, PC 212; the "G" (gate) load is equivalent to the input impedance of the general purpose NOR gate, PC 210.

The equivalent circuit of each of these loads is shown in figure 214–1. The actual load impedance may vary somewhat from the equivalent circuit describing it; however, allowances were made for this in formulating the

output loading rules. The two forms of the "F" load represent the two methods of coupling into the flip-flop. Because the transistor loads the junction of the resistor and capacitor in the actual input circuit of the flip-flop, the "F" load is a less accurate approximation than the "G" load.

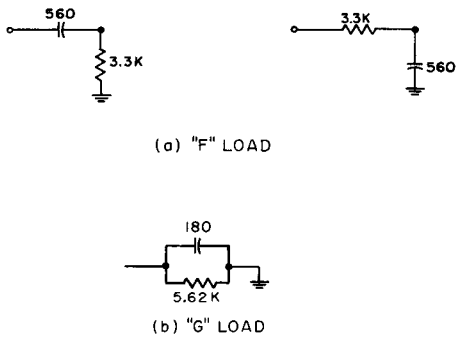


Figure 214-1.—Equivalent circuits of loads and input impedances.

2.4 *Power Supplies.* The −18 volt supply should be obtained by connecting the positive side of a 12-volt floating source to the −6 volt supply. In this way the clamping diode current can be maintained when the transistor is biased off without causing reverse current flow in the −6 volt supply. If the −18 volts is supplied from a separate source and the transistor is off, the clamping diode current will be maintained by a current from the −18 volt supply flowing in the reverse direction through the −6 volt supply, because the two supplies will be connected in series opposition.

Supply voltages should not deviate more than 10% from the nominal values of 6 volts, −6 volts, and −18 volts. The noise level on the −6 volt supply must not exceed 1.7 volts in peak magnitude to prevent spurious triggering of loads such as bistable multivibrator PC 212.

When PC 214 is used in a system, additional filtering of power leads is required to keep external and system induced noise to tolerable levels. This problem is discussed at length in Notes to the Preferred Circuits Manual, section 17.

3. PERFORMANCE

Voltage waveforms at points of interest throughout PC 214 are illustrated in figure 214-2, a through e, and discussed in the corresponding paragraph below. All of the traces were recorded at a sweep speed of 0.5 μsec per centimeter. The input signal was furnished by a general purpose NOR gate, PC 210, used as an inverter; 4 "G" loads formed the load on the output of PC 214.

(a) Input signal: A 4 μsec pulse is used for the input signal to allow the display of the complete pulse forming and shaping cycle of PC 214. The break in the leading edge of

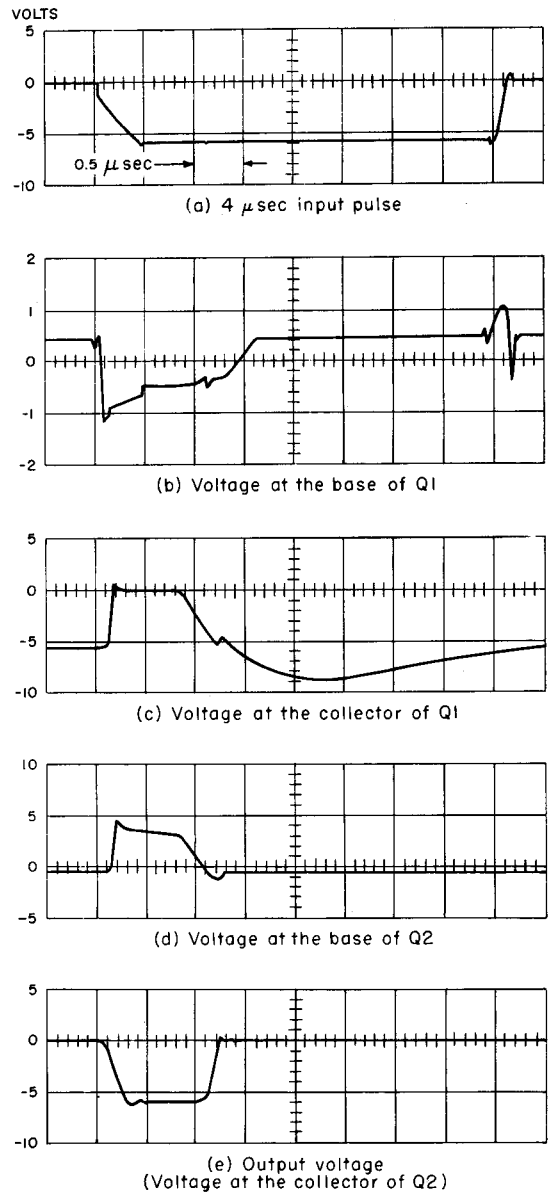


Figure 214-2.—Typical waveforms.

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the waveform occurs when the emitter-base diode of Q1 starts to conduct, lowering the input impedance of PC 214, and loading the signal source.

(b) Base voltage of Q1: Prior to the application of the input signal, the base is clamped at a slight positive voltage by the biasing circuit. With the application of the trigger pulse, the base voltage falls rapidly at about the same rate as the input signal until the base-emitter diode starts to conduct. From this point on the charging of capacitor C1 gradually reduces the base voltage. When the base current is no longer sufficient to maintain the collector current, Q1 turns off, and the biasing circuit restores the base voltage to its original condition.

(c) Voltage at the collector of Q1: The heavy drive at the base of Q1 rapidly forces Q1 into saturation and produces a fast rising leading edge on the collector voltage waveform. As long as Q1 remains in saturation and the base drive is sufficient to maintain an increasing current through inductor L1, the collector voltage remains at approximately ground potential. When the transistor comes out of saturation, the collector voltage falls at a rate determined by the decreasing collector current and by the load, L1, R2. When the voltage at Q1 collector reaches about −6 volts, Q2 turns on and its base-emitter diode in series with the parallel combination of C2 and R3 furnishes an additional discharge path for the energy stored in the inductor. The discharge of this energy causes the negative voltage swing after Q1 turns off.

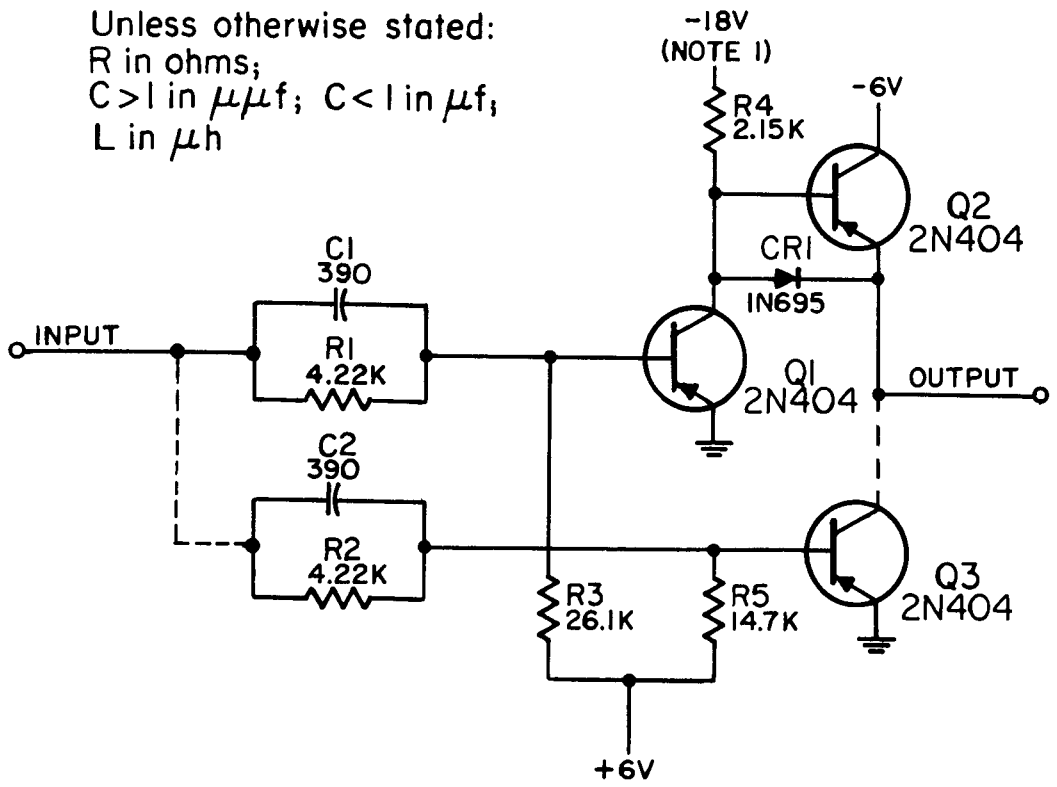
(d) Voltage at the base of Q2: Initially Q2 is on and its base is approximately at ground potential. Q2 base voltage tends to follow the rise in Q1 collector voltage when Q1 turns on, because the base of Q2 is connected to the collector of Q1 by resistor R3 and capacitor C2, which discharges little during the 1 μsec pulse. The extent of the discharge of C2 can be judged by the reduction in Q2 base voltage during the time that Q1 collector is grounded. During the trailing edge of the pulse at Q1 collector, the base voltage of Q2 drops to a slight negative value and the overshoot on the Q1 collector waveform is clipped by the base-emitter diode of Q2.

(e) Output voltage (voltage at the collector of Q2): The overshoot which appeared at the collector of Q1 is eliminated, and the speed of the trailing edge of the output waveform is improved by the action of Q2. The output pulse width is 1 μsec.

NBS PREFERRED CIRCUIT NO. 215
PULSE POWER AMPLIFIER

NBS PREFERRED CIRCUIT NO. 215

PULSE POWER AMPLIFIER



Components:

Maximum power dissipation: R1,R2,R3,R5: <10 mw; R4: 180 mw.

Limits (these are not tolerances; see note 2): All R: $\pm 5\%$. All C: $\pm 10\%$.

Operating characteristics:

Temperature range: $-30°C$ to $+60°C$.

Input impedance (see section 2.3):

For 2 transistor amplifier: 2 "G" loads.

For 3 transistor amplifier: 4 "G" loads.

Input signal characteristics:

Level (Note 3):

Logical "1": -6.2 volts $\pm 10\%$ at 3.1 ma.

Logical "0": -0.15 volts.

Pulse (Note 4):

Polarity: Positive or negative.

Amplitude: 6 volts $\pm 10\%$.

Width at 50% amplitude: 0.8 μsec minimum; 5 μsec maximum.

Rise time (Note 5): ≤ 0.2 μsec.

(Specifications continued on next page)

Operating characteristics—*Continued*

Switching characteristics for two- or three-transistor circuit (Note 6):

Input signal	Output signal
Level change from 0 v to −6 v with rise time of 0.4 μsec.	Level change from −6 v to 0 v. Turn-on time (Note 7): 0.4 μsec max. Delay time: 0.2 μsec max. Rise time: 0.2 μsec max.
Level change from −6 v to 0 v with rise time of 0.4 μsec.	Level change from 0 v to −6 v. Turn-off time (Note 8): 0.7 μsec max. Storage time: 0.2 μsec max. Rise time: 0.5 μsec max.
Negative-going pulse with rise time of 0.2 μsec.	Positive-going pulse Turn-on time: 0.35 μsec max. Delay time: 0.15 μsec max. Rise time: 0.2 μsec max.
Positive-going pulse with rise time of 0.2 μsec.	Negative-going pulse Turn-off time: 0.35 μsec max. Storage time: 0.15 μsec max. Rise time: 0.2 μsec max.

Maximum load: (See section 2.3.)

Circuit	Type of output			
	Direct current	Level	Positive pulse	Negative pulse
2-transistor amplifier	44 ma at −6.2 v ±10% 1 ma at −0.15 v	12 loads "F" or "G"	12 loads "F" or "G"	12 loads "F" or "G"
3-transistor amplifier	44 ma at −6.2 v ±10% 1 ma at −0.15 v	40 loads "F" or "G"	40 loads "F" or "G"	12 loads "F" or "G"

Power requirements:

Voltage	Maximum current	
	2-transistor circuit	3-transistor circuit
−18 volts ±10%	10 ma	10 ma
−6 volts ±10% (note 9)	50 ma	50 ma
+6 volts ±10%	0.9 ma	0.9 ma

(For notes, see next page)

NOTES:

1. The −18 volt supply is obtained by connecting a −12 volt source in series with the −6 volt supply. (See section 2.4.)

2. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.

3. The minimum duration of a level is 5 μsec.

4. Positive pulses are referenced to −6.2 volts ±10%; negative pulses are referenced to ground (actually about −0.15 volt).

5. Rise time is used in the usual pulse sense to mean the time required for the leading edge of the waveform to change from 10% to 90% of its maximum amplitude.

6. Maximum switching times were obtained by operating the circuit with the worst combination of limit transistors, components, supply voltages, and temperature. The load in each case was maximum for that type of operation.

7. The turn-on time is the time required for the collector voltage to complete the first 90% of its total change when the transistor is turned on. It is measured from the instant that the signal applied to the transistor to turn it on completes 10% of its amplitude change and includes the delay time (the time required for the first 10% change in collector voltage) and the rise time (the time required for the voltage change from 10% to 90%).

8. The turn-off time is the time required for the collector voltage to complete the first 90% of its total change when the transistor is turned off. It is measured from the instant that the signal applied to the transistor to turn it off completes 10% of its amplitude change and includes the storage time (time required for the first 10% change in collector voltage) and the rise time (the time required for the voltage change from 10% to 90%).

9. The current specified is maximum for the circuit; actual current requirements vary with the load. The −6 volt supply must furnish any external dc load plus 1.2 ma for each RC load used.

PC 215 PULSE POWER AMPLIFIER

1. APPLICATION

PC 215 is a pulse power amplifier designed for use as an auxiliary driving element when the load to be driven by PC 210, 211, 212, 213, or 214 exceeds the specified maximum for that circuit. PC 215 has an input impedance equal to 2 "G" loads, but is capable of driving 12 "F" or "G" loads. The addition of two resistors, R2 and R3, a capacitor, C2, and a transistor, Q3, increases the input impedance of PC 215 to 4 "G" loads, but allows the circuit to drive 40 "F" or "G" loads with a positive-going output signal.

2. DESIGN CONSIDERATIONS

The maximum number of loads that can be driven by any of the digital circuits is determined by the effect of the load on the rise time of the output signal. The rise time of the output signal is in turn determined by the rapidity with which the load capacitance can be charged or discharged, depending on the polarity of the desired output signal. PC 215 is basically a two-transistor circuit consisting of a grounded-emitter amplifier driving an emitter follower. A second grounded-emitter amplifier stage can be added in parallel with the first to improve the performance of the circuit for positive-going output signals.

2.1 *Circuit Configuration:* The grounded-emitter amplifier, Q1, serves as a low-impedance discharge path for the capacitive portion of the load when the output signal is positive going, and emitter follower, Q2, is a low-impedance discharge path for this same capacitance when the output signal is negative going. Resistor R3, together with the positive 6-volt supply, provides the base of Q1 with a positive bias current which prevents I_{CBO} multiplication when Q1 is off. When Q1 is on, the low impedance path it provides between the base and emitter of Q2 keeps the multiplied Q2 collector current in the vicinity of I_{CES} in magnitude.

When Q1 is off, the rise in its collector voltage is limited to approximately −6 volts by the clamping action of the internal base-collector diode of Q2. Q2 thus replaces the diodes used for clamping in the other circuits of the digital set, standardizing output amplitude and allowing faster rise times for negative-going signals than could be achieved without such clamping.

In the 3-transistor circuit, Q3 furnishes an additional discharge path for the load capacitance when the signal is positive going. It carries more of the discharge current than does Q1 because Q1 has the added impedance of diode CR1 in series with it, while Q3 does not; Q3 therefore tends to become hotter than Q1 and requires more positive bias current to prevent I_{CBO} multiplication.

2.2 *Circuit Operation:* PC 215 operates as an inverting power amplifier for either pulses or levels. When a negative 6-volt potential is applied to the input, Q1 is turned on in saturation, and the positive-going potential at its collector turns Q2 off. During the first few tenths of a volt change in Q1 collector voltage, diode CR1 remains back biased, keeping the collector of Q1 disconnected from the load and allowing fast turn-off of Q2. For the remainder of the discharge of the load capacitance the diode is in series with Q1, and the voltage across the load drops to ground potential at a rate determined by the impedance of Q1 and CR1 in series and the capacitive component of the load.

When the input terminal is brought to ground potential, Q1 is turned off, and the output voltage falls toward −6 volts at a rate determined by the impedance of the saturated transistor Q2 and the capacitive component of the load. Diode CR1 disconnects the collector of Q1 from the load, thus allowing the collector of Q1 to rise rapidly and cause a fast turn-on of Q2.

The third transistor stage, Q3 and its associated components, when added to PC 215 operates in parallel with Q1. Since Q3 does not have a diode in series with it, it reduces the impedance of the discharge path by more than half and therefore increases the circuit capabilities by a greater percentage than it decreases the input impedance. For negative-going outputs the performance is unaffected;

when the output is positive going, however, the rise time is decreased because of the decrease in output impedance under these conditions.

2.3 *Input Impedances and Loads:* The maximum load that can be driven by any of the digital circuits is determined by the effect of the load on the rise time of the output signal. To simplify the loading rules, the input impedance and maximum load for each circuit of the set of digital logic circuits, PC 210 through PC 216, are arbitrarily given in terms of "F" and "G" loads. The "F" (flip-flop) load is derived from the input impedance of the bistable multivibrator, PC 212. The "G" (gate) load is equivalent to the input impedance of the general purpose NOR gate, PC 210.

The equivalent circuit of each of these loads is shown in figure 215–1. The actual load impedance may vary somewhat from the equivalent circuit describing it. Allowances were made for this, however, in formulating the output loading rules. The two forms of the "F" load represent the two methods of coupling into the flip-flop. Because the transistor loads the junction of the resistor and capacitor in the actual input circuit of the flip-flop, the "F" load is a less accurate approximation than the "G" load.

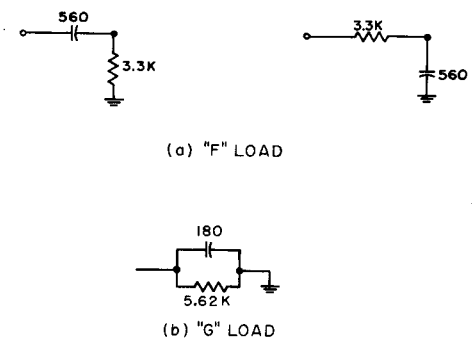


Figure 215–1.—Equivalent circuits of loads and input impedances.

2.4 *Power Supplies:* The −18 volt supply should be obtained by connecting the positive side of a 12-volt floating source to the −6 volt supply. In this way Q1 collector voltage can be clamped when the transistor is biased off without causing reverse current flow in the −6 volt supply. If the −18 volts is supplied from a separate source and the transistor is off, the clamping current will be maintained by a current from the −18 volt supply flowing in the reverse direction through the −6 volt supply, because the two supplies will be connected in series opposition.

Supply voltages should not deviate more than 10% from the nominal values of 6 volts, −6 volts, and −18 volts. The noise level on the −6 volt supply must not exceed 1.7 volts in peak magnitude to prevent spurious triggering of loads such as bistable multivibrator PC 212.

When PC 215 is used in a system, additional filtering of power leads is required to keep external and system induced noise to tolerable levels. This problem is discussed at length in Notes to the Preferred Circuits Manual, section 17.

3. PERFORMANCE

Typical operating characteristics of PC 215 when used as a three-transistor circuit are shown in figures 215–2 and 215–3. The effect of changing from a three- to a two-transistor circuit is illustrated in figures 215–4 and 215–5. This change was accomplished by disconnecting R2 and C2 from the input terminal, thereby effectively removing Q3 from the circuit. In all of the figures the waveforms were obtained at a sweep speed of 0.2 μsec per centimeter.

Figure 215–2 illustrates the effect of loading on the output of PC 215 operating with a negative input. Trace (a) shows the input signal, which remains relatively unaffected by the changes in output loading. The change in slope of the leading edge (trace (a)) occurs when transistors Q1 and Q3 go into saturation and sharply increase the load on the input source. Trace (b) shows the output voltage under light-loading conditions. As shown in trace (c), an increase to medium-loading conditions results in a reduced slope of both leading and trailing edges of the output signal. Trace (d) shows that under maximum loading conditions the leading edge rise time remains within the 0.2 μsec specification.

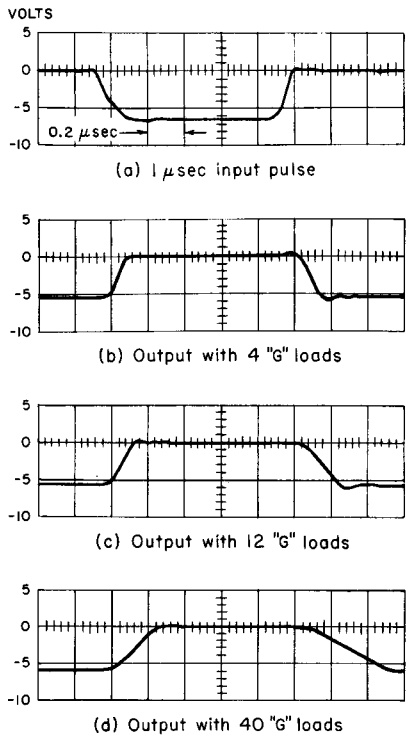


Figure 215-2.—Typical waveforms for three-transistor circuit with negative input.

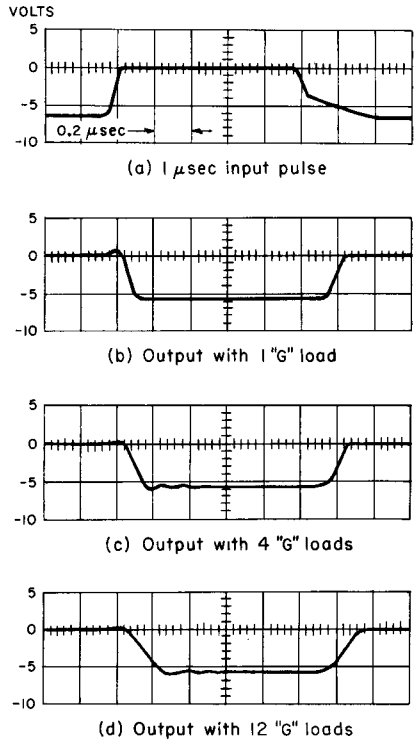
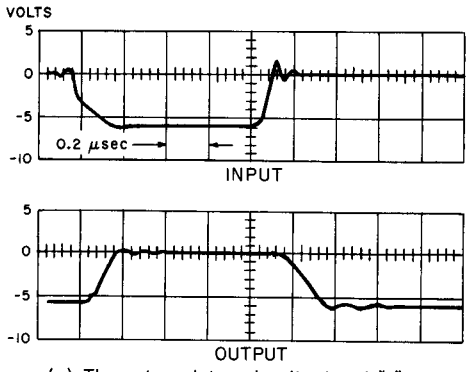


Figure 215-3.—Typical waveforms for three-transistor circuit with positive input.

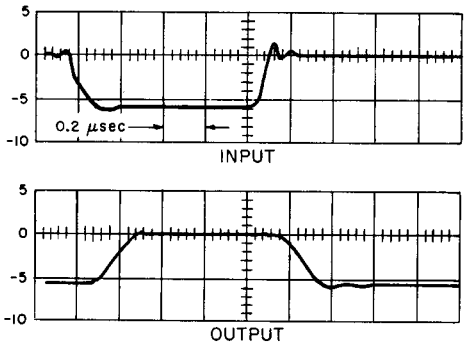
Figure 215-3 illustrates the effect of loading on the output of PC 215 when the input signal is a positive pulse. Here, the input signal was furnished by PC 210 used as an inverter. The effect of the 4 "G" input impedance of PC 215 on the gate is evident from the sharp break in the trailing edge slope in trace (a). Traces (b), (c), and (d) once again show the output waveform for light, medium, and maximum loading. Trace (d) shows that 12 "G" loads can be driven without the leading edge rise time of the output waveform exceeding the 0.2 μsec limit.

In figure 215-4 are shown the input and output waveforms for both the two- and three-transistor versions of PC 215. The 12 "G" load is the maximum that can be driven by the two-transistor version. The advantage of the two-transistor version is seen in the faster input rise time permitted by the decreased loading on the driving source. However, the slope of the leading edge of the output waveform is significantly reduced when the third transistor is rendered inactive, because the leading edge of the output waveform is formed by the discharge of the load capacitance through transistors Q1 and Q3 which have been turned on by the negative input pulse. Transistor Q3 is the more effective discharge path because it is not in series with a diode as is Q1, and Q3 is the transistor that has been removed in the two-transistor version.

Figure 215-5 is a repetition of the measurements illustrated in figure 215-4, but the input pulse is now positive rather than negative. Note that the slope of the leading edge of the output signal is unaffected by the presence or absence of Q3 in the circuit. This is to be expected, since during the leading edge of a negative-going output signal, the load capacity is being charged by Q2, while Q1 and Q3 are both cut off. Since Q2 is not affected by the removal of Q3, the leading edge rise time of negative-going output signals is not affected by the presence or absence of Q3.

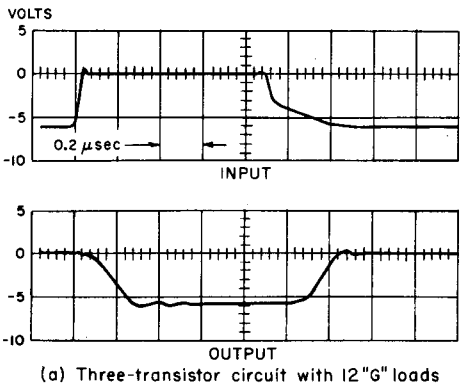


(a) Three-transistor circuit with 12 "G" loads

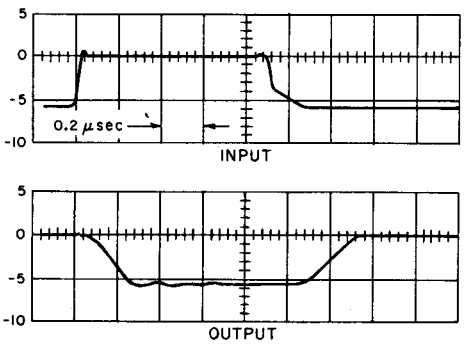


(a) Two-transistor circuit with 12 "G" loads

Figure 215–4.—Comparison of the performance of the two- and three-transistor circuits for negative input signal.



(a) Three-transistor circuit with 12 "G" loads



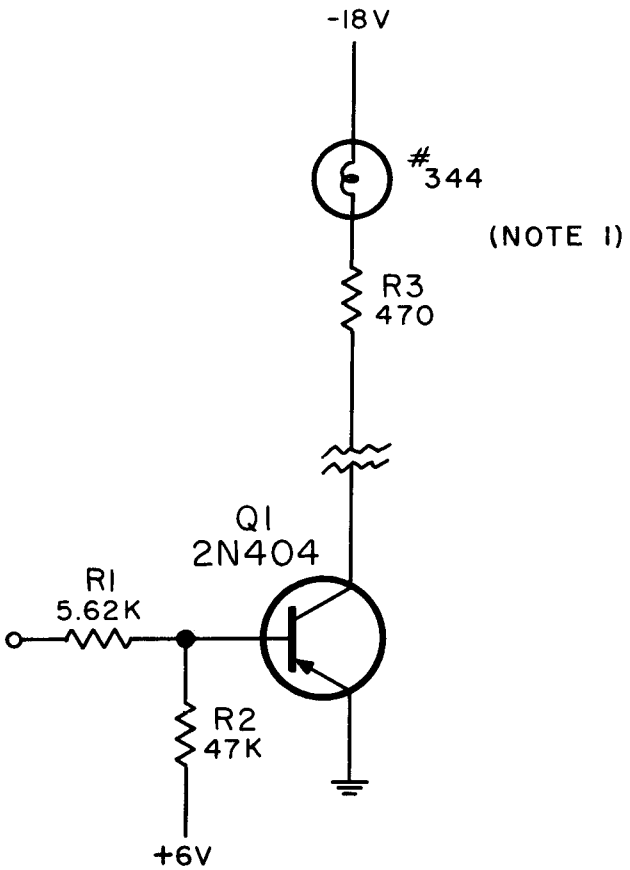
(b) Two-transistor circuit with 12 "G" loads

Figure 215–5.—Comparison of the performance of the two- and three-transistor circuits for positive input signals.

NBS PREFERRED CIRCUIT NO. 216
INDICATOR

NBS PREFERRED CIRCUIT NO. 216

INDICATOR



Unless otherwise stated: R in ohms

Components:

Maximum power dissipation: R1: 8 mw; R2: 5 mw; R3: 180 mw.

Limits (these are not tolerances; see note 2): R1, R2: ±5%; R3: ±20%.

Operating characteristics:

Temperature range: −54° C to 71° C.

Input impedance: ½ "F" load. (Note 3)

Input signal:

	Indicator action
Logical "0" (ground potential)	No light
Logical "1" (−6.2 volts±10% at 1.2 ma)	Lamp lights

Power requirements:

−18 volts ±10% at 15 ma.

+6 volts ±10% at 0.16 ma.

NOTES:

1. The indicator and the amplifier may be in different locations.
2. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.
3. The "F" load is the input impedance of the flip-flop circuit, PC 212.

PC 216 INDICATOR

1. APPLICATION

PC 216 is used as an indicator in the compatible set of digital logic circuits.[1] The circuit is designed for a nominal drive of 15 ma at 10 volts to insure conservative operation of the type 344 bulb under limit conditions. It can be used to drive electromechanical devices which operate within the same power limits, or to drive devices with 6 volt ratings, in which case a −6 volt source is used for the collector supply.

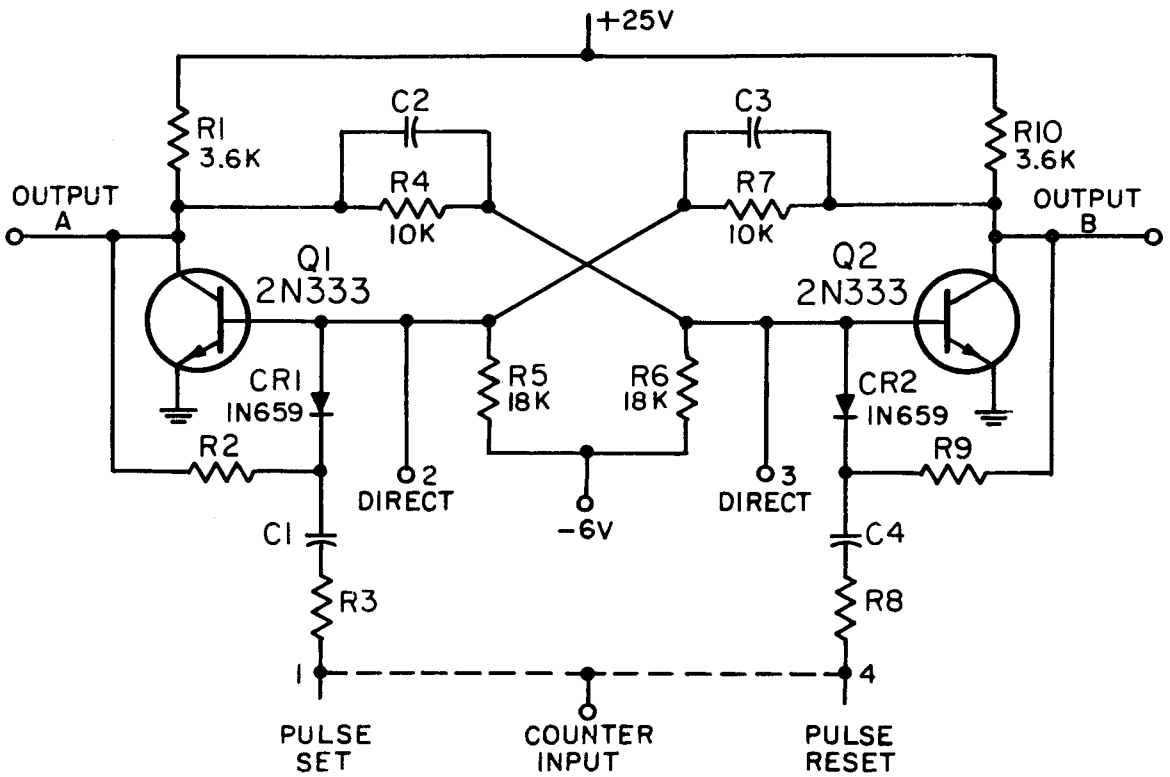
[1] See also Preferred Circuits 210 through 215.

2. DESIGN CONSIDERATIONS

PC 216 is a common-emitter amplifier designed to drive a type 344 light bulb which has a rating of 18 ma at 12 volts. A positive current bias derived from the +6 volt supply via resistor R2 prevents I_{CBO} current amplification at temperatures up to 71° C. Resistor R1 is chosen to insure saturation with low beta transistors at temperatures of 0° C and above. At lower temperatures Q1 may not saturate, but the added dissipation in Q1 is no problem at low temperatures. Further heating in this instance will increase beta and therefore lead to saturation and decreased dissipation.

NBS PREFERRED CIRCUIT NO. 250
SATURATING BISTABLE MULTIVIBRATOR

NBS PREFERRED CIRCUIT NO. 250
SATURATING BISTABLE MULTIVIBRATOR



Unless otherwise stated: R in ohms; C in $\mu\mu$f

Components:

R1, R4, R5, R6, R7, R10: ±5% limits; R2, R3, R8, R9: ±10% limits. All C: ±10% limits. (See Note 1.) For component values not specified on the schematic diagram of PC 250, see table 250–1, page 250–4.

Operating characteristics:

Input levels and minimum durations:

Counter or pulse: 7 volts negative, 3 μsec duration at −7 volt level. Direct: +1 ma for 10 μsec, or −4 ma for 5 μsec.

Maximum pulse repetition frequency: 40 kc.

Delay time: 2 to 5 μsec.

Output levels, both A and B: 18 ±3 volts for 10% supply voltage variation.

Output impedance:

Positive-going waveform: 2.5KΩ.

Negative-going waveform: Less than 500 Ω.

Power requirements: +25 volts, 10 ma; −6 volts, 0.7 ma.

Temperature range: −65° C to 125° C with temperature stable resistors and capacitors.

NOTE:

1. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.

PC 250 SATURATING BISTABLE MULTIVIBRATOR

1. APPLICATION

PC 250 is a slow-speed, stable, saturating multivibrator for use as a counter, shift register, gate, or switch. It provides transitional stages between electromechanical readout and higher speed nonsaturating bistable counters. The design was optimized to accept wide tolerance transistors and should be employed when selection is to be avoided.

2. DESIGN CONSIDERATIONS

The circuit is triggered by turning off the on transistor and allowing the resulting transient to regenerate, holding the circuit in the new state. In the rest condition the dc voltages applied to the diode terminals are such that the diode associated with the off transistor is biased off by approximately 20 volts. The diode associated with the on transistor is biased off by less than the collector saturation voltage of the on transistor, approximately one-half volt. A negative pulse with the specified amplitude will, when applied to the counter input, be steered to the base of the on transistor and cause a change of state. A positive pulse will not be passed by the steering diodes.

The input circuit must furnish to the base circuit of the on transistor a negative pulse of sufficient voltage and time duration to drive the transistor out of saturation. The required voltage and width of the applied pulse are related. Experimental measurements show that at a given impedance level the product of the two is very nearly constant for the minimum trigger level.

Three sets of part values for input connections 1 and 4 are listed in table 250–1. When PC 250 is driven from a low-impedance pulse source, the component values and performance specifications of Adaption 1 apply. When PC 250 is driven from a higher impedance source, such as a non-saturating bistable multivibrator or a time delay multivibrator, the component values and performance specifications of Adaption 2 apply. When successive stages of PC 250 are cascaded, the first stage is either Adaption 1 or Adaption 2, and the successive stages should have the component values specified for Adaption 3. Instead of buffer amplifiers being used to prevent reaction on prior stages, various values are used for the resistors and capacitors listed without sacrifice of ultraconservative performance.

2.1 *Circuit Operation:* The bias circuit permits one transistor to conduct in saturation while the other transistor is held in the off condition. The dc circuit elements have been chosen so that transistors with low limit values of dc current gain, h_{FE}, will saturate. Higher gain transistors will consequently be driven further into saturation.

In the design of this circuit care was taken to use the extreme lower limit value of h_{FE}. This value has been found to be approximately 7 for the 2N333.

The output voltage swing is expressed as

$$\Delta V_2 \approx V_{CC} \frac{\mathrm{R7}}{\mathrm{R7}+\mathrm{R10}} - V_{CE(sat)2}$$

where V_{CC}=collector supply voltage and $V_{CE(sat)2}$=collector to emitter saturation voltage. From this relationship it is readily determined that the output amplitude depends on the transistor saturation resistance. This is one of the most important advantages of saturating type switching circuits.

2.2 *Impedance:* Some changes in the circuit impedance can be made. Only the relative values of the circuit resistances are of importance, except that for a fixed supply voltage the value of R5 and R6 is limited by the I_{CBO} and the $V_{CE(sat)}$ characteristics of the transistor, rather than by the other circuit elements. It is recommended that R5 and R6 not exceed 20,000 ohms; larger values of the other resistances may be chosen.

The resistor values should not be scaled down beyond that point where either the collector current ratings or the power dissipation of the transistors are exceeded. The resistors in

TABLE 250–1.—*Component values and performance of PC 250*

Adaption No.	Signal source	Max. source imped.	R2 R9	R3 R8	C2 C3	C1 C4	Input imped.	Input: Max. rep. rate	Input: Trigger voltage range	Output: Rise time (tr)	Output: Fall time (tf)	Number of set-reset loads	Minimum circuit recovery time
		ohms	ohms	ohms	μμf	μμf	ohms	kc	volts	μsec	μsec		μsec
1	Operation from low impedance pulse source	[1] 500	2.2K	[1] 500	1200	1500	1K	[2] 40	3–5	15	2.5	0	[3] 20
								[2] 40	3–5	25	3.0	2	[3] 25
								25	7–25	40	5.0	5	40
								12.5	7–25	80	7.5	10	80
2	Operation from non-saturating multivibrator or from either output of time delay multivibrator	[2] 1K	5.6K	[2] 1K	680	1000	1.5K	20	7–25	15	1.5	0	50
								20		25	2.0	2	50
								20		40	3.0	5	50
								12.5		80	5.0	10	80
3	Cascaded operation of identical stages or from either of above adaptions	500	5.6K	2.2K	680	560	3K	40	14–25	15	1.0	0	25
								40		25	1.5	2	25
								25		40	3.0	5	40
								12.5		80	7.0	10	80

[1] Total of source and isolating resistance is 500 ohms, ±10%.
[2] Total of source and isolating resistance is 1000 ohms, ±10%.
[3] With input pulse width of 3–5 μsec duration.

PC 250 may be reduced to approximately one-half of the values given without exceeding the ratings of the 2N333 up to a case temperature of 125° C. However, input circuit Adaption 2 is not recommended for use with resistance values lower than those given. Note that the saturation resistance of the transistor is not affected by this scaling down, so that the output impedance for a negative-going signal does not change.

2.3 *Transistor Type*: The transistor characteristics of greatest importance to the circuit operation are: (1) collector voltage, power, and current ratings; (2) dc and high-frequency current gain; (3) base-to-emitter voltage required to sustain saturated conduction; (4) collector-to-emitter voltage during saturated conduction; and (5) maximum I_{CBO} to be encountered.

The transistor power dissipation is dependent on the saturation collector voltage, as well as on the saturation collector current. The power loss in the transistor is particularly low if transistors having a low value of saturation resistance are used.

3. PERFORMANCE

3.1 *Pulse Input:* The input circuit may be used for either set-reset or counter operation.

The characteristics required of the input signal are dependent on the values of R2, R9, R3, R8, C1, and C4. Values of these components have been chosen to provide operation from three general types of input, as outlined below and in table 250–1.

(a) Adaption 1 will operate from pulse inputs occurring at frequencies up to 40 kc. The highest frequency response is obtained when the pulse width of the negative-going input signal is 3 to 5 μsec. Pulse widths less than 3 μsec do not provide reliable operation, while pulses wider than 5 μsec do not allow the input circuit sufficient recovery time at 40 kc.

Generally, the duration of the more positive portion of the input signal should be a minimum of 16 μsec. For this circuit, the specified value of R3, as well as that of R8, is the sum of the source resistance and the physical isolating resistance.

(b) Signal sources for driving Adaption 2 can be a non-saturating flip-flop or either output of a time delay multivibrator. In this operation, only two set-reset (or one counter connection) inputs per source are recommended. A typical recovery time of the input circuit is approximately 50 μsec.

(c) Adaption 3 is intended for cascaded operation. Signal sources for driving Adaption

3 can be either Adaption 1, 2, or 3. The recovery time of the input circuit is approximately 20 μsec.

The minimum input required for reliable triggering of the three adaptions is plotted in figure 250–1 as a voltage of a given amplitude and rise time. The curves for the three adaptions show that for rise times below a certain value, dependent on the circuit, each circuit requires a minimum amplitude for triggering.

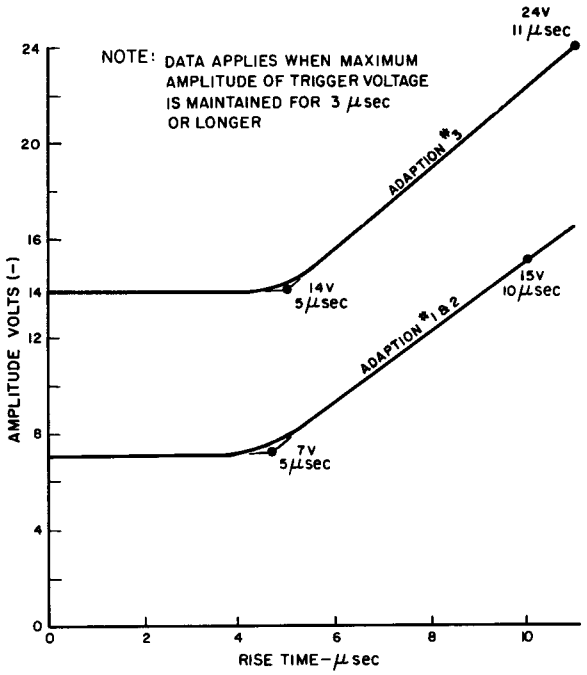


Figure 250–1.—Amplitude required for triggering vs. rise time.

The minimum duration of the applied trigger pulse, or the rest time after a negative-going ramp is applied, should not be less than 3 μsec, although shorter pulses of greater amplitude will cause triggering.

3.2 *Direct Input:* The direct input can be used for reset of the transistor by applying to the base a negative voltage source that will cause a current of 4 ma to ground for 5 μsec. Alternatively, a positive pulse from a source that will cause a current of 1 ma for 10 μsec may be used. The positive voltage resets the opposite transitor to the "off" condition.

The direct connection can also be used for the insertion of blocking pulses from a subsequent counter stage to provide other than binary counting operation, as illustrated in figure 250–2.

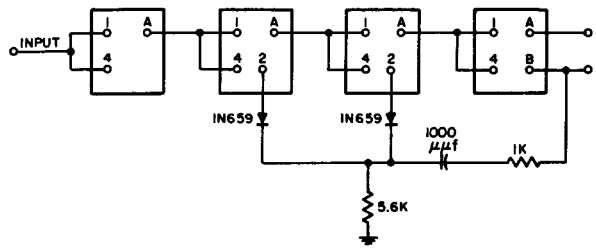


Figure 250–2.—Four stages of PC 250 connected for operation as a decade counter.

3.3 *Output:* The two outputs are complementary voltages of either 1 or 19 volts. The maximum circuit switching time is 2 to 5 μsec.

Figure 250–3 shows the output waveform. The irregularity on the more positive portion of the waveform is caused by the recovery of the input circuit from a positive-going input. Usually the spike is absorbed in the rise time of Adaption 1. In Adaptions 2 and 3 the height of the spike does not exceed 2 volts.

The rise and fall times of the outputs, which are dependent on the loading, are tabulated in table 250–1 for various combinations.

3.4 *Cascaded Operation:* Stages may be directly cascaded by connecting the inputs to the output of a previous stage. The number of inputs that can be connected depends on the input circuit used and the repetition rate desired.

The fundamental limit on the degree of loading permissible is the deterioration of the output fall time under load to the point that triggering voltages consistent with figure 250–1 are not obtained. The limit imposed by this consideration is 10 set-reset loads, or 5 counter stages, per either or both outputs. The speed-up capacitor C2 or C3 connected to the collector of the loaded side of the flip-flop should be increased by about 200 μμf for each set-reset input connected to the output.

Another consideration when the stages are cascaded is the deterioration of the output rise time under load. First, a deteriorated output rise time may not drive the opposite transistor

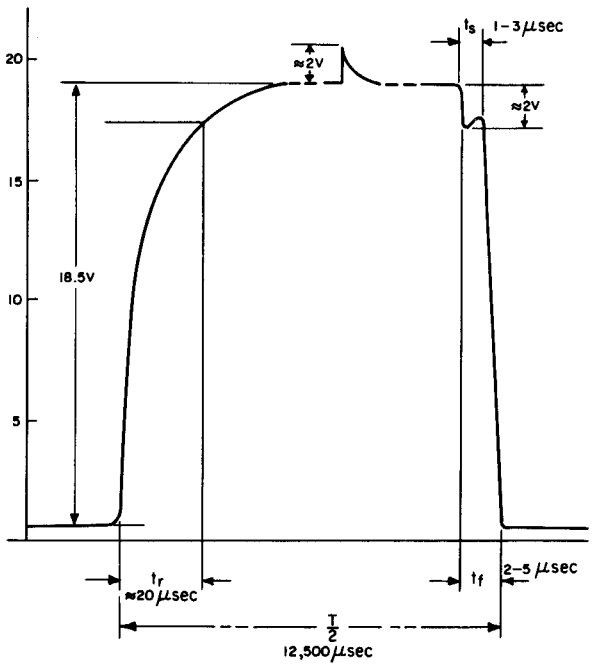


Figure 250–3.—Output waveform.

into saturation under some conditions; second, the time required for the output voltage to increase to its full "off" value exceeds the input pulse duration.

The increase in rise time restricts the upper limit on the circuit frequency response, as shown in table 250–1. The loads are always assumed to be Adaption 3.

A method of connecting four flip-flop stages for decade counter operation is shown in figure

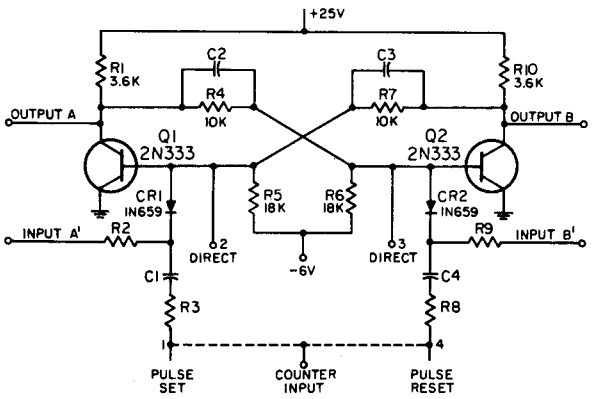


Figure 250–4.—Modification of PC 250 for use in shift registers.

250–2. This circuit has an asymmetrical output at terminal A of the fourth stage, a positive pulse of 20% duty cycle. The outputs have the same general characteristics as the binary circuit.

The saturating bistable multivibrator may be modified as shown in figure 250–4 to allow its use in a shift register. One method of interconnection is shown in figure 250–5.

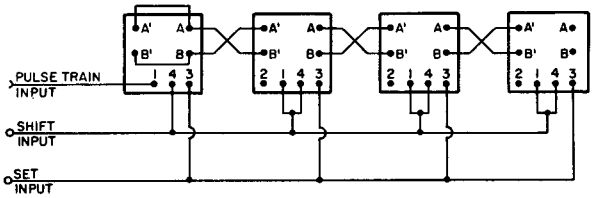
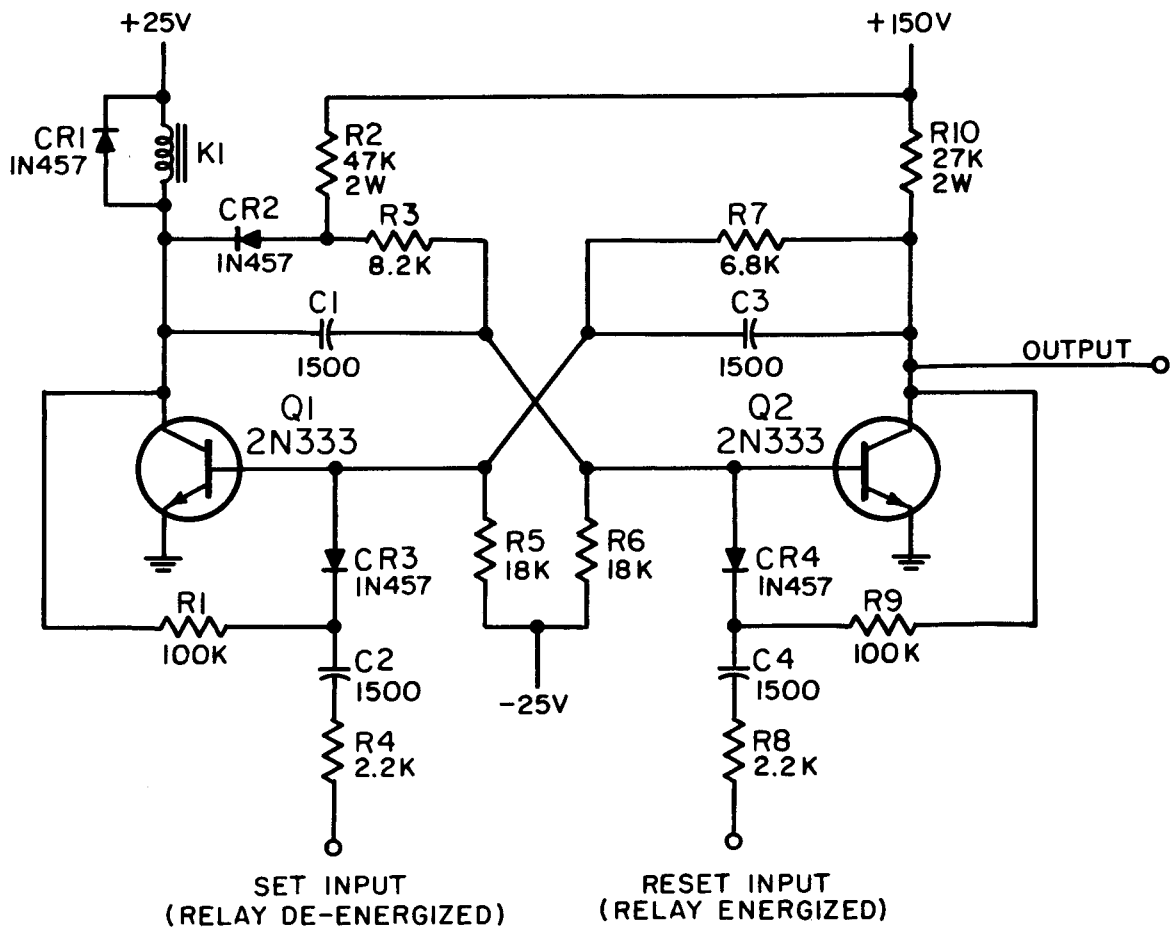


Figure 250–5.—Interconnection of modified PC 250 for shift registers.

NBS PREFERRED CIRCUIT NO. 251
RELAY CONTROL SATURATING MULTIVIBRATOR

NBS PREFERRED CIRCUIT NO. 251
RELAY CONTROL SATURATING MULTIVIBRATOR



Unless otherwise stated: R in ohms; C in $\mu\mu$f

Components: R2 and R10: $\pm 5\%$ limits; all other R: $\pm 10\%$ limits. All C: $\pm 20\%$ limits. (Note 1.)

Operating characteristics:

Input: 20 volt negative-going waveform or pulse with 10 μsec maximum rise time and minimum duration at -20 volt level of 3 μsec.

Input impedance: 2.5KΩ, or 400Ω with R4 and R8 omitted.

Outputs: Relay K1 energized by 8 ma (on); de-energized by 0.5 ma (off).
Voltage output: 30 ± 6 volts.

Relay characteristics: Winding resistance of 2.7KΩ $\pm 10\%$ and power requirement of 100 mw or less.

Power requirement: 1.5 watts total.

Temperature range: $-65°$ C to 125° C.

NOTE:

1. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.

PC 251 RELAY CONTROL SATURATING MULTIVIBRATOR

1. APPLICATION

PC 251 is intended for on-off control of electromechanical devices such as relays where the current ratio must be 10 between the on and off condition. The rate usually is limited by the control device response time. If desired, the control current can be reversed in direction between the on-off states.

2. DESIGN CONSIDERATIONS

This circuit is a modification of the saturating multivibrator PC 250. The diode CR2 and resistors R2, R3 are added to isolate the load K1 when Q1 is off. If the values of the resistors are chosen within the proper limits, the off current through the relay is the sum of the leakage currents through Q1 and CR2, or less than 0.5 ma at 125° C. This provides a relay current ratio from on to off of at least 15. For comparison, PC 250 using 2N333 transistors has an on-off ratio of less than 5 for the load currents. The modifications provide an improvement of three times in the current resolution.

2.1 *Circuit Operation:* The circuit operation is that of an ordinary transistor Eccles-Jordan, except that the current drive to hold Q2 in the on state is furnished through R2 and R3 rather than through Q1 collector load. Diode CR2 is nonconducting.

The collector power dissipation limit and the high saturation resistance of the 2N333 require that the collector current not exceed approximately 11 ma for operation to 125° C. Collector resistors of lower value than that shown will cause the collector currents to exceed this limit and will reduce the temperature range accordingly. An increase of impedances would be desirable to decrease dissipation, but the relay coil resistance would have to be increased.

2.2 *Transistor Type:* The high forward resistance of grown junction silicon transistors is incompatible with subminiature relays. The circuit power efficiency falls off sharply as the current is increased above a few milliamperes. Small relays usually require from 5 to 15 ma at a low voltage. The 2N333 was specified as a moderately priced unit in large quantity use. A diffused junction transistor such as the 2N550 has a lower resistance and higher dissipation rating but is more expensive. Lower circuit impedance could be achieved with transistors similar to the 2N550 with a resulting improvement in circuit power efficiency because of the lower permissible collector and base supply voltages.

2.3 *Relay Type:* The relay or other electromechanical device under control must have the characteristic of being energized by 8 ma coil current and being de-energized when the current drops to 0.5 ma. This specification is based on the dc load presented to the multivibrator and the power furnished to the relay winding. The inductance of the coil is unimportant, even though the rise and fall times are somewhat increased. The speed of response depends only on the relay response time.

The maximum power dissipation rating of the coil should be not less than 250 milliwatts.

3. PERFORMANCE

3.1 *Trigger Input:* The input signal required for triggering is approximately the same as that for PC 250, the simple saturating multivibrator. Since a high repetition frequency is not a major consideration, the coupling capacitors C2 and C4 have been increased.

A trigger of 14 volts with a rise time of 10 μsec is usually adequate, but with high h_{FE} transistors at the high limit temperature, a level of about 20 volts provides more dependable operation. The input circuit should be allowed at least 5 milliseconds to recover from a positive signal before the next trigger is applied.

If the source impedance is low enough, R4 and R8 may be omitted. The input impedance is then approximately 400 ohms. Capacitors

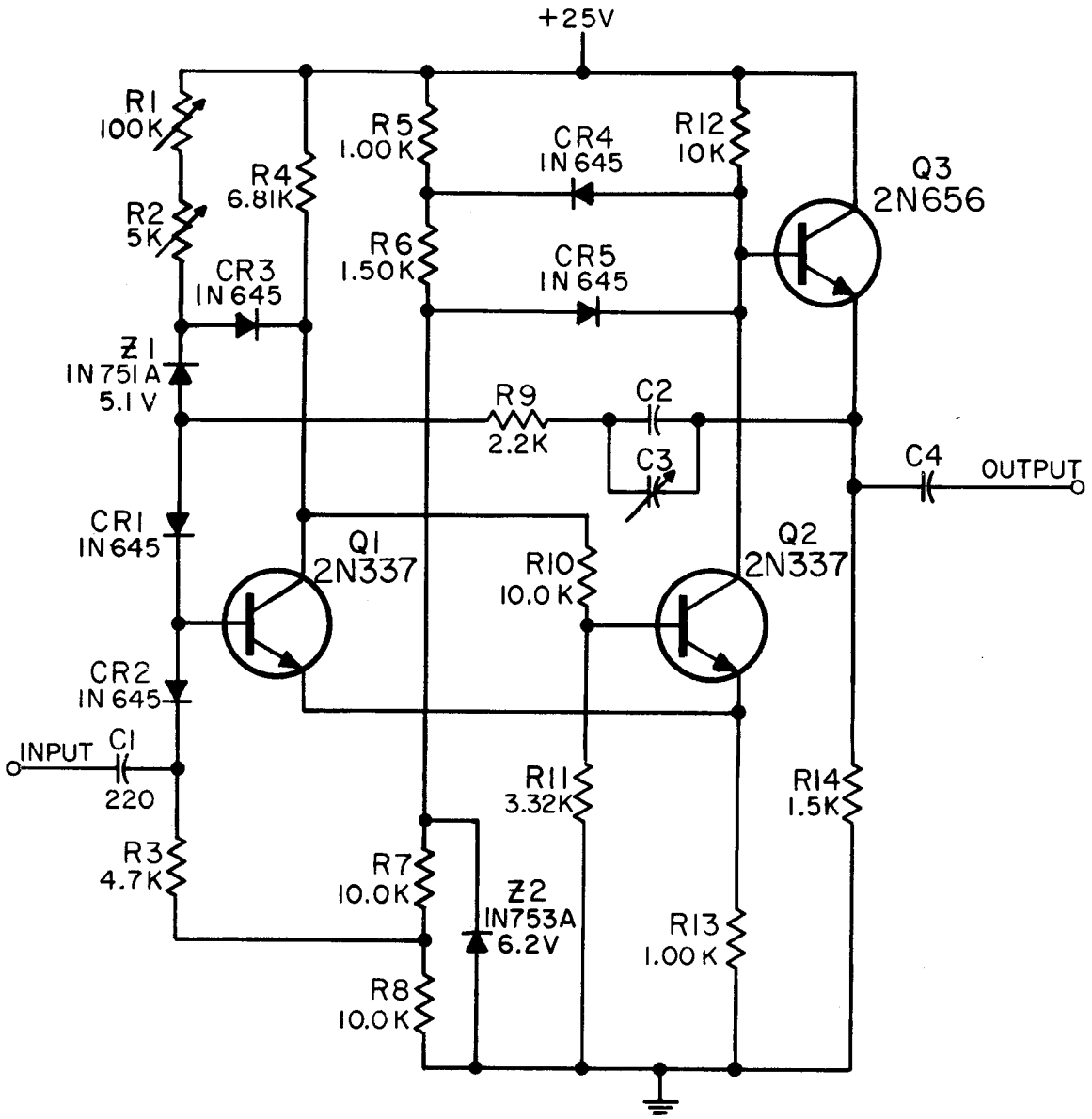
C2 and C4 should be increased to 4700 $\mu\mu$f to maintain the proper trigger pulse duration at the base of the transistor.

3.2 *Voltage Output:* A voltage output in phase with the relay closing may be taken from the collector of Q2. The level will be 30 volts, and a 10% variation in the 150-volt supply and the variability of transistors and resistors will cause a variation of about 6 volts. The source impedance at this output is 5KΩ for the positive excursion and is the saturation resistance of Q2 for the negative excursion.

NBS PREFERRED CIRCUIT NO. 252
MULTIVIBRATOR VARIABLE GATE GENERATOR

NBS PREFERRED CIRCUIT NO. 252

MULTIVIBRATOR VARIABLE GATE GENERATOR



Unless otherwise stated: R in ohms; C>1 in $\mu\mu$f; C<1 in μf; L in μh

(For specifications, see next page)

Components:

R1: Variable from 10KΩ to 100KΩ for continuously variable gate; 30KΩ to 100KΩ for fine control on step-switched gate. Linearity <0.2%. (Note 1)

C2: Select for desired gate width (see table 252-1) and for temperature compensation (see figure 252-3).

C3: See section 2.2 of text.

C4: Select for desired maximum percentage droop of output gate.

$C4 > \frac{100\ T_{max}}{R_L P}$, where T_{max}=maximum gate width, R_L=load resistance, and P=maximum percentage droop desired.

Z1: 5.1 volts ±5% at 5 ma; temperature coefficient ≈ −.015%/°C; dissipation=5 mw at 125° C.

Z2: 6.2 volts ±5% at 5 ma; temperature coefficient ≈ +.02%/°C; dissipation=50 mw at 125° C.

Approximate power dissipation: R2, R3, R7, R8, R9, R11: <0.01 watt; R13: 0.01 watt; R1, R10: 0.02 watt; R4, R12: 0.05 watt; R5: 0.06 watt; R6: 0.1 watt; R14: 0.2 watt.

Limits (these are not tolerances; see note 2 below): R1, R2, R5, R6, R7, R8, R10, R11, R13: ±1%; R4: ±2%; R12: ±5%; R3, R9, R14: ±10%. C2: See section 2.4 of text; C3: ±5%; C1, C4: ±20%.

Operating characteristics:

Temperature range: −55° C to +125° C.

Input signal:

Polarity: Negative

Amplitude: 10–20 volts.

Repetition rate: Limited by circuit recovery time. (See below.)

Wave front slope: >10 volts/μsec.

Pulse duration: 1 μsec to $0.5T_{min}$, where T_{min}=minimum gate width to be generated.

Output gate:

Polarity: Negative

Amplitude: 12.5 volts. (Note 3)

Width: 10–10,000 μsec continuously variable by R1 in 10 to 1 segments selected by C2.

Accuracy and linearity: Accurate to ±2% over the temperature range; linear to ±1%; over-all accuracy and linearity=±3%.

Rise time: 1.0 μsec (longest). (Note 4)

Fall time: 2.0 μsec (longest). (Note 4)

Maximum jitter: 0.1% of gate width.

Loading: 8KΩ (min.).
220 μμf (max.).

Recovery time: $<0.85\ T_{max}$ where T_{max}=gate width generated when R1=100K.

Delay: 0.1 to 0.3 μsec. (Start of trigger to start of output.)

Power requirements: 25 volts ±1% at 24 ma.

NOTES:

1. Gate widths may be step-switched by C2 with R1 acting as a fine control.

2. In this circuit the initial tolerance of all resistors need only be ±10%; however, drifts due to environmental changes or aging must be held to the percentage specified.

3. The maximum variation in output amplitude is ±3% plus the percentage change in supply voltage. The output amplitude may vary ±3% over the temperature range; variations in the supply voltage will cause an equal percentage variation in output amplitude.

4. Rise and fall times may be reduced 50% by using a 2N697 in place of the 2N656.

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PC 252 MULTIVIBRATOR VARIABLE GATE GENERATOR

1. APPLICATION

PC 252 generates a rectangular waveform, commonly referred to as a "gate", whose duration is relatively independent of temperature effects and directly proportional to the setting of a linear potentiometer. Such a circuit is frequently used in radar equipment to produce movable markers for display. If desired, the gate may be step-switched by capacitor C2, with the potentiometer acting as a fine control.

2. DESIGN CONSIDERATIONS

A variable rectangular waveform may be generated by either of two basic circuits, the phantastron or the monostable multivibrator. PC 252 is similar to the cathode-coupled version of the latter circuit. Because transistors are sensitive to temperature and operating point changes, certain complexities must be added to the basic circuit in order to obtain a gate continuously variable over a 10 to 1 range and stabilized against temperature changes. These additions are as follows: a breakdown diode, Z1, in combination with a rectifier diode, CR3, to prevent saturation of the normally ON transistor, Q1; a breakdown diode, Z2, in combination with two clamping diodes, CR4 and CR5, to stabilize both the output voltage and the voltage applied across the timing capacitor, C2, against temperature changes; a rectifier diode, CR1, to prevent excess reverse bias from being applied to the base-emitter junction of Q1; and an emitter-follower output to reduce loading effects on the gate width.

2.1 *Circuit Operation:* In the rest state, Q1 is held on by base current flow through R1, R2, Z1, and CR1, while Q2 is biased off by an emitter voltage which is larger than its base voltage. Diode CR4 is conducting, holding the Q2 collector to approximately 18 volts, a level determined by the divider consisting of R5, R6, and Z2.

The circuit is triggered by a negative-going wave front at the base of the ON transistor Q1, turning it off. The resulting regeneration through Q2 cuts off the base current of Q1 and completes the switching action. Diode CR1 prevents the negative voltage that occurs at the junction Z1, R9 immediately after switching (fig. 252-1) from being applied to the base of Q1 and exceeding the emitter-to-base reverse breakdown voltage of that transistor. Positive-going input wave fronts are rejected by steering diode CR2. During switching, resistor R9 prevents the emitter follower, Q3, from loading the trigger source through CR1 and C2.

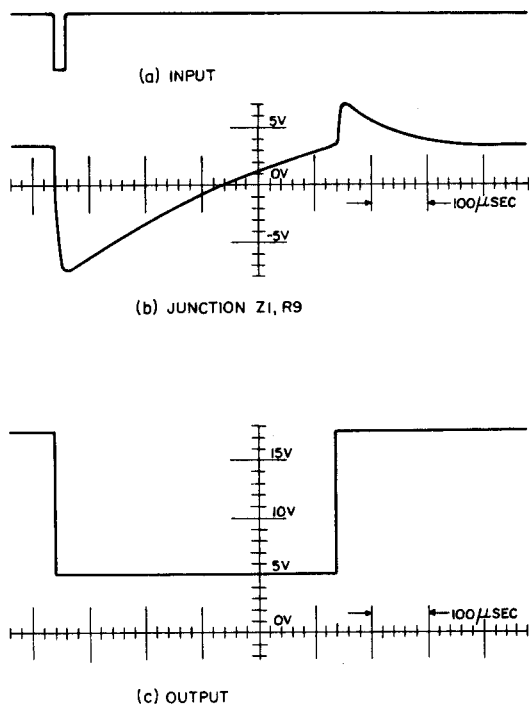

Figure 252-1.—Typical waveforms PC 252.

After switching, the circuit is in a quasi-stable state with Q1 off, Q2 on, and diode CR5 conducting, holding Q2 collector voltage to approximately the breakdown voltage of Z2. During this time, capacitor C2 discharges through R1, R2, Z1, R9, and R14, causing the voltage at the junction of Z1 and R9 to rise in an exponential curve (fig. 252-1) until CR1 begins to conduct, supplying base current to Q1, and ending the quasi-stable state. The discharge of C2, adjustable by R1, produces the timing waveform which controls the gate width. For adjustment to be linear over a 10 to 1 range, resistors R2, R9, and R14 must be small relative to the minimum value of R1.

Due to emitter-follower action, the dc output voltage follows the Q2 collector at all times. The output voltage is well stabilized against changes in temperature, since the upper and lower limits of its swing are clamped by diodes CR4 and CR5 respectively. Even more important, the change in voltage applied across C2, which affects the timing waveform and gate width, is also clamped and is therefore temperature stable.

Emitter follower Q3 improves circuit operation by decreasing the effect of output loading on gate width, and by allowing a quick recharge of C2 after the end of the gate, thus decreasing the recovery time of the circuit. For low output impedance and linear adjustment of gate width by R1, emitter resistor R14 must be small, thereby increasing the power dissipation requirements of Q3. The 2N656 or the 2N697 must be used if the circuit is required to operate over the entire high-temperature range. The 2N337 may be used if the operating temperature is limited to a range of 5°C to 40°C.

2.2 *Gate Width Range and Adjustment:* The value of capacitor C2 is chosen for the range of gate widths desired. Table 252–1 gives the approximate values required to obtain gate widths of 10–100 μsec, 100 μsec–1 msec, or 1–10 msec. Capacitor C3 should equal approximately 10% of C2 to allow precise calibration of R1 (see section 2.3) for any set of circuit component values within the specified limits. However, for a particular set of components, an approximate value for C3 may be determined experimentally and a fixed capacitor inserted. A variable capacitor only 1% the value of C2 may then be used for calibration of R1.

TABLE 252–1.—*Approximate value of C2 for desired gate width*

Gate width* μsec	R1 Ω	C2 μf
10–100	10K–100K	.0016
100–1000	10K–100K	.016
1000–10,000	10K–100K	0.16

*Gate width ≈ 0.6 R1 C2 when R1 > 30K

A potentiometer control of C2 discharge time provides the continuous adjustment of gate width. For a linear adjustment over a wide range, the timing potentiometer, R1, must be placed in the base circuit of Q1, since attempting to isolate it from the dc circuit of the transistor base would introduce shunting resistance, reducing the range of adjustment of the potentiometer and destroying its linearity. The necessary location of the timing adjustment in the dc base circuit, however, results in a wide range of base currents to the normally ON transistor. If it were not for breadkdown diode Z1, the lower values of timing resistance would result in large base currents and saturation of the transistor. Under these conditions, the charge stored in the base region would prevent the transistor from turning off quickly and would require trigger voltages much too large for correct triggering under non-saturated conditions, i. e., when higher values of timing resistance are used. The discrepancy would be magnified by changes in transistor beta with temperature.

Although saturation occurs when the collector-base *junction* is biased in the *forward* direction, the voltage drop in the bulk resistance of the 2N337 collector under these conditions is large enough to result in a *reverse* bias being measured between the collector and base *terminals*. Breakdown diode Z1 in combination with diode CR3 prevents saturation by holding the collector-to-base voltage, V_{CB}, to a value greater than the aforesaid voltage drop, in this case approximately 1 volt under worst conditions. For Q1, V_{CB} may be represented as

$$V_{CB} = -V_{CR3} - V_{Z1} + V_{CR1}$$

where the voltage drops are in the conventional current forward direction. Typically $V_{CB} = -0.5 + 4.0 + 0.5 = 4.0$ volts.

2.3 *Calibration of Gate Width Adjustment:* In most applications, potentiometer R1 will be calibrated so that gate width may be read directly from the potentiometer dial in terms of units appropriate to a particular application. The calibration is accomplished for any set of circuit component values within the specified limits by adjustment of R2 and C3.

The percentage change in gate width with variation of C3 is constant over the entire range of R1, while the percentage change with variation of R2 is largest at low values of R1. C3 is set so that the dial tracks near the high end of the range of R1; R2 is set to compensate for the reduction in the voltage change applied to the junction of Z1,R9 (see fig. 252-1) as the resistance of R1 is reduced. C3 and R2 should be adjusted to obtain the best independent linearity[1] for the particular transistors and breakdown diodes in the circuit.

The procedure is first to set R2 at the center of its range and R1 at a large value, adjusting C3 for the desired dial reading. Then set R1 near its minimum value of 10KΩ, and adjust R2 for the desired dial reading. Repeat the above procedure until interaction between the two adjustments is eliminated, remembering to adjust for minimum error over the entire range. This may necessitate checking a few intermediate settings of R1. If replacement of a transistor or breakdown diode is necessary, the calibration should be rechecked. Figure 252-2 is a typical curve showing the independent linearity of the gate width adjustment.

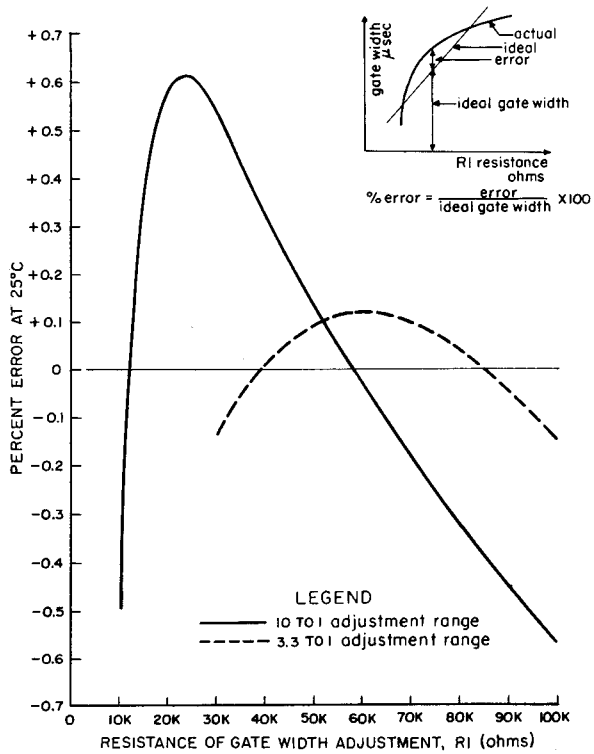

Figure 252-2.—Independent linearity of gate width adjustment.

2.4 *Temperature Compensation and Selection of C2:* An important consideration when choosing C2 is its percent change with temperature over the complete temperature range of −55° C to +125° C. PC 252 is designed so that normal changes in C2 capacitance with temperature will compensate for temperature changes in the remainder of the circuit. In a typical circuit, for exact temperature compensation of gate width, C2 should have a temperature characteristic similar to that shown in figure 252-3. Stated another way, a typical PC 252 circuit with C2 unaffected by temperature would have a percentage change in gate width vs. temperature curve exactly like the curve of figure 252-3, except that the ordinate scale would be inverted. Adding to this the percent changes of C2 with temperature would give an over-all circuit in which the gate width does not vary at all with temperature.

It should be noted that the solid curve of figure 252-3 is typical. The curve for exact compensation may vary ±2% from that shown (dotted curves). Exact temperature compensation could be obtained by matching C2 to the remainder of the circuit, but this is seldom possible.

PERFORMANCE

3.1 *Output Gate:* PC 252 generates a rectangular waveform (gate), 12.5 volts in amplitude, which may be varied linearly by a potentiometer over a 10 to 1 range. Longest rise and fall times of the gate are 1.0 μsec and 2.0 μsec, respectively. Independent linearity[2] over the temperature range is ±3% or better.

[1] Independent linearity is the deviation when the slope and position of the straight line representing desired output versus shaft rotation may be chosen to make the deviation a minimum. This is the deviation from the "best fit" straight line as opposed for instance to using the straight line determined by the zero and 100% points. See J. F. Blackburn, Components Handbook, *Rad. Lab. Series*, Vol. 17, McGraw-Hill N.Y., 1949, pp. 266, 267.

[2] Ibid.

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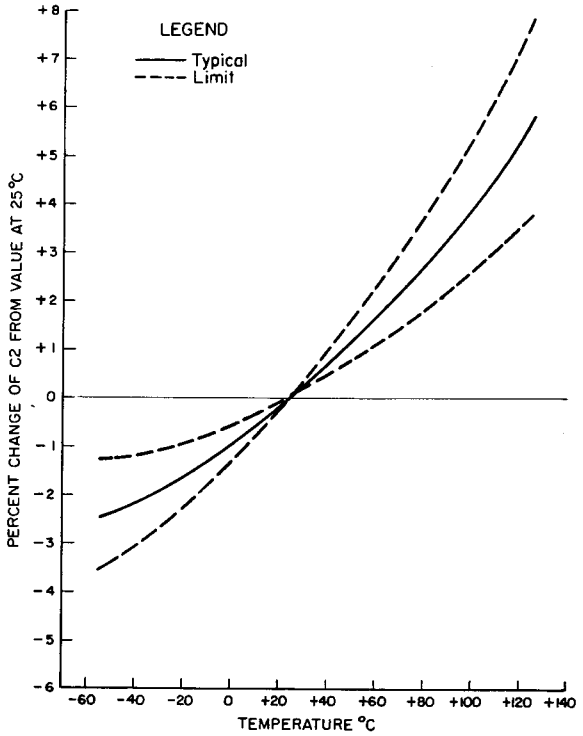


Figure 252–3.—Temperature characteristic of C2 required to compensate for temperature changes in remainder of circuit.

Independent linearity of the gate width adjustment at 25° C is better than ±1% over a 10 to 1 continuous adjustment range (fig. 252–2) and better than 0.3% over a 3.3 to 1 adjustment range, i.e., R1 variation from 30KΩ to 100KΩ. Over the −55° C to 125° C temperature range, the output gate width, whether step-switched or continuously variable, is accurate within ±2% of its value at 25° C. Reducing the maximum temperature excursion to +100° C will increase gate width accuracy to ±1.5%. Independent linearity over the temperature range is obtained by adding the ±1% linearity at 25° C to the ±2% maximum variation with temperature. Percentage changes in supply voltage are reduced by a factor of 10 in their percentage effect on gate width.

The voltage amplitude of the output gate at 25° C is approximately 12.5 volts, depending upon the exact value of Z2 breakdown voltage. Once determined for a particular circuit, the amplitude is accurate to ±3% over the temperature range. Percentage variation in supply voltage causes an equal percentage variation in the output gate amplitude.

Rise and fall times of the output gate may be reduced 50% by using a 2N697 in place of the 2N656 in the emitter follower stage, Q3. Both rise and fall times are longest at the low temperature extreme, −55° C.

Circuit recovery time varies with the value of timing capacitor C2. Expressed as a function of gate width, the recovery time is less than 0.85 T_{max}, where T_{max} is the maximum gate width which may be generated (R1=100K) with any particular value of C2.

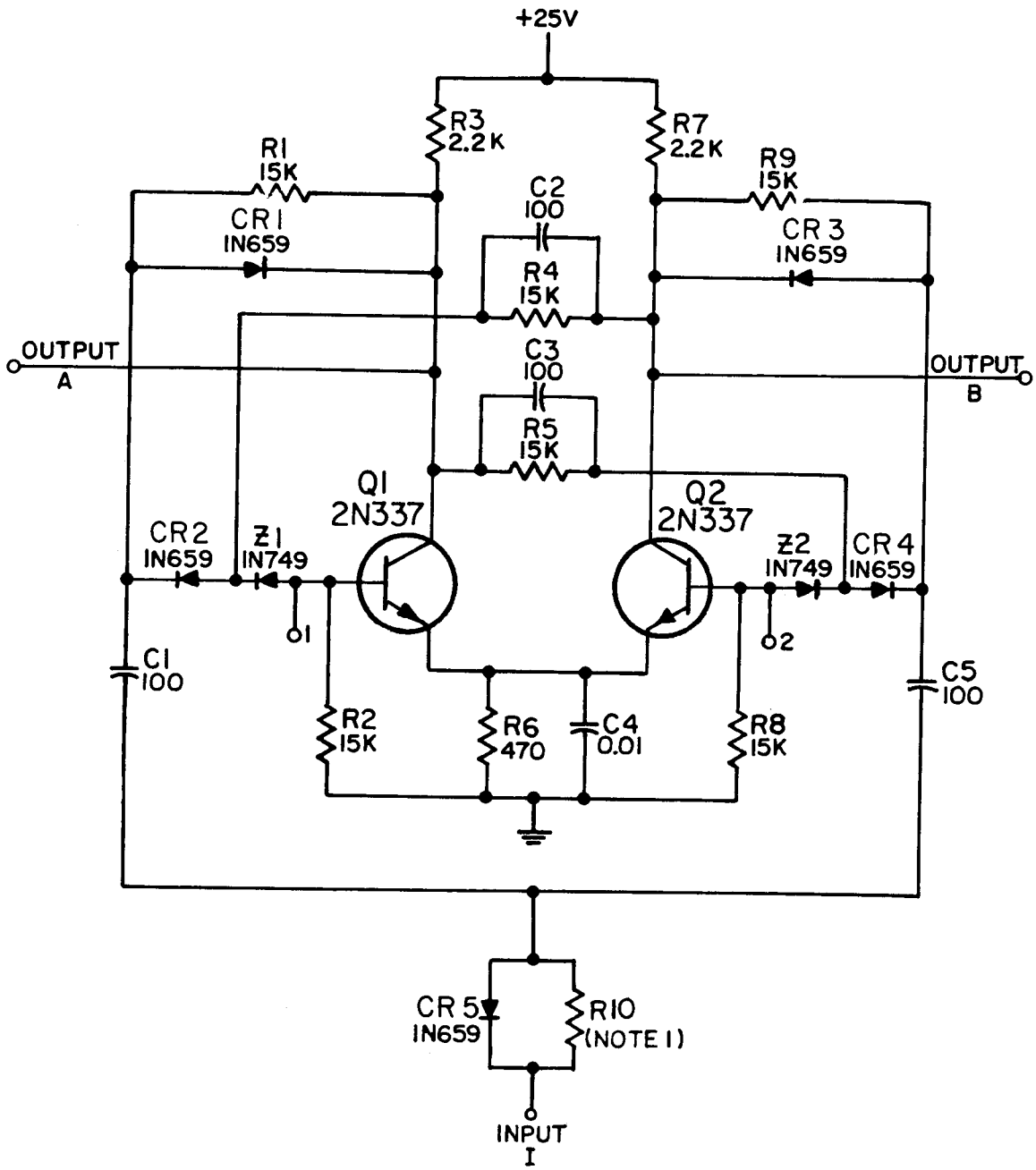
Resistive loading of the output is limited to 8KΩ or more over the range of R1 from 10KΩ to 100KΩ. Loading down to 5KΩ is possible when the minimum setting of R1 is 30KΩ. Capacitive loading up to 500 μμf will have little effect on gate fall time, but 220 μμf is maximum to preserve the 1.0 μsec rise time limit indicated on the circuit sheet, p. 252–3.

3.2 *Input:* Any input variations within the limits specified on page 252–3 will have negligible effect (less than 0.1%) on the output gate width. The output gate width is sensitive to a positive-going wave front which occurs at or near the end of the gate. For this reason the maximum trigger duration is limited to less than 50% of the gate width.

NBS PREFERRED CIRCUIT NO. 253
NON-SATURATING BISTABLE MULTIVIBRATOR

NBS PREFERRED CIRCUIT NO. 253

NON-SATURATING BISTABLE MULTIVIBRATOR



Unless otherwise stated: R in ohms; C > 1 in $\mu\mu$f; C < 1 in μf; L in μh

(For specifications, see next page)

Components:

Z1, Z2: 4.3 volts ±10% at 5 ma.

Approximate power dissipation: R1, R2, R8, R9, R10: <0.01 watt; R4, R5: 0.02 watt; R6: 0.05 watt; R3, R7: 0.15 watt.

Limits (these are not tolerances; see note 2 below): R3, R4, R5, R6, R7: ±10%; R1, R2, R8, R9, R10; ±20%. C1, C2, C3, C5: ±10%; C4: ±20%.

Operating characteristics:

Temperature range: −55° C to +125° C.

Maximum operating rate: 1 mc.

Input signal:

Polarity: Negative.

Amplitude: 12–20 volts.

Rise time: 0.4 μsec (max.) for 1 mc operation. (Note 3)

Fall time: .04 to 0.4 μsec for 1 mc operation. (Note 3)

Input impedance: 110 μμf.

Output amplitude: 16 volts. (Note 4)

Delay: 0.2 μsec (max.). (Start of trigger to start of output.)

Loading:

Input: 1000 μμf (max.).

Output: 220 μμf total both outputs, 1 mc operation.
440 μμf total both outputs, 500 kc operation.

Power requirements: 25 volts ±5% at 10 ma.

NOTES:

1. If the input signal has a fall time shorter than 0.3 μsec, the input diode CR5 and resistor R10 must be included to prevent false triggering by the trailing edge of the trigger. For fall times between 0.15 and 0.3 μsec, a 470Ω resistor is satisfactory. If the fall time is less than 0.15 μsec, a 1KΩ resistor should be used. The input diode and resistor need not be added between cascaded stages.

2. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.

3. For 500 kc operation, the maximum rise time is 0.6 μsec. Maximum fall time is limited only by the repetition rate.

4. The maximum variation in output amplitude is ±1% plus the percentage change in supply voltage. The output amplitude may vary ±1% over the temperature range; variation in the supply voltage will cause an equal percentage variation in output amplitude.

PC 253 BISTABLE NON-SATURATING MULTIVIBRATOR

1. APPLICATION

PC 253 is a bistable counting multivibrator which is used for frequency division of pulse trains when high stability is required. Cascade connection with appropriate feedback can provide any desired ratio. Among other uses of PC 253 are coding, gating, and synchronizing.

2. DESIGN CONSIDERATIONS

Achievement of high counting rates with grown junction silicon transistors requires that the collector current saturation region be avoided, since when saturation occurs, the charge stored in the base region increases the trigger voltage requirement and prevents the transistor from turning off quickly. Saturation is avoided in PC 253 by using breakdown diodes to prevent the collector junction from becoming forward biased. This is believed to be one of the best of the several methods available in that it does not require several low impedance supply voltages or selection of transistors. In addition, the output voltage is highly stabilized against changes as the temperature varies.

Saturation does occur in PC 253 if the breakdown diodes Z1 and Z2 are removed, even though, under these conditions, a back voltage of 0.9 volts is measured between collector and base of the ON transistor. This voltage, measured at the transistor terminals, does not indicate the actual condition at the collector junction. In the 2N337 it was found that the voltage drop across the bulk resistance of the collector material is sufficient to cause a back voltage to be measured at the transistor *terminals* even when the collector *junction* is forward biased. If saturation is to be prevented, therefore, the collector-to-base voltage must be clamped high enough to allow for this added voltage drop in the collector circuit.

2 1 *Switching and Steering:* The operation of PC 253 is conventional except for the breakdown diodes, Z1 and Z2, which prevent the collector-to-base voltage of the conducting transistor from entering the saturation region. The circuit is triggered by a negative-going wave front at the base of the ON transistor. Positive-going wave fronts are rejected and the negative-going wave fronts directed to the correct stage by steering diodes CR2 and CR4. When the circuit is in the quiescent condition, the dc voltages applied to these diodes through R1 and R9 are such that the diode associated with the OFF transistor (CR2, figure 253-1) is biased off by approximately 18 volts, while the diode associated with the transistor to be switched (CR4, figure 253-1) is biased in the forward direction. Clamping diodes CR1 and CR3 provide low resistance paths for the discharge of capacitors C1 and C5 after a positive-going wavefront or after the trailing edge of a negative trigger. Input resistor R10 is added to slow the rise of positive-going wave fronts, since these are coupled, through the clamping diode associated with the ON transistor, to the base of the OFF transistor and may cause false triggering. Diode CR5 bypasses R10 for negative-going wave fronts so that the rise time of the desired trigger is unaffected. The diode and resistor need not be included if the rise of positive-going wave fronts is longer than 0.3 μsec.

2.2 *Static Conditions:* The dc voltages (figure 253-1) are such that all three diodes associated with the ON transistor are conducting. Diodes CR3 and CR4 conduct in the forward direction, and breakdown diode Z2 conducts in the reverse direction. Collector-to-base voltage, V_{CB}, of the ON transistor may thus be represented as

$$V_{CB} = -V_{CR3} - V_{CR4} - V_{Z2}$$

where all voltage drops are in the conventional current forward direction. Typically $V_{CB} = -0.5 - 0.5 + 3.2 = 2.2$ volts. Variation in this value with temperature is small due to the canceling effect of the voltage drops, i.e., all three diodes have negative temperature coefficients, but the breakdown diode contributes a positive voltage drop while the other two diodes contribute negative voltage drops.

Typical potentials associated with the ON transistor over the temperature range are given in Table 253-1. Collector-to-emitter voltage, V_{CE}, equal to the sum of V_{CB} and V_{BE}, is seen

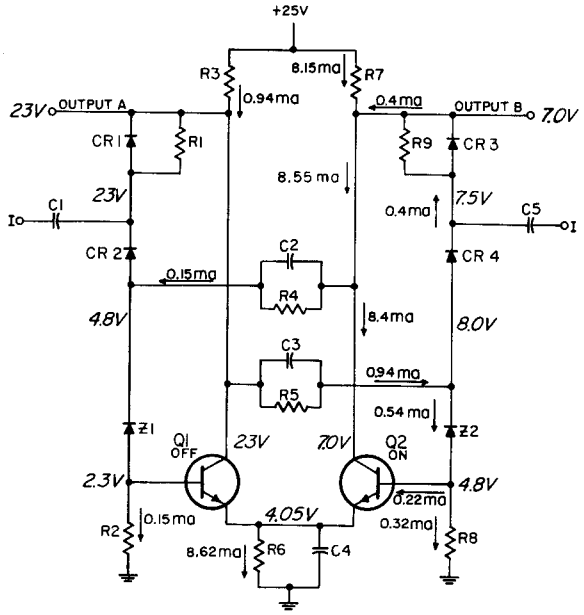


Figure 253–1.—Typical currents and voltages with Q2 conducting.

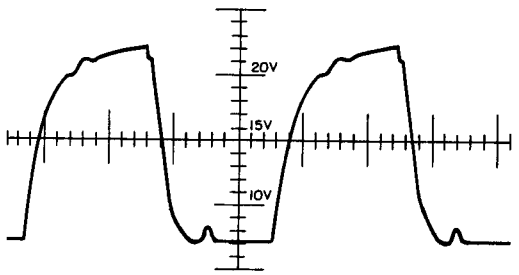
to be practically constant, thus stabilizing the collector current against changes in temperature. The OFF collector voltage is not dependent on the transistors and hence is relatively independent of temperature, while the ON collector voltage is determined by the collector current, I_C, which is stabilized. As a result the output voltage, equal to the difference between transistor ON and OFF collector voltages (see figure 253–1) is also stabilized against temperature changes.

TABLE 253–1.—*Potentials associated with the conducting transistor*

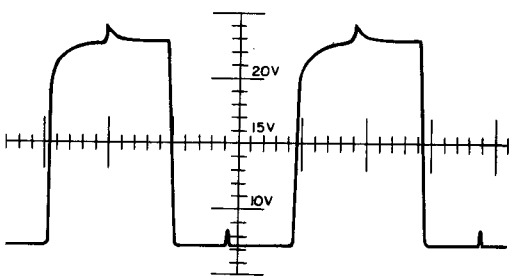
	−55° C	+25° C	+125° C
V_{Z_2}	3. 4V	3. 2V	2. 85V
V_{CR3}	0. 7	0. 5	0. 3
V_{CR4}	0. 7	0. 5	0. 3
V_{CB}	2. 0	2. 2	2. 25
V_{BE}	0. 9	0. 75	0. 65
V_{CE}	2. 9	2. 95	2. 9

3. PERFORMANCE

The operating characteristics shown on page 253–3 are conservative. Input resistor R10 is not needed if the rise of positive-going wave fronts is slow or if operation is confined to room temperatures. In the latter case, if the rise time of the negative input signal is less than 0.1 μsec, PC 253 can be triggered by a signal of 4 to 8 volts, and the counting rate and output loading may both be increased. When the transistor beta increases with temperature, higher input voltages are required, necessitating the addition of the input resistor to prevent false triggering. The input signal voltage level will be less critical if the transistors are selected to obtain betas near the center of the range. Typical output voltage waveforms are shown in figure 253–2.



(a) 1mc operating rate



(b) 100kc operating rate

Figure 253–2.—Typical output voltage waveforms.

4. EXAMPLE OF USE

A typical method of connecting four stages of PC 253 to obtain a decade counter is shown in figure 253–3. Capacitor C1, resistor R2,

and diodes CR2, CR3, and CR4 introduce feedback of the correct polarity to convert binary operation to decade operation.[1] If the input to the decade has a fall time shorter than 0.3 μsec, input diode CR1 and resistor R1 must be included to prevent false triggering. (See note 1, page 253–3, and section 2.1.)

[1] J. Millman and H. Taub, *Pulse and Digital Circuits*, McGraw-Hill, New York, 1956, p. 327.

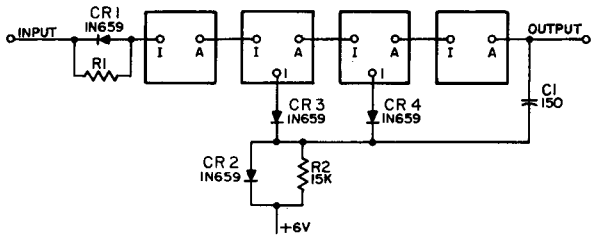


Figure 253–3.—Connection of PC 253 for decade counting.

NOTES TO THE PREFERRED CIRCUITS MANUAL

PART 2

NOTES TO THE PREFERRED CIRCUITS MANUAL

1. BASIC CONSIDERATIONS

Within any class of electronic equipment there are a number of identical functions to be performed; however, there are usually several circuit designs for each function. Usually no one of the designs is particularly better than another. These factors make it desirable and possible to develop one circuit design to replace the many designs performing one function.

Based on the experience of industrial groups and a detailed survey of the problem, the following method of approach was developed:

(*a*) Review the state of the art.

(*b*) Compare types of circuits performing identical or similar functions.

(*c*) Study system requirements.

(*d*) Design "preferred circuits" based on the present state of the art to meet these requirements.

(*e*) Make this information available to all interested parties to stimulate discussion and exchange of ideas leading to the adoption of standard circuits.

(*f*) Revise and add to this information when, or if, new and improved circuits of better performance or reliability become available.

Several general rules were chosen for guidance in the design of the preferred circuits:

(*a*) The fundamental unit must be a functional unit without regard to the number of tubes included.

(*b*) The circuits should represent the highest performance consistent with conservative and stable design.

(*c*) The circuits must be sufficiently flexible so that any of the modular, plug-in, miniature, or subminiature types of construction can be used.

(*d*) Tubes should be chosen from reliable types in large quantity production. Electrical equivalents are included with exact choice depending upon application.

(*e*) The circuits must perform satisfactorily using any tube that falls within the limits allowed by MIL–E–1B specifications including the end-of-life requirements.

(*f*) The number of different capacitors and resistor values should be restricted as much as possible within the R–E–T–MA and MIL preferred series.

Every effort has been made to design the preferred circuits to minimize interaction. Electronic circuits are not, however, ideal building blocks. The user of preferred circuits must keep this factor constantly in mind.

1.1 *General Design Considerations:* In considering the technical feasibility of circuit standardization, many questions arise. The first and one of the most important of these is concerned with the voltage levels that are chosen by the designer. Fortunately there are a few definite design principles which designers follow and have therefore almost completely standardized.

Taking these in functional groups:

(*a*) Video circuits:

(1) Diode detectors in receivers must operate above 1 volt to be linear, and operation at more than 6 or 7v becomes inefficient because of af versus i-f gain considerations.

(2) The transmission of wide-band video signals over long distances must be at low levels (about 1 volt) or expensive cable drivers must be included.

(3) Operations such as mixing, gating, or limiting are more readily accomplished at specific levels.

(4) Display tubes require about the same signal drive voltages because of electron

optical considerations. Therefore the same amount of gain is required to raise the transmission signal level to drive level.

(5) Linear amplification requires that the tubes must not be overdriven and therefore further restricts the choice of level.

(*b*) Timing and display circuits:

(1) Accuracy of timing depends largely upon rate of voltage change. Therefore most timing waveforms must be of high amplitude but usually not more than is necessary to drive a grid from cutoff to conduction. A range of 30 to 70v covers most cases.

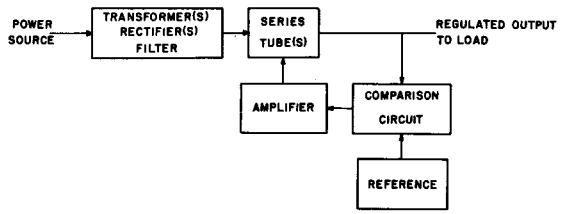
(2) Gating waveforms of display tubes must be of the same order of magnitude because of the similarity in characteristics of all display tubes.

(3) Deflection waveforms depend somewhat upon deflection components but even these are becoming stabilized in design with a small range of characteristics. At stages prior to drive stages, the deflection components have little effect.

The design criteria enumerated above are not meant to be all-inclusive but only to indicate a few of the functional similarities that exist.

2. REGULATED POWER SUPPLIES

The subject of regulated power supplies may be considered in two parts: the first includes the ac regulator, if any, power transformer, rectifier, and filter; the second is the dc regulator. The regulator considered here is the negative feedback electronic type (fig. 2–1). This regulator



BLOCK DIAGRAM OF REGULATED POWER SUPPLY

FIG 2–1

may in turn be subdivided into four parts: series tube, dc amplifier, comparison circuit, and reference circuit. The last three may be considered a unit called the "regulator-amplifier." This subdivision serves the purpose of circuit standardization because the design of the regulator-amplifier depends primarily upon the degree of voltage regulation required and is relatively independent of the current to be supplied.

A study was made of 20 equipments to determine the types of regulators in use; the apparent performance requirements (specifications were absent in most cases); and the characteristics of each from the standpoint of gain, stability, ripple reduction, output impedance over a frequency range, and ease of adjustment.

The frequency of use of plate supply voltages is shown in figure 2–2. It was found that voltage supplies of +300, +150, −150, and −300v can satisfy the majority of requirements.

2.1 *Examples of Circuits in Current Use:* The regulator amplifiers were divided into groups according to the output voltage desired. Five configurations were distinguished within each group: single pentode, twin-triode cascode, twin-triode pentode (balanced in-

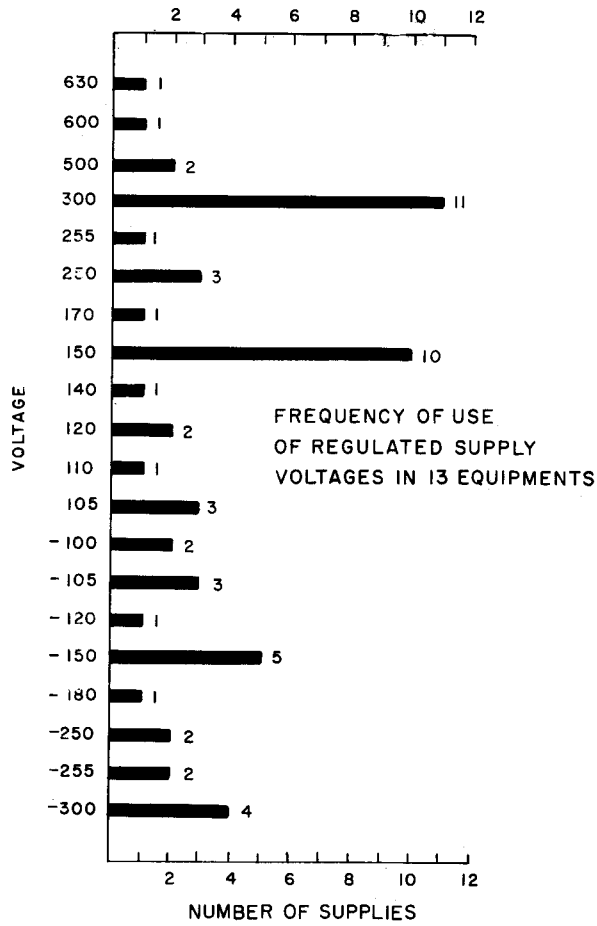


FIG. 2–2

put), and pentode twin-triode (balanced output).

Within each configuration there are variations in polarity of reference potential, choice of connection for output load resistor, size of output load resistor, and for the single-pentode type, choice of screen connection.

2.2 *Positive Output 250 and 300 Volt Regulators:* Figures 2–3 through 2–6 show eight circuits designed for 300v output and one for 250v output. These circuits were selected to show some of the circuit configurations.

(*a*) Single pentode: Three pentode-regulator circuits are included. In the circuit of figure 2–3a, the plate load resistance of the 6AK5 is high (1 megohm), resulting in poor frequency response. The reference tube is in the cathode circuit of the 6AK5; therefore, the current follows variations of

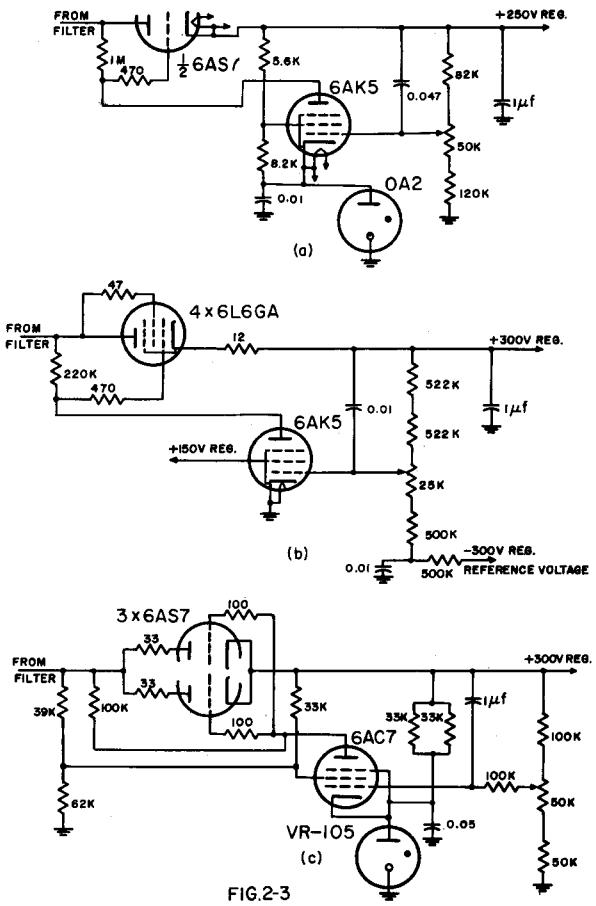


FIG.2-3

the 6AK5 current. The 6AK5 screen is fed from the regulated output through a divider.

The circuit of figure 2–3b has a smaller load resistor (220KΩ), allowing better frequency response. The screen is fed directly from a regulated voltage. The reference circuit is connected to an external negative supply. Its current does not vary since the only load is the 6AK5 grid. The circuit uses a 6L6 series tube. The 300v negative reference comes from a shunt regulating supply using VR–105 and VR–150 reference tubes.

Figure 2–3c is a circuit similar to 2–3a except that the screen is fed jointly from the unregulated and regulated sides of the supply. This method of supplying dc for the screen reduces ripple. The plate resistor is low (100KΩ), providing good frequency response but increasing the current fluctuation through the reference tube.

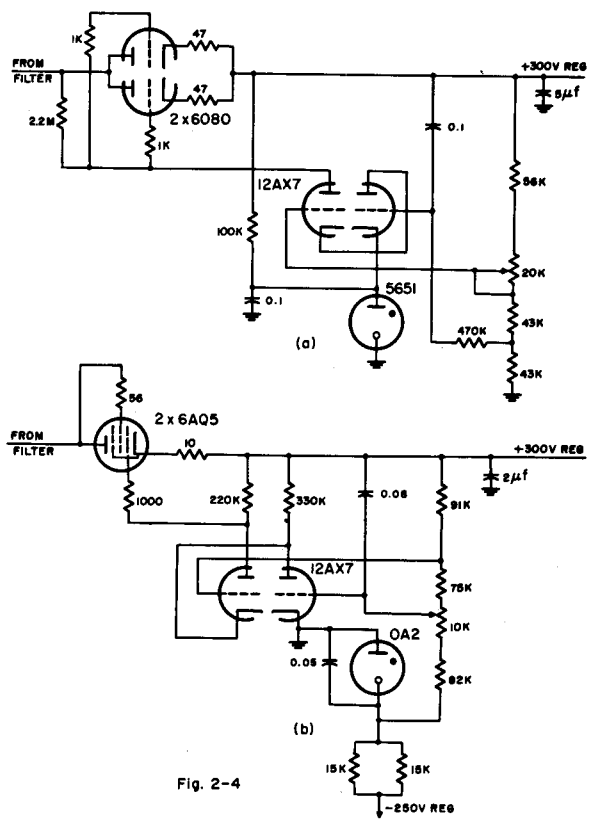


Fig. 2-4

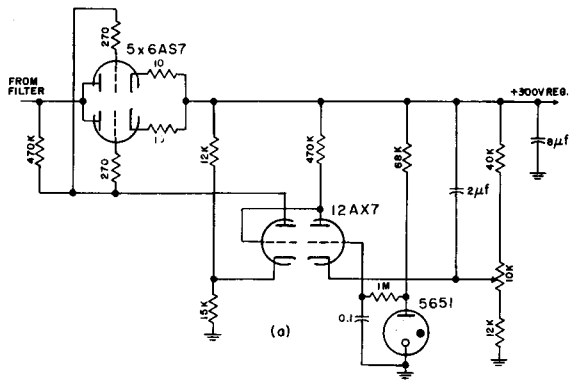
(*b*) Twin-triode cascode: Figure 2–4a is a true cascode circuit. The inherent frequency response is poor due to the 2.2MΩ plate load resistor. This effect is reduced by the use of 5μf capacitor across the regulated output. A 5651 voltage reference tube in the cathode return has the variable tube current flowing through it. The magnitude of this current is small, however, due to the large resistor in the plate circuit. The cascode circuit is employed when the required gain is too high for a single triode, avoiding the need for a second dc supply, as required for the screen when a pentode is used. It should be noted, however, that the low input impedance of a high-mu triode, compared with that of a pentode, may result in far less gain than theoretically available under conditions of small negative bias and low plate-cathode voltage. [1]

Figure 2–4b is a modified cascode. The plate resistor for the lower potential triode parallels the top triode, which is the plate load for the true cascode. This increases the gain of the circuit by

[1] J. L. Lawson, *Notes on the Design and Construction of Regulated Power Supplies, Rad. Lab. Report No. 44*, Section IV; Feb. 26, 1945.

increasing the average plate current and therefore the g_m of the bottom triode. [2]

(*c*) Twin-triode cascade: Figure 2–5a illustrates a circuit theoretically capable of the greatest gain among the single-envelope dc amplifiers in the examples surveyed. The 470KΩ output load resistor used gives a frequency response intermediate between the extremes noted in the previous circuits. In addition to high gain, this circuit has a self-contained reference voltage,



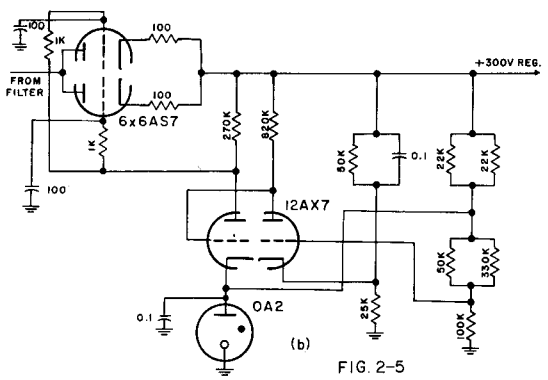


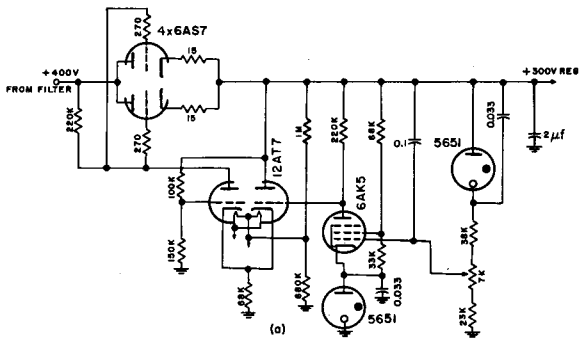
FIG. 2–5

and does not "load" the reference tube. The cathode of the input triode "loads" or shunts the divider which provides the comparison voltage. Another such divider paralleling the first is loaded by the cathode of the output triode. The two dividers must have low resistance. In the circuit shown, these dividers draw a total of 15ma from the output side of the regulator.

The use of two amplifier stages requires three coupling networks, and the cumulative phase-shift may cause oscillation unless precautions are taken.

The circuit of figure 2–5b uses a smaller load resistor, allowing better frequency response. The second divider is replaced by the reference tube and its dropping resistor. This reduces the "internal current" used by the regulator but requires a higher-current reference tube, leaving the total internal current essentially constant. In this example both the reference tube and the comparison divider are "loaded."

(*d*) Pentode twin-triode (balanced output): The example shown in figure 2–6a uses a twin-



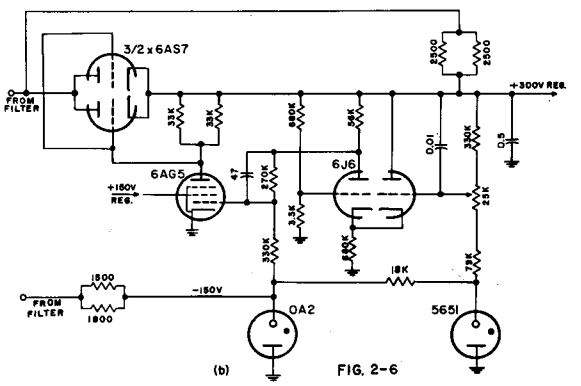


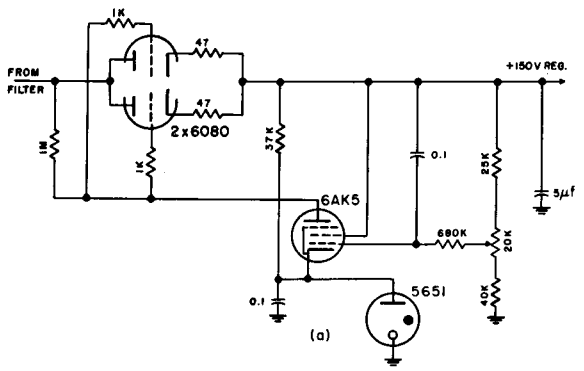
FIG. 2–6

triode, a pentode, and two 5651 reference tubes in the regulator amplifier. The pentode is used as a high-gain input stage. The 5651 in series with the voltage divider increases the over-all dc gain of the amplifier by a factor of 1.5. This arrangement results in high gain, approaching 10,000. This circuitry was designed for maximum ripple reduction in a particular radar development program. Subsequent work showed that the ripple was due to external pickup, and the circuit was replaced by a much simpler twin-triode cascade.

[2] V. H. Attree, A Cascode Amplifier Degenerative Stabilizer, *Electronic Engineering*, April 1955, pp. 174–177.

(e) Twin-triode pentode (balanced input): The unit of figure 2-6b uses a twin-triode balanced input stage to reduce the effects of tube aging and heater voltage change. The output pentode has a 16.5KΩ plate load resistor resulting in the best frequency response of all the circuits. The twin-triode-to-pentode coupling uses a "phase lead" network for stabilization against oscillation. Neither the reference tube nor the comparison voltage divider is loaded. Although the loop gain is only 300, the circuit is capable of yielding the best over-all performance of the regulator amplifiers shown.

2.3 *Positive Output Regulators for 150 Volts or Less:* Regulators designed for output voltages of



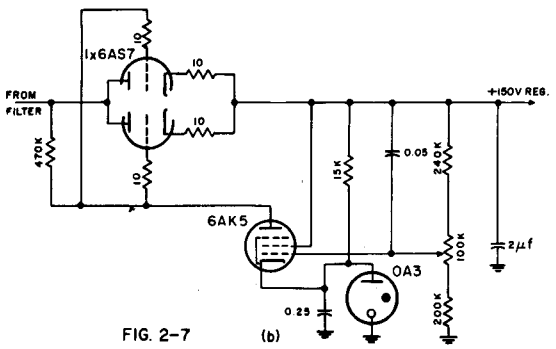


FIG. 2-7

150v or less usually contain external negative reference potentials. Marginal operation may be obtained with pentode regulator amplifiers having self-contained positive reference potentials such as the two examples of figures 2-7a and 2-7b.

In the example of figure 2-8 an external negative source makes possible a wider supply voltage range and will permit better operation.

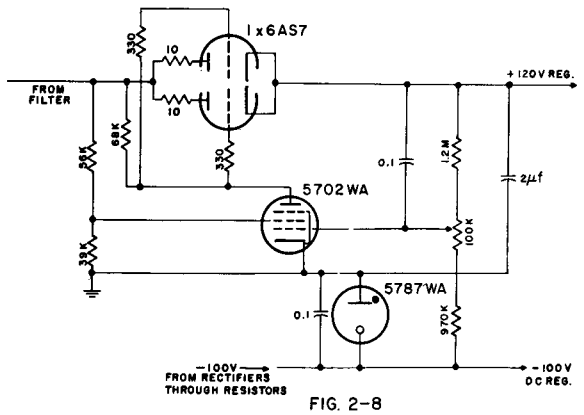
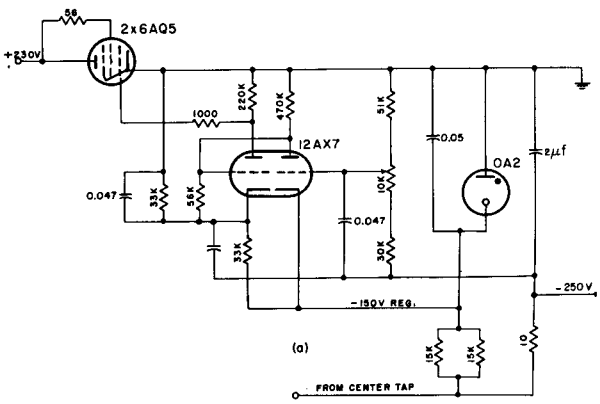


FIG. 2-8

2.4 *Negative Output Regulators:* Circuits similar to those previously discussed have been utilized for negative operation. Typical examples are shown in figures 2-9 and 2-10.



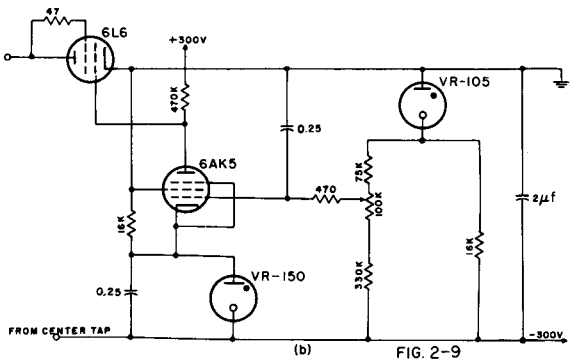


FIG. 2-9

2.5 *Summary:* From this survey it appears that two degrees of regulation are required. A great many applications can be met with supplies which have limited regulating ability of about 1%. More precise applications require a regulation capability considerably higher — about 0.1%.

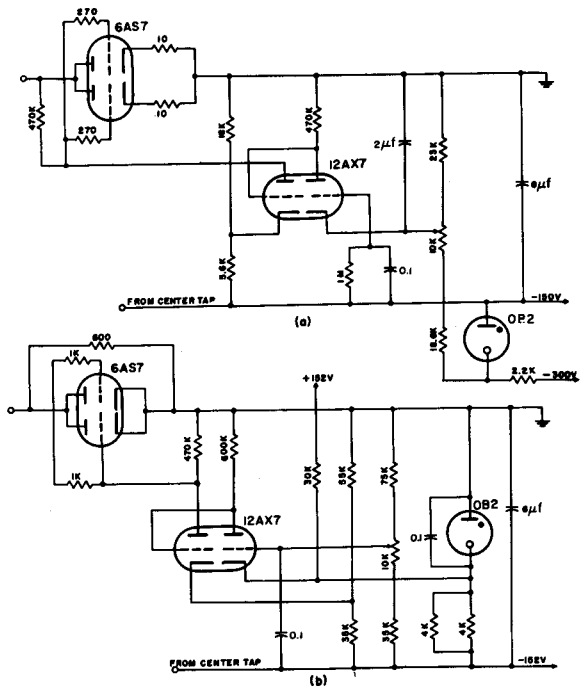


FIG. 2-10

It appears that only four voltages, +300, +150, −150, and −300v, should be required in most cases.

2.6 *Series Control Tube for Regulated Power Supplies:* There are three frequently encountered applications of series regulator tubes.

(1) A triode-connected beam power tube of the 6L6 variety.

(2) A low-mu, high perveance tube of the 6AS7 type.

(3) A beam power tube of the 6L6 type with a separate screen supply.

Applications (1) and (2) are in most common use at present. Type (1) has higher μ and narrower MIL-E acceptance tolerances. This results in higher gain and greater useful percentage of rated capacity, and requires lower plate swing of the dc amplifier.

Application (2) has the advantage of higher heater-cathode voltage rating and lower dc plate resistance. The MIL specifications for the 6AS7 and 6080 were drawn up for use of the tubes as low-impedance drivers, pulse generators, etc. Their primary use as a series tube in a degenerative voltage regulator was not considered. As a consequence, the minimum μ specified is too low. This factor and the unrealistic test setup for determination of tube balance makes it necessary to derate the tubes by 20% and use a cathode equalizing resistor when using tubes in parallel. Despite this drawback, the 6AS7 and 6080 remain the best practical choices for series tubes in equipment where minimum power loss in the regulating circuit is a prime consideration.

Application (3) has appeared in recent laboratory equipment. This circuit has the advantage of (1) and has a lower minimum static plate resistance and a higher plate dissipation than a single triode section of a 6080. It has the disadvantage at the present time of the added weight, complexity of screen supply, and the greater space factor due to the use of single envelopes per pentode compared to the dual envelope 6080. Dual pentodes such as the 815, however, eliminate this. Although the heater-cathode potential is less than that for the 6080, the maximum plate voltage is greater. The 6080 is rated at a maximum of 300v heater to cathode. This rating is too close for a nominal 300v supply (including the peak inverse voltage). The 180v rating of the 6L6 is satisfactory for a 150v supply. The heater winding necessary for the heaters of the 6080's in large supplies is usually separate, however, and can be floated as easily as grounded.

Having decided on the 6080 and equivalents, the problem of plate current equalization will be examined.

(*a*) Plate current equalization: During the course of the survey, a wide variation was found in the value of equalizing resistors used to improve

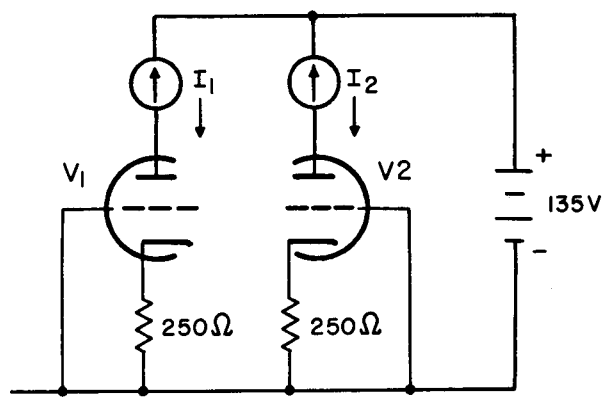


Fig. 2-11 TEST SETUP FOR MIL-E SPECS

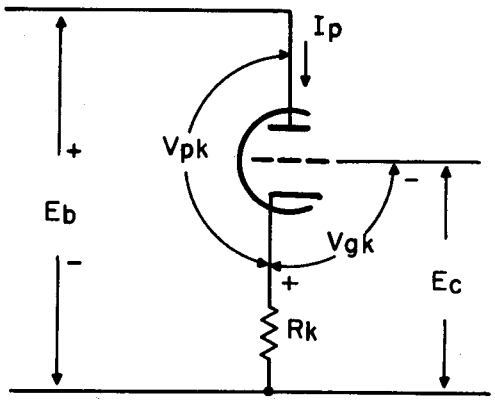


Fig. 2-12

the balance in plate current among 6AS7 triode units operated in parallel. Work was done to determine the best value or values to be used for this purpose. A qualitative analysis was undertaken from a theoretical standpoint to determine the chief factors affecting balance and their variation with plate voltage, cathode resistance, etc. This analysis, shown in detail later in this section, leads to the following conclusions:

1. In general, the first few ohms of cathode resistance are most effective in improving plate current balance.
2. The variation in μ between tubes is the prime factor in causing unbalance.
3. As a direct consequence of the variation mentioned in 2, unbalance is greatest in tubes operating under conditions of high negative bias when the value of fixed bias is much greater than the bias voltage developed across the cathode equalizing resistors.

In order to check the validity of this conclusion, and determine the quantitative behavior of tubes with variation in bias and cathode resistor values, twenty-six 6AS7 twin triodes were selected from a group of 75 tubes available for test. These tubes were selected for apparent initial unbalance, and are not to be thought of as a random sample. The purpose in so selecting the tubes for test was to show that plate current unbalance is a function of fixed bias, and increases with magnitude of negative bias.

The 26 tubes were tested in the following manner:

1. Regulated voltage of 112 volts was applied from plate to ground. This value was used because the maximum rated cathode current of 125ma times 112 volts equals the maximum rated dissipation of 14 watts per triode section.
2. A negative voltage source was connected between the tube grids and ground.
3. Resistor values of 0, 10, and 47 ohms in turn, were inserted between cathode and ground of the triode sections of each 6AS7. In each case, the fixed negative bias was so adjusted that the tube section drawing the maximum current drew 120ma, which was chosen because it was a convenient value slightly below 125ma. The percentage balance, or the ratio of current through the lower current section to 120ma, was computed.

The test results are shown graphically in figure 2–13. The number to the right of each curve identifies the tube tested, while the negative number along each curve shows the value of fixed negative bias used when the value of cathode resistor is 47Ω.

The test points on each curve are shown by dots at 0, 10, and 47 ohm points on the abscissa scale.

It will be noted that the equalization afforded under conditions of severe unbalance is a nearly linear function of resistance up to a value of 47Ω, whereas the equalization afforded for reasonably balanced tubes is not great in the case of values approaching 47Ω.

Equalizing resistors in the cathode deteriorate the performance of the circuit. The recommended choice of 33Ω noted in PC 1, 2, and 3, is a compromise between maximum equalization and minimum performance deterioration.

A sample of seven tubes from the previous test were retested using the arrangement of figure 2–11 (the test set up for MIL–E–1B specifications). This test included tubes 1 and 12 which were among the poorest cases of balance found in the prior test. The results for these tubes, as shown in table No. 2–1, were within the plate current limits of 100 to 150ma set by MIL–E–1B specifications.

On the basis of these tests, a value of 33Ω is selected for use in the tube cathodes. This value, as well as the highest (47Ω) used in the tests is insufficient to correct for the severest cases of unbalance found. In the case of reasonably

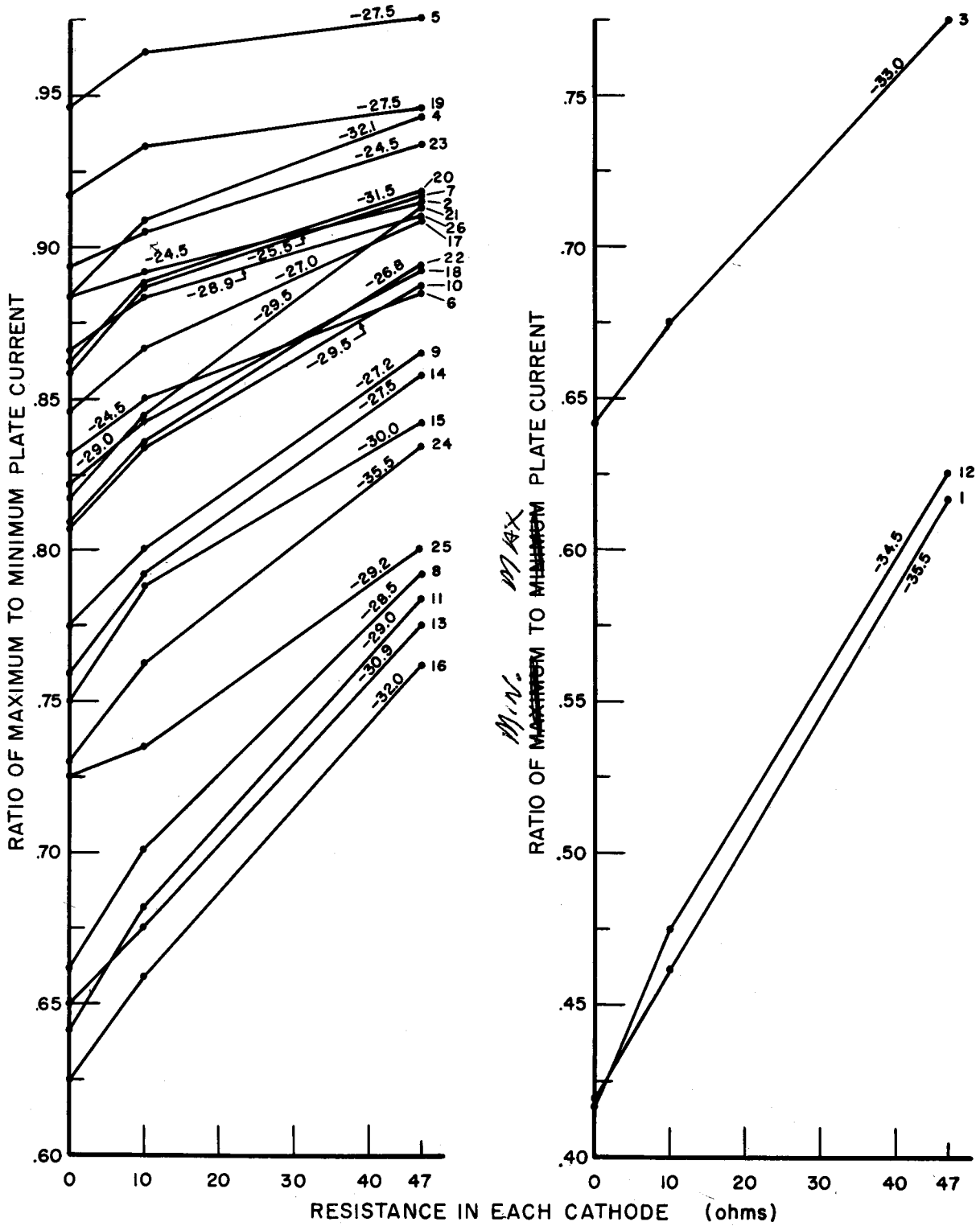


Fig. 2-13 6AS7 BALANCE TEST

TABLE 2-1—*Balance Test—6AS7*

E_p v	R_k Ω	Tube No.	I_1 ma	I_2 ma	Percent balance
135-----	250	1	143.0	119.0	83.0
135-----	250	8	131.0	115.0	87.8
135-----	250	11	132.5	115.0	86.8
135-----	250	12	144.0	116.5	81.0
135-----	250	13	136.0	118.0	86.8
135-----	250	16	138.0	120.0	87.0
135-----	250	20	126.5	127.5	99.5

balanced tubes, initial values of balance of 75% or better, this value will give an effective balance of better than 80%.

(*b*) Approximate analysis: The test circuit for determining acceptance of 6AS7 and 6080 tubes under MIL-E1/49A and MIL-E1/209 respectively is shown in figure 2-11. The acceptance limits for μ and plate current are

	Minimum	Maximum
μ	1.4	2.6
I_p	100ma	150ma

Figure 2-12 shows the general circuit for a triode cathode follower.

The equation for current flow of a planar triode is

$$I_p = G(V_{gk} + \frac{V_{pk}}{\mu})^{3/2} = \frac{G}{\mu^{3/2}}$$

$$(\mu V_{gk} + V_{pk})^{3/2} = K(\mu V_{gk} + V_{pk})^{3/2}$$

where $K = \frac{G}{\mu^{3/2}}$. Let $V_{gk} = E_c - I_p R_k$ and $V_{pk} = E_b - I_p R_k$.

$$\therefore I_p = K[\mu (E_c - I_p R_k) + (E_b - I_p R_k)]^{3/2} = K[\mu E_c - (\mu + 1) I_p R_k + E_b]^{3/2}.$$

Variations in the geometry of a planar triode changes the μ and the static plate resistance in the same direction. The equivalent diode would have a larger plate cathode spacing for the higher μ tube. For a given value of bias voltage and plate-cathode voltage, the tube with the lowest μ will be most likely to pass the largest current. On this basis, it is assumed that a triode section passing 150ma under test conditions of figure 2-11 will probably have a μ of about 1.4, while a section passing 100ma will have a μ of 2.6. Letting $E_c = 0$ we can solve for $K_1^{2/3}$ thusly:

$$I_p = K[E_b - (\mu + 1) I_p R_k]^{3/2} \text{ or } K = \frac{I_p}{[E_b - (\mu + 1) I_p R_k]^{3/2}} \quad (1)$$

$$K^{2/3} = \frac{I_p^{2/3}}{E_b - (\mu + 1) I_p R_k} \quad (2)$$

If we substitute the values of μ_1 equals 1.4 and I_{p1} equals 150ma in equation (2), we can solve for $K_1^{2/3}$ thusly:

$$K_1^{2/3} = \frac{(.15)^{2/3}}{135 - (2.4)(.15)(250)} = 6.27 \times 10^{-3}.$$

In a similar manner for $\mu_2 = 2.6$, $I_{p2} = 100$ma,

$$K_2^{2/3} = \frac{(.1)^{2/3}}{135 - (3.6)(.1)(250)} = 4.8 \times 10^{-3}.$$

In a planar triode where the grid cathode spacing approaches or is smaller than the grid pitch, μ and K will vary with grid bias. However, this will occur in all tubes of the same type in a similar manner, and although quantitative results may not be obtained by assuming constant μ and K, valid qualitative results may be so derived.

Therefore assuming μ and K to be constant under the changing bias conditions we have

$$I_p^{2/3} = K^{2/3}[E_b - (\mu + 1) I_p R_k + \mu E_c].$$

Now we may assume values of E_c, R_k, E_b and solve for I_{p1} and I_{p2} by substituting the values of $K_1^{2/3}$ and $K_2^{2/3}$ in turn. The solutions are accomplished by trial and error and are tabulated in table 2-2 for five cases. The first row of table 2-2 tabulates the conditions and % balance for the two hypothetical triodes chosen. In the second and third rows are shown the effects of a −10v fixed bias with 100 and zero ohms of cathode bias respectively. In the fourth, fifth and sixth rows are shown the effects of a −30 volt fixed bias and 100, 10 and zero ohms of cathode resistance respectively.

(*c*) Practical considerations: On the basis of these tests, a value of 33Ω is selected for use in the cathode circuit. This value, as well as the 47Ω value used as a maximum in the test, is insufficient to correct for the severest cases of unbalance found. In the case of reasonably balanced tubes, initial values of 75% balance or better, this value will give an effective state of balance of better than 80%.

There are three alternatives for arriving at a recommendation for the use of a preferred com-

TABLE 2-2—*Computed Plate Current Balance*

Lower μ Limit Tube $\mu_1=1.4$, $K_1^{2/3}=6.27\times10^{-3}$				Upper μ Limit Tube $\mu_2=2.6$, $K_2^{2/3}=4.8\times10^{-3}$				% Balance $\frac{I_{p2}}{I_{p1}}\times100$
$E_c=0$	$E_b=135$v	$R_k=250\Omega$	$I_{p1}=0.150$a	$E_c=0$	$E_b=135$v	$R_k=250\Omega$	$I_{p2}=0.100$a	66.7
$E_c=-10$v	$E_b=100$v	$R_k=100\Omega$	$I_{p1}=0.161$a	$E_c=-10$v	$E_b=100$v	$R_k=100\Omega$	$I_{p2}=0.09$a	55.8
$E_c=-10$v	$E_b=100$v	$R_k=0\Omega$	$I_{p1}=0.396$a	$E_c=-10$v	$E_b=100$v	$R_k=0\Omega$	$I_{p2}=0.212$a	53.3
$E_c=-30$v	$E_b=130$v	$R_k=100\Omega$	$I_{p1}=0.165$a	$E_c=-30$v	$E_b=130$v	$R_k=100\Omega$	$I_{p2}=0.057$a	34.5
$E_c=-30$v	$E_b=130$v	$R_k=10\Omega$	$I_{p1}=0.350$a	$E_c=-30$v	$E_b=130$v	$R_k=10\Omega$	$I_{p2}=0.111$a	31.7
$E_c=-30$v	$E_b=130$v	$R_k=0\Omega$	$I_{p1}=0.409$a	$E_c=-30$v	$E_b=130$v	$R_k=0\Omega$	$I_{p2}=0.124$a	30.6

NOTE: Balance conditions computed for hypothetical limit-triode sections in parallel, under varying conditions of cathode and fixed bias.

ponent in a unit. (1) Design around these tubes, using deratings so drastic as to curtail the initial advantages of the tubes. (2) Choose different tubes. (3) Recommend changes in acceptance tests for the tubes. The tubes may then be used within their new limits.

The third alternative has been chosen here. Use of the 6AS7 as a series tube has been chosen on the basis of a new acceptance test.

The critical condition of a series tube is determined by the maximum rated plate power dissipation. Such a condition occurs when the conditions of maximum load current and maximum line voltage occur simultaneously. It is only logical, therefore, that such conditions, which determine the limits of the tube, should be used in any acceptance test. Since some cathode resistance is advocated for equalizing purposes, the test should be made using the applicable plate supply and compensating resistance. A plate supply voltage of 116v and a cathode resistor of 33Ω, for example, in conjunction with proper bias supply voltage for maximum acceptance (about −27v) is suggested.

For a simple amplifier with self-bias, positive grid current (gas or otherwise induced) will flow as shown in figure 2-14. I_g flows through R1+R2 and R3 to the cathode. This positive potential in the grid-cathode circuit reduces the bias and allows more current flow through R3. This current flow in turn increases the bias and reduces excess current flow. If R3 is too small, the current flow through R1+R2 will decrease the bias beyond the power of R3 to compensate. The increased current flow will heat the tube, causing further increase in current flow. The cumulative effect will be overloading and failure of the tube.

In the case of a series tube in a dc regulator, increased positive grid current decreases the series tube impedance, resulting in an increased output potential. This increase in turn is detected by the comparison circuit, resulting in loop action to correct the condition. Therefore, the former restriction does not apply to the case of a single tube. In the case of several tubes in parallel, the following conditions exist. Consider $(n+1)$ triode sections in parallel. Let one section have excess grid current. The bias will be decreased for all

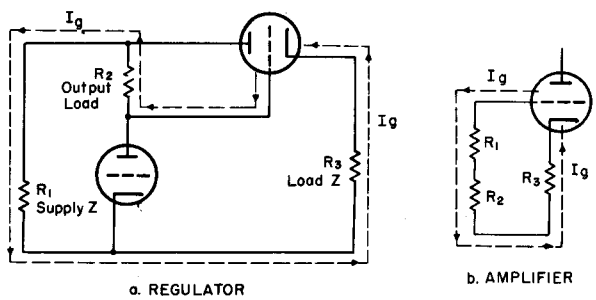


Fig. 2-14 POSITIVE GRID CURRENT FLOW

sections by the same amount. The loop will once again correct for this condition. The bias change will approximately equal:

$$E = \frac{\text{single tube correction}}{(n+1)}.$$

Therefore the magnitude requirement does not hold for the case of a series regulator to the extent that it does for an amplifier circuit alone.

There are two limits on the magnitude of the output load resistor in the case of a regulator amplifier. The first consideration is permissible error. When grid current flows, an error, which is a function of the magnitude of the output load resistor, occurs. Although this error is reduced by the regulator loop, it does exist. Its magnitude after correction is not negligible and may be of sufficient size to negate the additional advantages derived from the use of a large plate load resistor.

The second consideration is supply impedance which is a function of the gain band-width of the complete regulator loop. In most simple degenerative electronic regulators, supply impedance is mainly determined by the plate circuit impedance of the regulator amplifier. The capacitive part of this impedance is large in magnitude and is a function of the number of series tubes. In general, impedance consideration will be the controlling factor.

2.7 *Development of the Preferred Regulator Circuit for ±300v Power Supplies:* There are three simple circuits which may be chosen for 300v supply regulators: the single pentode, the dual-triode cascade, and the dual-triode cascode. The simplest and therefore preferable circuit is the single pentode and was selected for use in the 150v supplies. In the case of a 300v supply, the added plate swing necessary for a given percentage of line voltage variation and the limitations on plate dissipation of a 6080, requiring the maximum utilization of its low static plate resistance, indicated the choice of a cascade amplifier.

The gain of a single pentode is small unless a large plate load resistor is used. Such a resistor results in intolerable decrease in the frequency response. The gain may alternatively be increased by using screen sensing of the input voltage and control-grid sensing of the output voltage. Screen sensing of the input voltage does not counteract non-linearities in the feed-back loop, i.e., the effects of positive grid current. The pentode amplifier used in PC 1 and PC 2 is nonlinear and operates poorly at low input voltage levels. In the case of a 300v supply, the plate swing necessary to control a low-mu tube such as a 6080 under conditions of line voltage variation included in many military specifications is beyond the plate dissipation rating of the tube. The addition of several volts to the minimum operational plate-cathode potential would in many cases not be warranted by the saving in circuit simplification accomplished.

The cascode circuit requires a large plate-load resistor for adequate gain. The reference voltage must be taken from an external source or from a gas tube in the cathode of the input-triode section. The frequency response suffers sufficiently to restrict the area of application.

The cascade amplifier gives the greatest linear gain with reasonable output load impedance. This circuit is more complex than the single pentode and requires a large minimum output capacitor. The reference voltage divider is loaded by the cathode of the input section of the 5751. This divider is critical because of the amount of power dissipated. Despite these drawbacks, the over-all performance of the circuit is sufficient to make it applicable for many uses.

2.8 *Pentode-Connected Pentode Series-Tube Examples:* Figures 2–15a and 2–15b, show examples of pentode-connected pentode series-tubes.

In figure 2–15a, the regulator amplifier is a simple triode. The series tube regulating the 300v

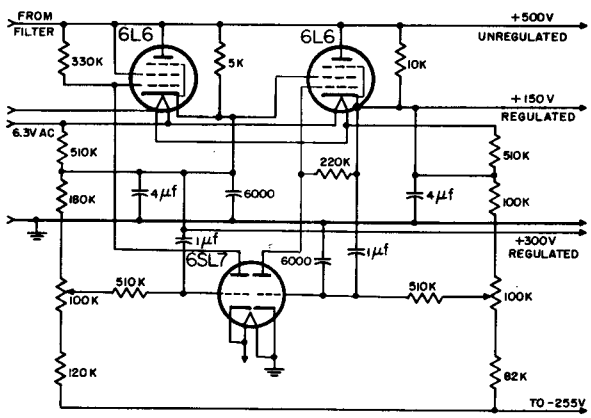


Fig. 2–15 (a)

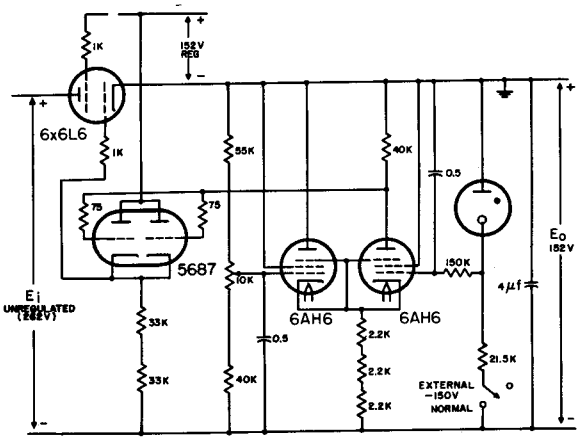


Fig. 2-15 (b)

supply is a conventional triode-connected pentode, but the series tube regulating the 150v supply has its screen fed from the output of the 300v regulated supply. It is therefore a pentode-connected series tube. Maintenance records show almost no reports of difficulty with this supply. Units of this type have been in operation since 1945.

Figure 2–15b shows a regulator using a pentode-connected pentode series-tube that is part of relatively recent equipment. There are very few maintenance reports available on this unit. The regulator amplifier has excellent frequency response, but uses three envelopes. The screen grid characteristics of the 6AH6 will affect tube balance with age and heater changes. The operating point and the use of pentode tubes provide better protection against grid-current flow in the amplifier stage of the cathode-coupled amplifier than could a dual triode, operating with reasonable amplification. Both the cathode follower and the two pentodes draw considerable current, which, while small with respect to the total current available, is not negligible. The excellent frequency response derived thereby does not appear to outweigh the gain which could be derived if the cathode follower were an amplifier using negative feedback for frequency compensation. Such operation would supply better regulation and lower dc resistance.

2.9 *Pentode-Connected Beam Power Series Tube Considerations:* Under Section 2.6, characteristics of series tubes are discussed. The conclusion is drawn that over-all considerations for general purpose voltage regulators lead to the choice of high g_m, low μ triodes such as the 6AS7 or 6080, primarily because of the increased efficiency. Considerations in the design of a 0.1% regulator lead to the choice of a pentode-connected beam-power tube because the reduction in complexity of the regulator amplifier, in the case of 150v supplies in particular, more than makes up for the increased circuitry and added dissipation caused by the pentode screen supply.

Note has previously been made of the use of pentode-connected beam power series-tubes in commercial laboratory supplies. Such supplies, in general, use 6L6 or similar tubes with rather high plate-cathode voltages and with severely derated maximum cathode currents. Tubes such as the 6CU6 or 6BQ6 when operated as pentode-connected beam-power series tubes compare favorably in efficiency with low-mu triodes of the 6AS7 or 6080 type. The 6098 or 6AR6WA beam power tube provides less efficiency than the 6CU6 or 6BQ6 type but is more efficient than the 6L6 type, and in addition, is available as a preferred military type. Further, the specified acceptance

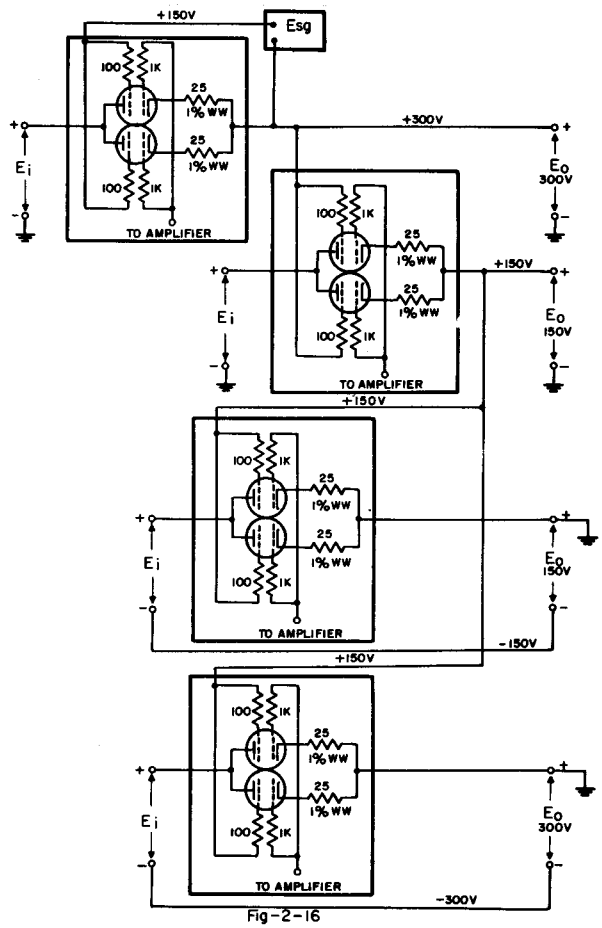


Fig-2-16

test and the maximum dissipation rating of this tube type allow use with nominal derating.

The addition of a separate screen supply to a beam power series-regulator tube increases the degree of regulation (reduction in output voltage variation) by virtue of the fact that the plate current of a pentode is much more dependent on screen voltage than on plate voltage. The screen voltage is smaller than the input voltage; therefore, a given change in line voltage results in less change in screen-cathode voltage than in plate-cathode voltage, even if the screen voltage is unregulated. Since screen-cathode voltage is reduced less than plate-cathode voltage as line voltage decreases, minimum static plate resistance will be lower for pentode than for triode connection. Thus, the pentode connection of a beam power tube provides an effective increase in amplification factor and a decreased minimum static resistance, thereby increasing series-tube efficiency and lowering the requirements of the regulator amplifier.

The increased effective gain of the pentode-connected beam power tube allows an amplifier using two direct-connected stages to be used in a 150v, 0.1% regulated supply without the need of either dc step-down attenuators between stages, or a highly regulated auxiliary voltage. Such operation is not possible using a low-mu triode because the plate swing required to control the grid of a pentode-connected 6098 is one-quarter of that required for the control of a 6080 operating under the same line and load conditions.

Wire wound, 25Ω, 1% resistors are used for cathode equalizing in PC 4 and PC 5 because they are a standard value less than 33Ω for this type of resistor, and provide a means for checking. If the cathode of each tube is brought out to a test point such as a pin jack, an ordinary multimeter can be connected between the output voltage terminal and each jack to check balance. If a unit is operated under full load conditions and the line voltage is reduced to minimum, then all tubes showing subnormal current flow in the cathode should be discarded. If the line voltage is raised to the maximum, then all tubes drawing more than 10% greater than average current should be replaced.

Though the regulators are designed to be used as self-contained units, they may be used in combination to provide the four preferred voltages required for a given unit. Such operation requires but one separate screen supply, and a schematic of this connection is shown in figure 2-16.

3. RECEIVER VIDEO CIRCUITS

Video circuits are particularly amenable to circuit standardization. This conclusion is a result of consideration of the pulses to be amplified, the polarities, and the amount of amplification required. Table 3–1, a list of the parameters for several recent radars, shows how similar the pulse responses must be.

Although the CRT can be driven with either negative video at the cathode or positive video at the grid, the circuit is more efficient if the final video amplifier is biased near cutoff, delivering negative video. The cathode follower following the detector is more efficient when delivering positive video. With these considerations, the polarity at all points in the video chain is well established.

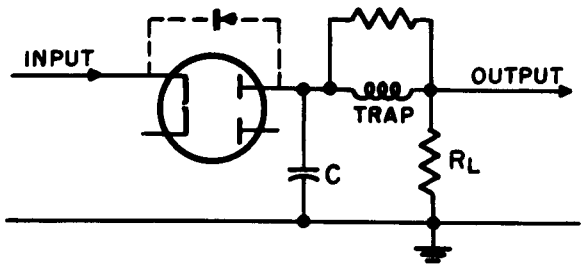
The similarity between the amounts of gain required result from more fundamental considerations. The CRT indicators require driving signals from 35 to 60v. The amplitude of the pulse at the video detector output must be in the order of 2v. The action of the limiter and cathode follower maintains the level between 1 and 2v into the second half of the video chain. The over-all gain is therefore about 30. The gain of the second half, however, must be sufficient to accommodate variations in tubes, components, and operating conditions.

3.1 *Examples of Receiver Video Circuits in Current Use:* Several radars have been examined to show current practice in the design of video amplifiers. A diode detector with negative output polarity is generally used to operate the limiter amplifier which inverts the signal polarity. A low-level cathode follower provides a positive output signal.

Examples of detector, limiter, and cathode follower stages taken from eight pulse radars are tabulated in table 3–2 and figure 3–1. The tabulation of i-f and pulse information in table 3–1 shows most of the pulse data which are pertinent in the design of the video chain.

TABLE 3–1—*Intermediate Frequency and Pulse Performance Characteristics*

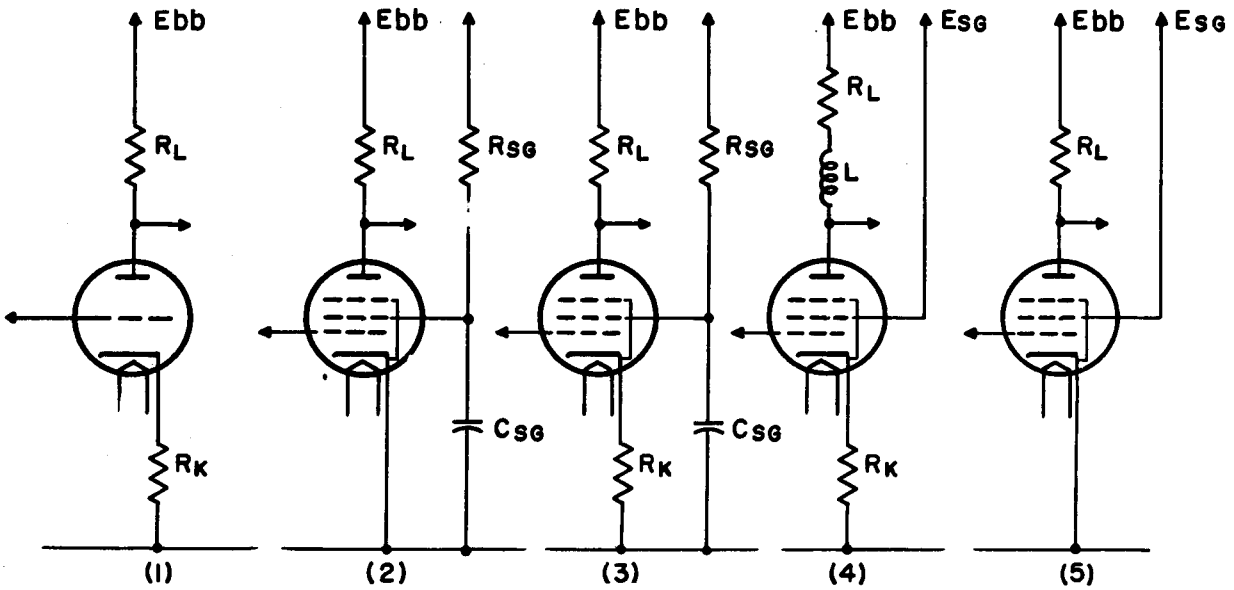
Key	Center frequency mcps	I-f or video bandwidth	Pulse width μsec	Video characteristics
A	60	30cps–3mc	0.5.	
B	30 ± .25 Beacon 30	0.8mc 6mc	0.67. 2.0.	0.5—100μsec pulses. Rise 0.25μsec, droop 1 db.
C	30	6mc	0.5.	
D	60 ± 1.25	30cps–4mc 5 ± 1mc 3 db 1mc	0.5. 2.25. 4.5.	30cps–4mc 1 db. Indicator 20cps–5mc, 3 db.
E	30	6mc	0.5. 1.75. 2.25.	
F	60	200cps–3mc 1.5 db	0.75. 2.25. 5.00.	Rise 0.08μsec. Droop 1 db 2500μsec.
G	30	750kc 6mc 4mc	0.5. 0.7. 2.35. 3.2.	Beacon 200cps–3mc 3 db. Wide Band 30cps–3.2mc, 3 db. Rise 0.15μsec. Droop 1 db 1000μsec.
H	30	1.2mc	1.8	Rise time 0.1μsec, droop 3 db 300μsec pulse.



Tubes and Parts

Key	Tube	$R_L(\Omega)$	C in $\mu\mu f$	L
A	1/2 6AL5	3.3K+4.7K	5	Not used.
B	6AK5	Plate detection	Not drawn	Not used.
C	1/2 6AL5	2K	22	6mc.
D	1/2 6AL5	1.8K	10	Not used.
E	1/2 6AL5	2.7K	10	30mc.
F	1N70	3K	10	Not used.
G	5702	5.6K	10	30mc.
	5702	3.3K	10	Not used.
H	6AL5	6.8K	22	Not used.

Figure 3-1—Video Detector



Tubes and Parts

Key	Circuit	Tube	Voltage	$RL(\Omega)$	R_k	$R_{sg}-E_{sg}$	C_{sg}
A	(2)	6AK5	+105v	6.8K		18K	0.001μf.
B	(4)	6AK5	+140v	470Ω+(10K)	220Ω	+140v	715$\mu\mu$f 10.5μh.
C	(1)	1/2 12AT7	+150v	1K	22Ω		
D	(2)	6AK5	+150v	1.2K		68K	0.1-0.1μf.
E	(2)	6AK6	+150v (has diode limiter).	1.2K		11.6K	0.101μf.
F	(3)	First video combined with cathode follower (fig. 3-3, F)					
G	(4)	5702	+110v	1.5K	220Ω	+110v	0.1-0.1μf.
H	(5)	6AK5	+105v	1K		+105v	

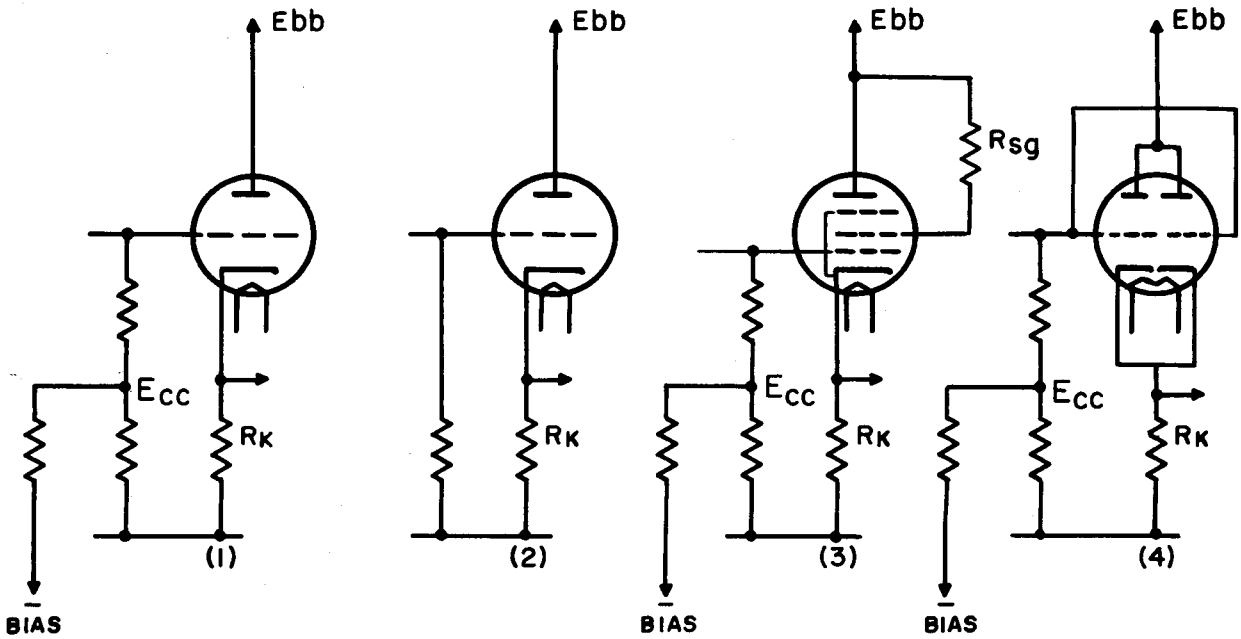
Figure3-2—Video Amplifier-Limiter

(*a*) Detector: The tabulation of the various detectors suggests that this stage shows only a small deviation in part values and a suitable preferred circuit can be developed. Although not listed, switching provisions for fast time constant (FTC) and beacon reception are commonly used. Seven of the eight radars use diode detectors, 5 using 1/2 6AL5; 1, a subminiature diode; and 1, a crystal diode. One radar uses a 6AK5 plate detector. The range of load resistors is from 2 to 5.6KΩ. The i-f capacitor ranges from 5 to 22$\mu\mu$f. Most circuits employ an i-f trap.

(*b*) Amplifier-Limiter: The video amplifier, immediately following the detector, takes several forms in the eight radars. There are five circuit variations for this stage as shown in figure 3-2.

(1) Triode, self-bias.
(2) Pentode, zero-bias, screen resistor.
(3) Pentode, self-bias, screen resistor.
(4) Pentode, self-bias, fixed screen.
(5) Pentode, zero-bias, fixed screen.

Some of the stages are limiters and others are regular amplifiers. Of the seven radars, six use pentodes and one uses a triode. The load resistor varies from 470Ω to 6.8KΩ. The plate voltage varies from 105 to 150v. Only one amplifier uses a peaking coil. This basic amplifier-limiter function lends itself to standardization. The



Tubes and Parts

Key	Circuit	Tube	E_{bb}	R_{sg}	R_k (Ω)	E_{cc}
A	(3)	6AK5	+105	100Ω		−15v
B		See video limiter				
C	(2)	½ 12AT7	+150		750 (parallel 10K)	
D	(4)	6J6	+150		100	−4v.
E	(4)	12AU7	+150		510	−5v.
F	(3)	6AK5	+105	E_{sg} 24v	430 (parallel 10K)	
		Combined with limiter				
G	(1)	5977	+110		150	−4.7v.
H	(2)	½ 12AT7	−105		330 (parallel 10K)	

Figure 3-3—Cathode Follower

characteristics which need greatest care are the linearity of amplification and constancy of limiting level with high duty-cycle signals. As mentioned in the case of the detector, switching provisions for FTC and beacon reception are connected at the limiter input. A dc restorer diode is used in three limiter circuits.

(*c*) Cathode Follower: Of the eight radars examined two used pentode cathode followers, and five used triode cathode followers singly or in duo-sections. These circuits are shown in figure 3–3. One radar did not use a cathode follower. Of the seven cathode follower stages, four used an external bias. The plate voltage ranged form 105 to 150v.

3.2 *Summary of Types in Current Use:* The first half of the video amplifier chain generally uses the pattern of detector, amplifier-limiter, and cathode follower. Of the three stages, the cathode follower appears most suited for a preferred circuit. The signal path is similar for all examples. A negative output pulse from the detector is inverted by the amplifier-limiter to provide a positive pulse to the cathode follower whose output is also positive.

TABLE 3–2—*Video Amplifier Tube Line-up*

Key	Detector	Video limiter	Cathode follower
A	1/2 6AL5	6AK5	6AK5.
B	6AK5 (plate detector)	No limiter	No follower.
C	1/2 6AL5	1/2 12AT7	1/2 12AT7.
D	1/2 6AL5	6AK5	6J6 (duo).
E	1/2 6AL5	6AK5	12AU7 (duo).
F	1N70	6AK5	Limiter-follower.
G	5674	5702	5977.
H	1/2 6AL5	6AK5	1/2 12AT7.

The detector circuits all use a diode detector. The amplifier-limiter and cathode follower, in contrast, have many variations. The amplifier-limiter tubes are predominantly pentodes, but there are a variety of circuit configurations. The cathode follower tube selections are predominantly triodes used singly or in duo-section. The type of biasing is evenly divided between self and fixed bias. The range of plate supply voltage for the chain is from 105 to 150v.

4. VIDEO MIXERS

Video mixing is the combining of various forms of pulse information. In a radar system, video mixing may include any number of the following: radar video, beacon, range markers, range strobe, azimuth markers, and other special forms of information. The term "video mixer" should not be confused with the intermodulating function that occurs at the mixing of radio frequency and local oscillator signals in a receiver.

In the strict sense of the word, video mixers should be considered as adding elements. This implies that the circuit will perform an algebraic addition of pulses of either polarity that are in or out of coincidence. In radar applications, however, video mixers are chosen to combine time coincidence pulses in a nonadditive manner in order to prevent distortion at the indicator. Certain video mixers will combine signals of only a chosen polarity.

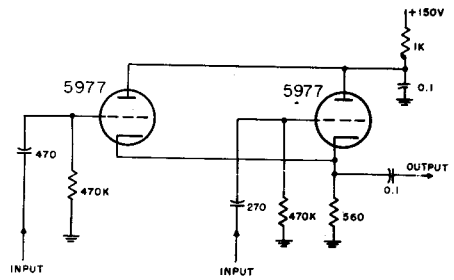
4.1 *Examples of Video Mixers in Current Use:* The following is a summary of various video mixers found in radar systems in the course of the survey. The circuits are shown in figure 4–1, (a) through (v).

VM–1 A common-cathode video mixer combining range markers and heading markers.

VM–2 Two separate common-cathode video mixers, the same heading markers being inserted in both mixers. The other inputs handle independent markers.

VM–3 A circuit combining four inputs into a common cathode. All four inputs are marker pulses of a positive polarity.

VM–4 A common-cathode video mixer combining three markers.



(a) VM-1

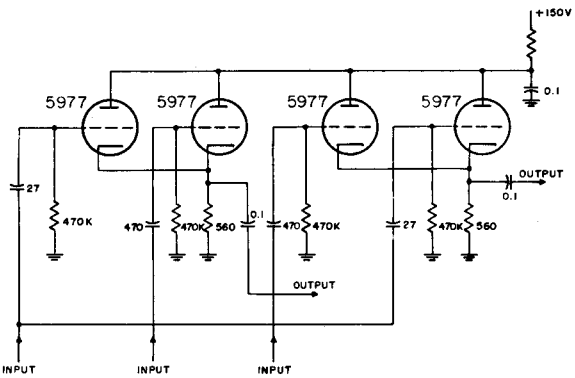
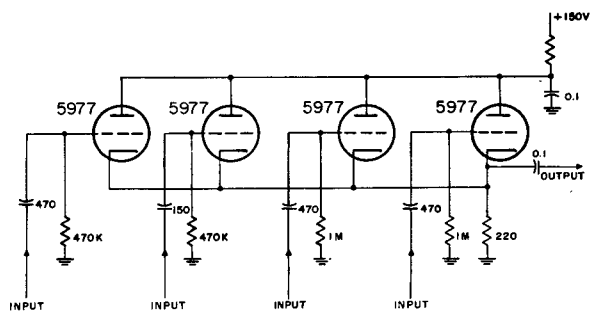


Fig. 4-1 (b) VM-2



(c) VM 3

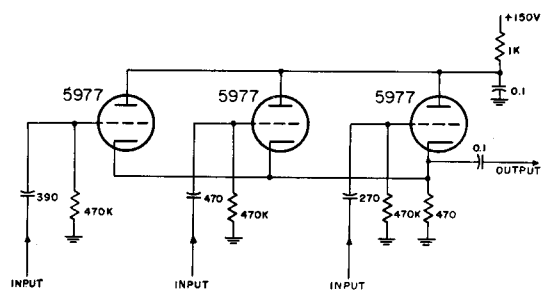
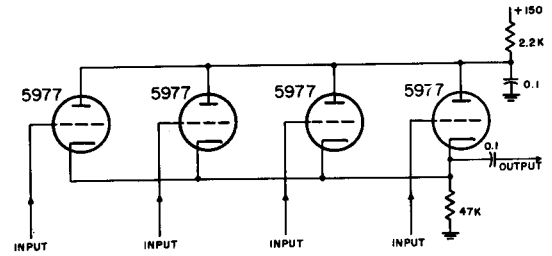


Fig. 4-1 (d) VM 4



(e) VM-5

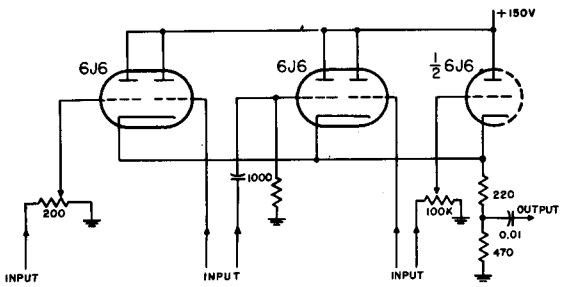


Fig. 4-1 (f) VM-6

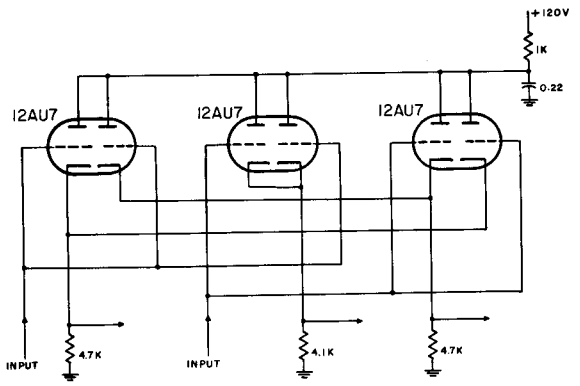
VM-5 A common-cathode video mixer combining four trigger pulses of positive polarity. The large cathode resisitor, (47KΩ), was chosen to allow nonadditive mixing of high amplitude pulses in the vicinity of 50v.

VM-6 A common-cathode video mixer combining five marker inputs.

VM-7 A triple common-cathode video mixer combining three inputs and providing three independent outputs for separate indicators.

VM-8 A common-cathode video mixer combining three inputs. Each of the grids is biased to cutoff and therefore passes only positive polarity pulses of sufficient amplitude to overcome the bias.

VM-9 A common-cathode video mixer for combining two positive polarity range strobe triggers.



(g) VM-7

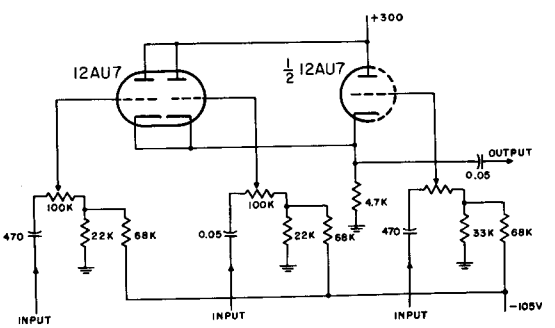
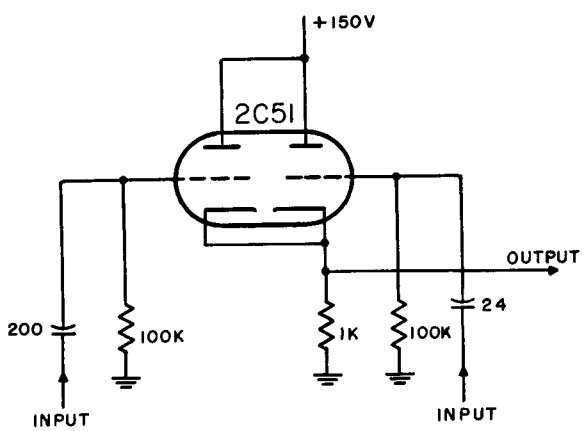


Fig. 4-1 (h) VM-8



(i) VM-9

VM-10 A common-cathode video mixer combining 9v positive polarity markers with 2 to 10v positive IFF signals.

VM-11 A common-cathode video mixer combining positive polarity range strobe and IFF signals. Output is approximately 8v positive.

VM-12 A common-plate video mixer consisting of three pentodes. Both positive and negative signals are combined. High frequency compensation is used in the plate circuit. A triode is used as a phase splitter.

VM-13 A two pentode common-plate video mixer combining radar video and IFF video. The polarity is positive at the grids. Each grid also has a diode clamp establishing the base line at −1.8v.

VM-14 A two pentode common-plate video mixer combining gated video and beacon video.

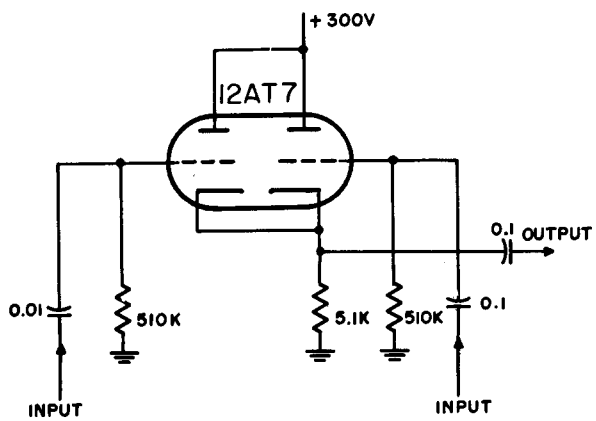
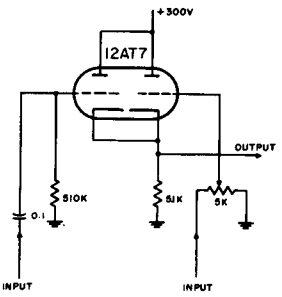


Fig. 4-1 (j) VM-10



(k) VM-11

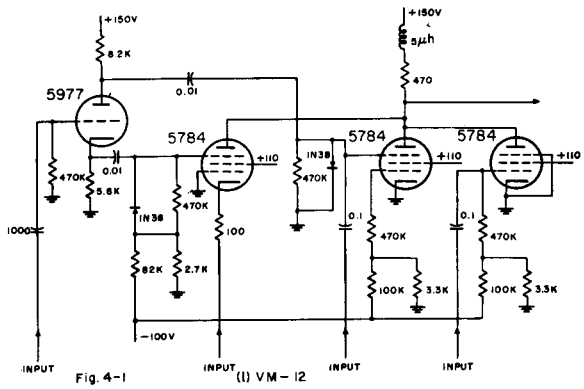
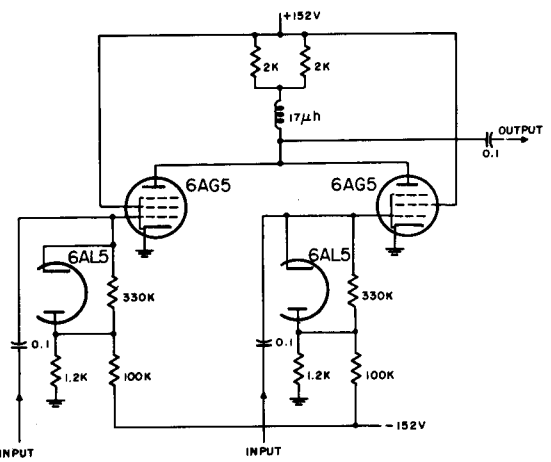


Fig. 4-1 (l) VM-12



(m) VM-13

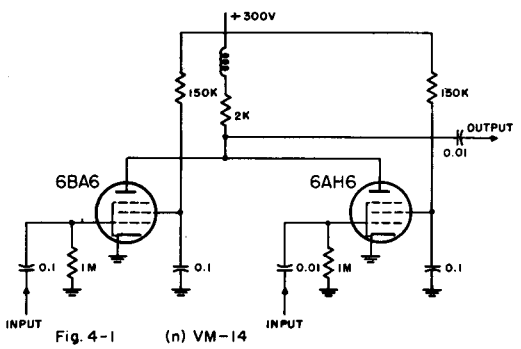


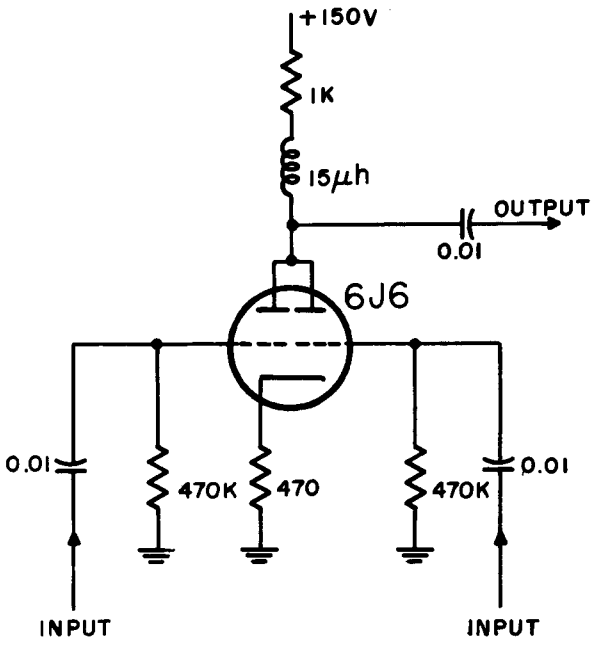
Fig. 4-1 (n) VM-14

VM-15 A common-plate video mixer using triodes for mixing high level blanking pulses. In series with the plate load of the mixer triodes is a third triode for mixing an additional blanking pulse.

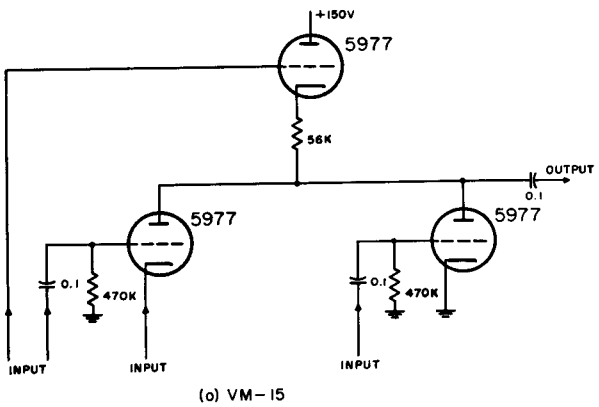
VM-16 A three triode common-plate video mixer for combining three IFF signals. The common-cathode resistor provides some degeneration.

VM-17 A common-plate video mixer for combining radar video and mixer markers. A compensated plate load is used.

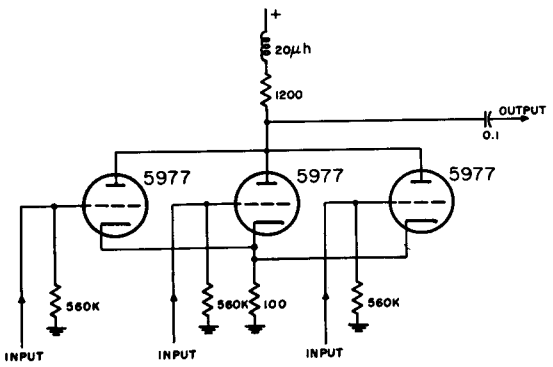
VM-18 A common-plate video mixer using a dual triode, combining radar video and mixed markers. Each cathode has its own unbypassed resistor for gain stabilization.



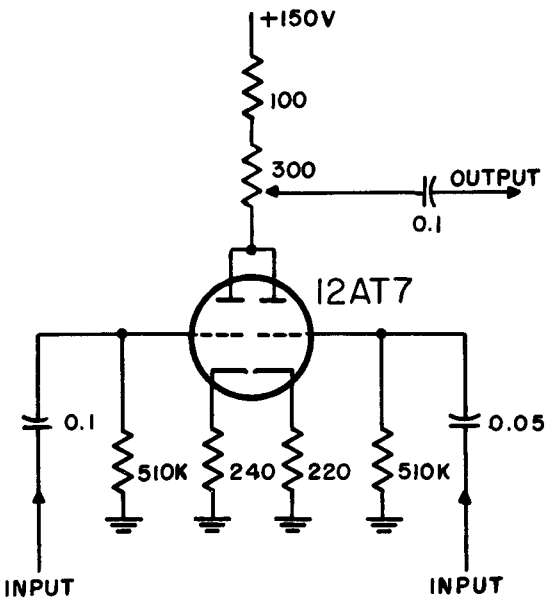
(q) VM-17



(o) VM-15



(p) VM-16



(r) VM-18

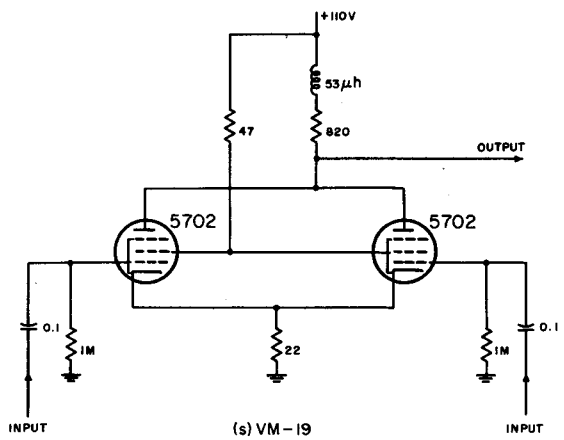
Fig. 4-1

VM-19 A common-plate video mixer for combining radar video and range markers. Two pentodes are used with a compensated load for high frequency response.

VM-20 A common-plate video mixer using special tubes with sharp cutoff characteristic at each grid. At one tube, IFF and markers are inserted at separate grids. Radar video is impressed at one grid of the other tube.

VM-21 A single pentode video mixer, negative video plus IFF being inserted at grid. Impressed at the cathode is the range strobe derived from the cathode output of a blocking oscillator.

VM-22 A common-plate video mixer using a diode to couple the two plates. The function of the diode is to provide a nonadditive feature. Note that the plate with the +115v potential is connected to the "cathode" of the diode and the other plate with a +110v potential is connected to the "anode" of the diode, thus rendering the diode nonconducting. Both grids are impressed with negative-going pulses. Under conditions of noncoincidence, a negative pulse of sufficient amplitude at either grid will appear at the output. The positive pulse appearing at the plate of section B will not conduct through the diode because of the positive pulse at the opposite side of the diode. The video pulse must be applied to the input A. The input at B has to overcome a 5v bias at the diode.



(s) VM-19

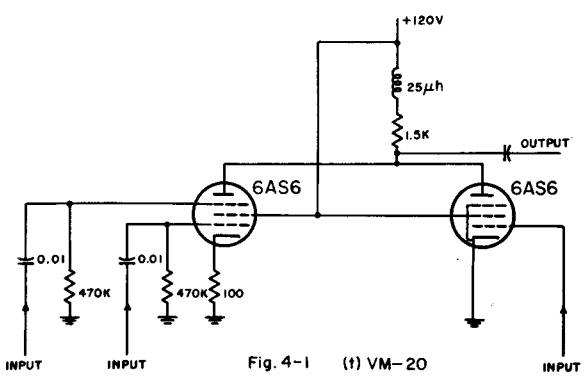
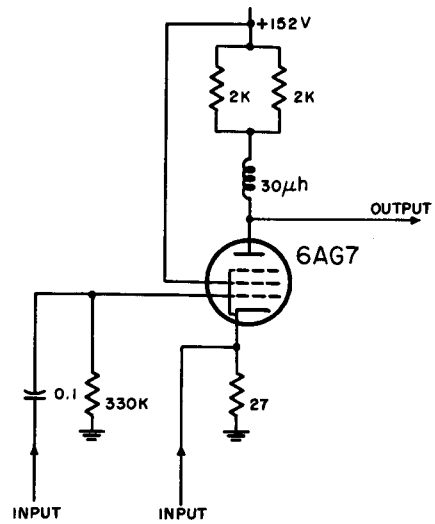


Fig. 4-1 (t) VM-20



(u) VM-21

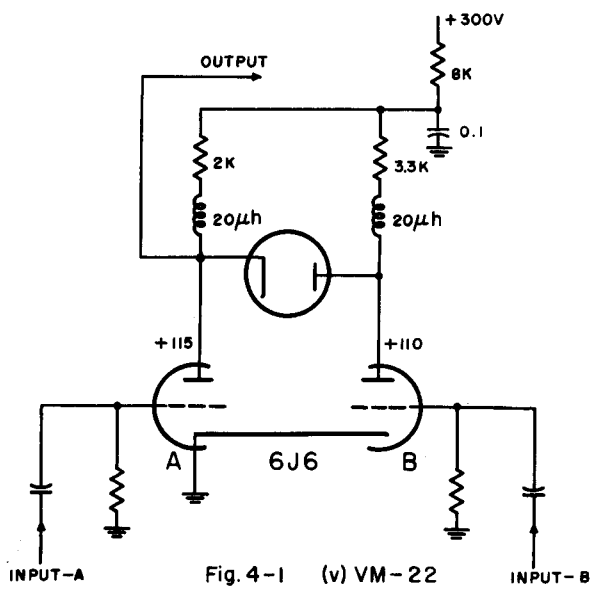


Fig. 4-1 (v) VM-22

4.2 *Analysis of Types in Current Use:* The 22 examples of video mixers that have been described briefly were taken from radar systems of various functional designs. The pulse widths cover a range of 0.5 to 5μsec, and repetition rates from 200 to 2000pps. The common-plate mixers have high-frequency compensation commensurable with the rise time of the video pulses. The common-cathode mixers by virtue of cathode-follower action are capable of handling very fast rise times. From this survey it appears that most video mixer requirements can be met with only two types of circuits — the common-plate and the common-cathode. The choice between the two is based only on the necessity for phase inversion. Low-level mixing is used purely for efficiency considerations.

4.3 *Additional Design and Performance Data for the Common-cathode Video Mixer:* Preferred Circuit 23 was developed as the preferred common-cathode video mixer. This circuit and its accompanying technical data deal with the 5670 tube. This tube was chosen on the basis of circuit performance and reliability. For purposes of comparison, however, other types of miniature twin-triodes were evaluated: namely 12AU7, 12AT7, 12AX7, and 12AY7. Tubes of these types were selected from the "reliable" series.

Tables 4–1 through 4–4 give performance data of the various twin-triodes when used as common-cathode video mixer. The voltage levels of inputs 1 and 2 were chosen to produce identical output levels. Any discrepancy between the input levels can be attributed either to tube unbalance or the effects produced by unequal duty cycle. The additive factor was determined by applying a positive 180μsec pulse to input 1 and a positive 10μsec pulse, input 2, that was varied in time coincidence with the first. In general there are only small differences in the circuit performance of the various twin-triodes. This is probably due to the inherent degenerative action of this mixer.

4.4 *Additional Design and Performance Data for the Common-plate Video Mixer:* Preferred Circuit 24 was developed as the preferred common-plate video mixer. Other types of tubes for use as common plate-mixers were investigated along with the

TABLE 4–1—*Video Mixer, Common Cathode Type 12AU7*

E_{bb} = +150v

Output (for either input), volts	Output (for inputs in coincidence), volts	Input 1, volts	Input 2, volts
Cathode Resistor—4700Ω			
0.20	0.38	0.43	0.46
1.0	1.6	1.9	1.9
3.0	4.1	5.5	5.0
10.0	12.0	14.0	14.0
Cathode Resistor—470Ω			
0.20	0.39	0.58	0.60
1.0	1.7	2.8	2.8
3.0	4.5	7.1	7.3
5.0	7.0	12.0	10.0
Cathode Resistor—150Ω			
0.20	0.38	0.81	0.80
1.0	1.7	4.0	3.9
3.0	5.0	31.0	9.0

TABLE 4–2—*Video Mixer, Common Cathode Type 12AT7*

E_{bb} = +150v

Output (for either input), volts	Output (for inputs in coincidence), volts	Input 1, volts	Input 2, volts
Cathode Resistor—4700Ω			
0.20	0.36	0.45	0.39
1.0	1.4	1.6	1.5
3.0	3.5	4.3	4.0
10.0	11.0	12.0	12.0
Cathode Resistor—470Ω			
0.20	0.38	0.56	0.53
1.0	1.6	1.9	1.9
3.0	3.7	5.5	4.5
5.0	6.0	22.0	7.0
Cathode Resistor—150Ω			
0.20	0.38	0.65	0.60
1.0	1.5	3.4	2.4

TABLE 4-3—*Video Mixer, Common Cathode Type 12AX7*

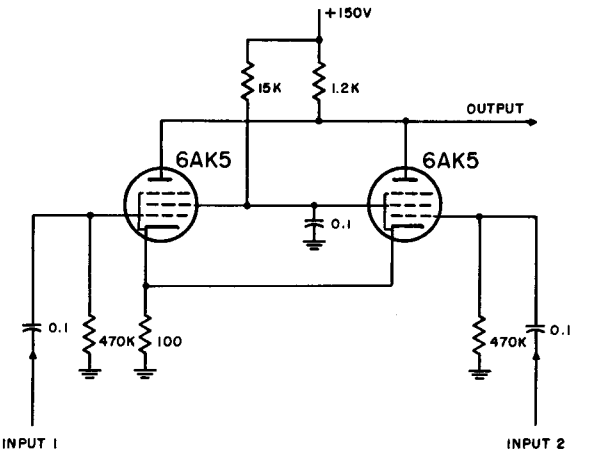
E_{bb} = +150v

Output (for either input), volts	Output (for inputs in coincidence), volts	Input 1, volts	Input 2, volts
Cathode Resistor—4700Ω			
0.20	0.33	0.39	0.35
1.0	1.2	1.5	1.4
3.0	3.4	3.9	3.7
10.0	11.0	13.0	12.0
Cathode Resistor—470Ω			
0.20	0.36	0.61	0.62
1.0	1.5	5.4	2.2
Cathode Resistor—150Ω			
0.20	0.18	0.91	0.92
0.50	0.80	12.0	2.2

TABLE 4-4—*Video Mixer, Common Cathode Type 12AY7*

E_{bb} = +150v

Output (for either input), volts	Output (for inputs in coincidence), volts	Input 1, volts	Input 2, volts
Cathode Resistor—4700Ω			
0.20	0.36	0.40	0.41
1.0	1.4	1.7	1.6
3.0	3.6	4.1	3.9
10.0	11.0	14.0	13.0
Cathode Resistor—470Ω			
0.20	0.38	0.57	0.56
1.0	1.6	2.4	2.2
3.0	4.7	18.0	5.4
Cathode Resistor—150Ω			
0.20	0.39	0.90	0.90
1.0	1.6	10.0	3.3



Output (for either input), volts	Output (for inputs in coincidence), volts	Input 1, 180μsec, volts	Input 2, 10μsec, volts
−1	−1.8	+0.55	+0.32
−2	−3.7	+1.0	+0.68
−4	−5.6	+2.0	+1.4
−8	−13.0	+3.6	+2.6
−10	−17.0	+5.5	+2.9
+1	+2.2	−0.65	−0.41
+2	+4.5	−1.5	−0.8
+3	+7.5	−5.0	−1.3
+4	+11.0	−9.0	−2.4
+5			

Figure 4-2—Common Plate Mixer (Pentode)

5670 employed in PC 24. These included 6AK5 pentodes and the 12AU7 dual triode.

Figure 4-2 is a common-plate mixer using 6AK5 pentodes. The table beneath the schematic diagram shows the additive factor at the plate as a result of two coincident inputs. This circuit is a good adder. If the application demands a low additive factor, it will be necessary to use accompanying circuitry to nullify the adding effect. There is little advantage in using pentodes rather than triodes. On the contrary, the single-envelope dual triode has a definite appeal over two separate pentodes from the viewpoint of saving components. The inherently low Miller effect associated with pentodes is counterbalanced by the fact that the triodes are used in a unity-gain circuit. Therefore pentodes offer no significant reduction in input capacity. Another disadvantage of the pentodes is the problem of the screen bypassing

capacitor. Unless a large capacitor is used, there is always the adverse droop characteristic associated with rectangular pulses. A time constant of 25,000μsec is required to keep the droop of a 500μsec pulse at 2%. The operating range and linearity of the plate mixer using 6AK5 pentodes

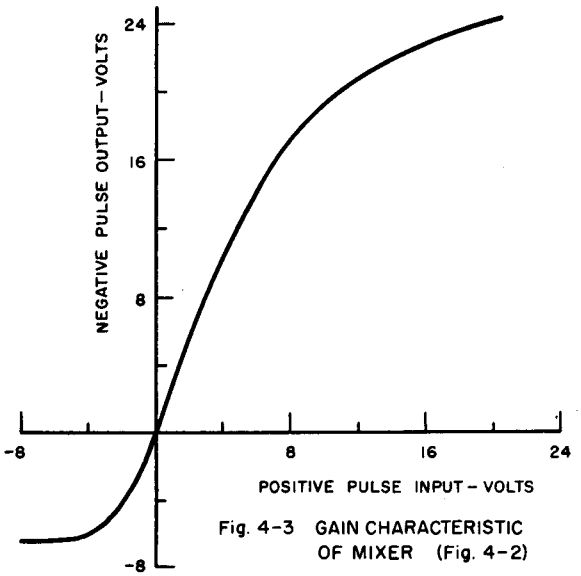
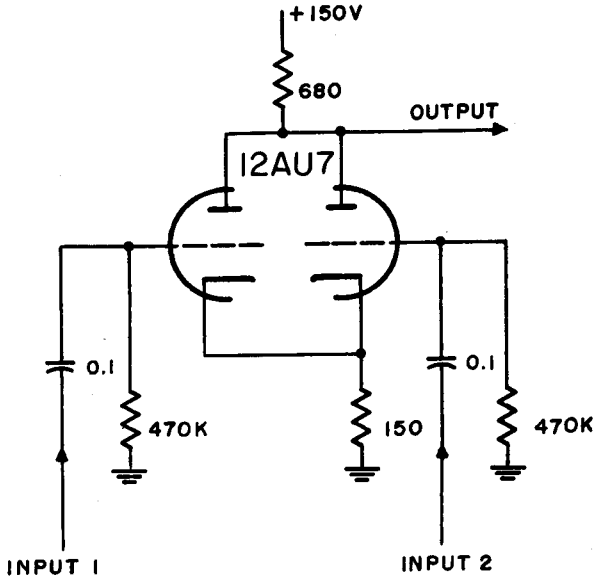


Fig. 4-3 GAIN CHARACTERISTIC OF MIXER (Fig. 4-2)

are given in figure 4-3. Even under conditions of high current drain, the plate potential remains close to the supply potential due to the low value of load resistance. Therefore the circuit is best operated with positive input pulses and a negative-going output.

For purpose of comparison the 12AU7 tube was also tested in a common-plate mixer circuit. The plate-load and cathode resistors were selected to produce a gain characteristic similar to that of PC 24. The results are tabulated in figure 4-4. The 12AU7 circuit draws twice the plate current of the 2C51 circuit. The plate current could be reduced by increasing the cathode resistance, but the plate resistor would then have to be increased correspondingly in order to keep the gain at the same figure. This increase in plate resistance would adversely affect pulse rise time and necessitate high-frequency compensation.

As pointed out previously, common-plate mixers will combine signals that are coincident in time in a good additive manner. If this effect is detrimental to the operation of associated circuits,

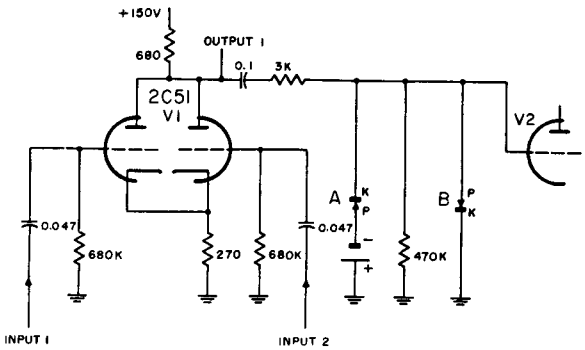


Output (for either input), volts	Output (for inputs in coincidence), volts	Input 1, 180μsec, volts	Input 2, 10μsec, volts
−0.5	−1.0	+0.62	+0.49
−1	−1.9	+1.1	+1.0
−2	−3.8	+2.2	+2.2
−4	−7.5	+4.6	+4.6
−8	−14.0	+11.3	+7.5
+0.5	+0.9	−0.7	−0.7
+1	+2.1	−1.2	−1.3
+2	+4.5	−2.6	−2.7
+3	+7.3	−4.5	−5.0
+4			

Figure 4-4—Common Plate Mixer (Triode)

it will be necessary to employ techniques to nullify the adding feature. Figure 4-5 shows a common-plate mixer with a diode-limiting coupling circuit. Operational data are included in the figure. The data illustrate how the bias voltage sets the limiting level.

The circuit shown in figure 4-6 is a system whereby a common-plate mixer can be arranged to provide a lower additive factor. A diode is inserted between the plates whose quiescent operating potentials are staggered by the unequal plate-load resistors. The diode polarity is arranged in a nonconducting direction with approximately 1.5v back voltage to be overcome before



Input 1, volts	Output 1, volts	Input 2, volts
Bias Voltage—1.5v		
+3	−3	−1.1
+9	−10	−2.2
+23	−23	−2.7
Bias Voltage—3.0v		
+3	−3	−1.8
+9	−11	−3.7
+24	−24	−4.1

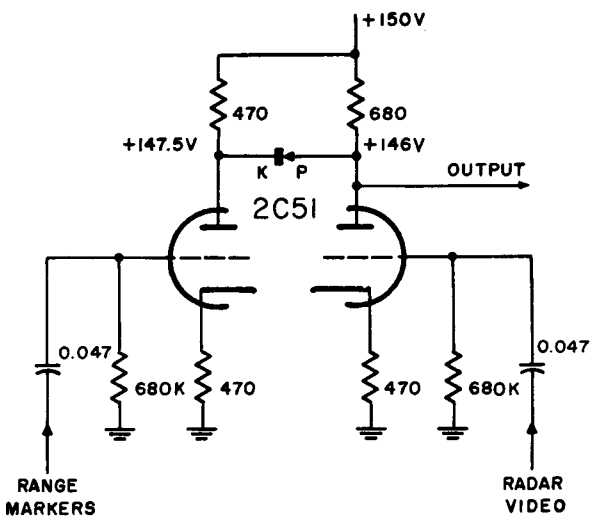
Rise time = 0.05μsec. The 3KΩ resistor can be shunted with a few micromicrofarads to speed up the leading edges.

Diode B needed with fast repetition rates or high duty cycles in order to limit the positive excursions.

Figure 4–5—Mixer-Limiter

conduction can occur. In this circuit it is imperative that the radar video be applied to section B. The input to section A has to be of sufficient amplitude to overcome the diode back-bias before the signal can appear at the output. Therefore, if this were radar video, small echoes would be lost in the output. Positive radar video applied at the input of section B appears as a negative output at the plate. Positive marker pulses applied to the input of section A will, if given a sufficient level, pass through the diode to the output. Whenever the radar video is coincident in time with a marker pulse, the radar video biases the diode to the extent that only a small amount of marker pulse can pass through the diode and add to the radar video.

While studying operation of common-plate mixers, a possible source of signal deterioration was uncovered. A circuit of this sort can behave as



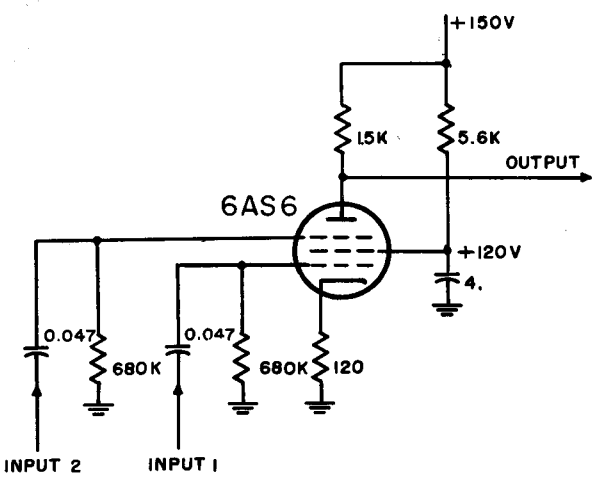
Marker input, volts	Video input, volts	Marker out, volts	Video out volts	Both in coincidence, volts
+8.6	+1.0	−2	−1	−2.5
+15	+1.0	−3	−1	−3.4
+8.7	+2.2	−2	−2	−3.8
+15	+2.2	−3	−2	−4.6

Figure 4–6—Diode Connected Mixer

if the plate load were shunted by a resistance and capacitance in series. This condition can result from too small a value of capacitor at one of the inputs if one of the inputs is left unconnected. The deterioration of rectangular pulses due to this condition simulates the effect of shunting the plate load with a capacitance and resistance in series.

Two basic rules should be practiced in order to avoid the described situation. All grid inputs should be connected to their signal sources and not left isolated, as might be the case in a relay switched system. Grid input coupling capacitors should have a value not only large enough to satisfy the pulse duration requirement but also large enough to avoid the above effect. For example, a coupling capacitor of 500μμf and 0.5MΩ grid resistor would satisfy pulse width considerations for a 10μsec pulse (4% droop). A safe value to use, however, would be 0.047μf.

The circuit shown in figure 4–7 is a special case of plate mixer. A 6AS6, dual control pentode with a suppressor grid having a cutoff characteristic



Input 1, volts	Input 2, volts	Output for Input 1, volts	Output for Input 2, volts	Output for both inputs in coincidence, volts
−1	−2	+2	+2.0	+3.4
−1	−3	+2	+3.4	+4.3
−1	−4	+2	+4.6	+5.5
−2	−2	+5	+2.2	+5.8
−2	−3	+5	+3.5	+6.5
−2	−4	+5	+5.0	+6.7
−2	−6	+5	+7.9	+8.1

Figure 4–7—Dual Grid Mixer

similar to the control grid, is employed. Pulses of higher amplitude such as markers should be impressed on the suppressor grid since its transconductance is about one-fourth that of the control grid. A table of operating levels is included in figure 4–7. One drawback of the circuit is the high-value, bulky capacitor needed to bypass the screen grid.

5. PRF GENERATORS

A survey of repetition rate generators used in current airborne radar equipments shows little correlation between the specified frequency stability and the circuit type. Multivibrators, blocking oscillators, and Wien bridge oscillators, for example, have all been used in equipments in which a 3% frequency stability was specified. As a repetition rate generator, the multivibrator has the advantage of greater frequency stability than the blocking oscillator and greater economy of components than the Wien bridge oscillator. A disadvantage of the multivibrator is that the output impedance is essentially equal to the plate load resistance. This resistance must be relatively high for good frequency stability.

5.1 *Examples of Multivibrators in Current Use:* The diagrams show repetition rate generators taken from three equipments in which multivibrators are used to generate the repetition frequency. As these three equipments were all engineered by the same organization, there is a noticeable similarity in the design of these circuits.

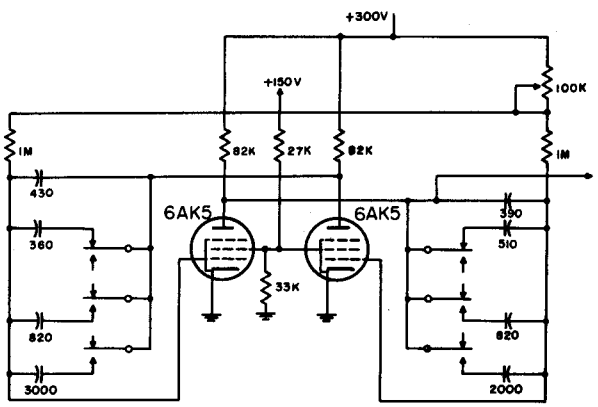


Fig. 5-1 MULTIVIBRATOR PRF GENERATOR

The specifications for the equipment from which the circuit of figure 5-1 was taken require a 3% frequency stability for the 200pps repetition frequency, and 8% stability for the 400 and 800pps frequencies. No information is given in the specifications on the frequency stability required from the circuit of figure 5-2. The circuit shown in figure 5-3 is from an experimental version of a radar set for which a frequency stability of 3% was specified. In this version, the multivibrator could be either free-running or triggered, but only the free-running connections are shown in the diagram.

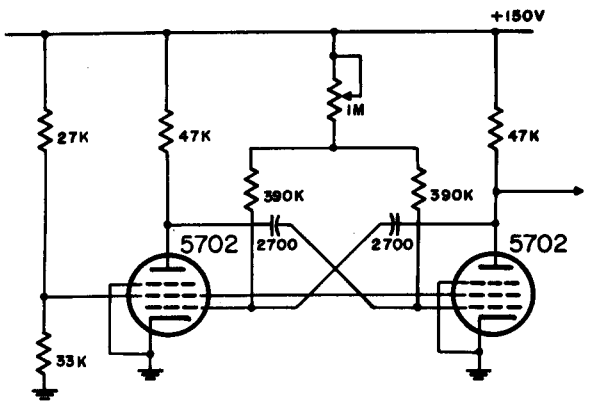


Fig. 5-2 MULTIVIBRATOR PRF GENERATOR

Although the frequency stability specified for the multivibrator of figure 5-1 is not greater than that required for the multivibrator of figure 5-3, the much larger plate resistors used in the circuit of figure 5-1 indicate that the frequency stability of this circuit, for the same quality of components, will be superior to the circuit of figure 5-3. In any case, the specified frequency stability could be obtained from a twin-triode multivibrator.

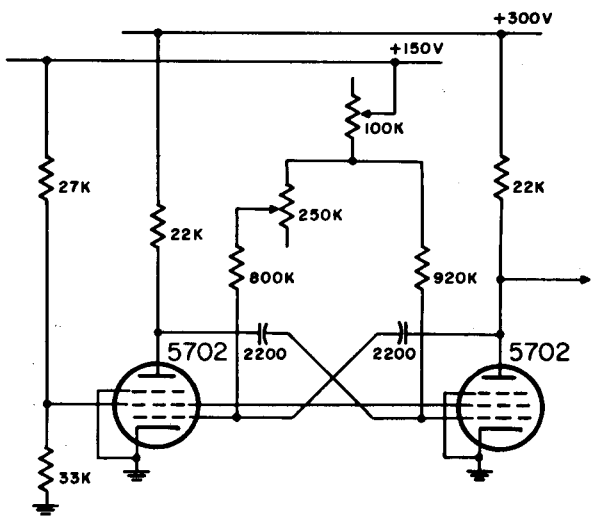
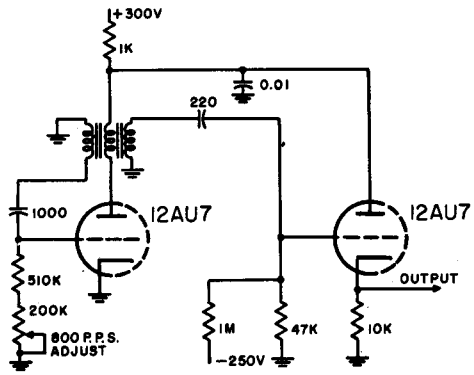


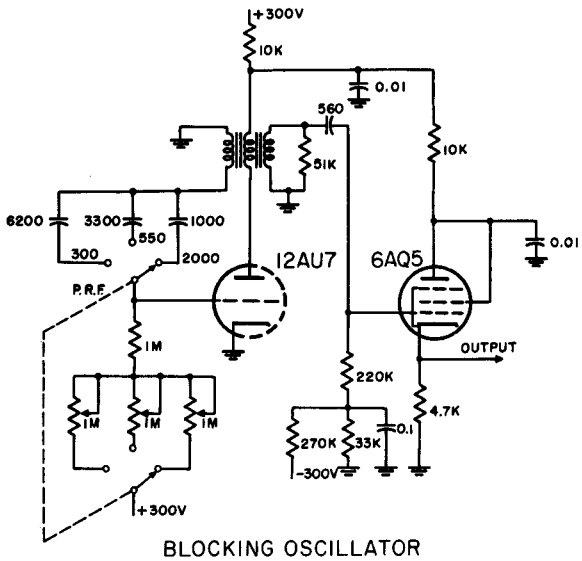
Fig. 5-3 MULTIVIBRATOR PRF GENERATOR. FREE RUNNING CONNECTION SHOWN

5.2 *Blocking Oscillator Examples:* Blocking oscillators have been used widely for PRF generators where the frequency stability requirements are about ±5%. Typical circuits taken from different radars are shown in figures 5–4, 5–5, and 5–6. All operate at frequencies between 200 and 2000pps as indicated on the diagrams.

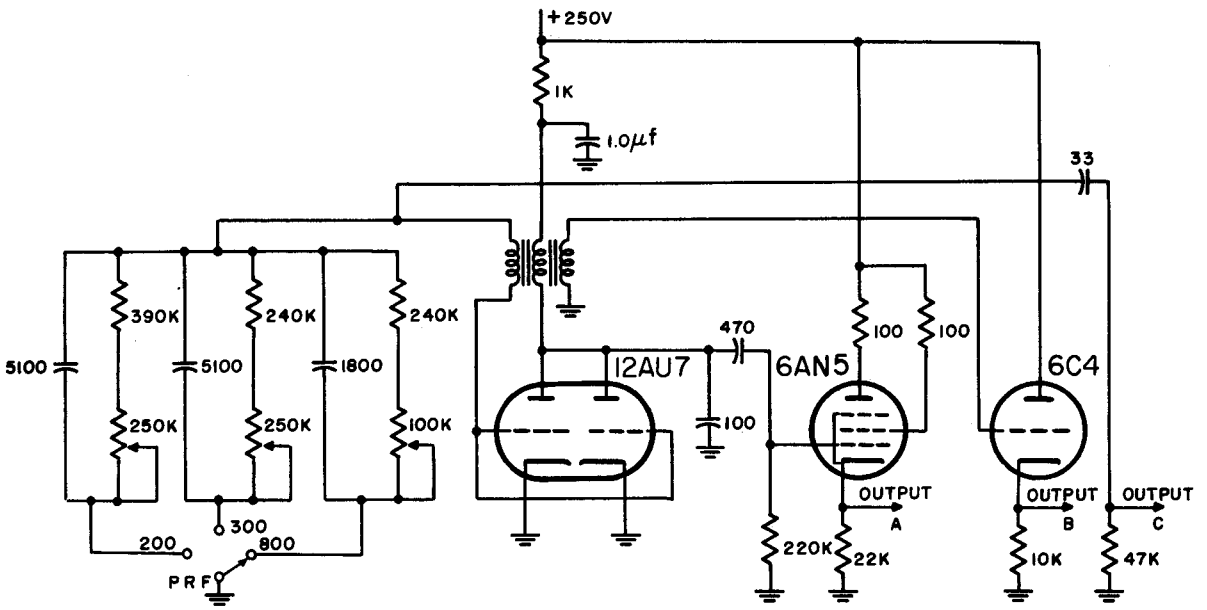


BLOCKING OSCILLATOR
P R F GENERATOR
FIG. 5-4

The positive grid return in figure 5–5 is the only major difference in the circuits except for component values. Returning the grid to the plate supply is likely to decrease the frequency stability if the filament voltage drops below its rated value.



BLOCKING OSCILLATOR
P R F GENERATOR
FIG. 5-5



BLOCKING OSCILLATOR
P R F GENERATOR

FIG. 5-6

Cathode follower outputs minimize the effects of the load on the blocking oscillator frequency. The one exception is output C of figure 5-6. Although the load at this point is across the principal frequency-determining element, its effect is negligible because of the low impedance of the source during the pulse and the low time constant of the load circuit compared to the frequency determining *RC* circuit. The output polarity here is negative. All the other outputs are positive, including output B of figure 5-6, where the desired signal is the positive overshoot to provide a trigger which is delayed with respect to outputs A and C by the width of the pulse. The 100$\mu\mu$f capacitor contributes to the delay and was probably added for that purpose.

5.3 *Additional Design and Performance Data:* A large number of variations of the basic blocking oscillator circuit were tested. The 12AT7, 12AY7, and 6AK5 were tried in addition to the 12AU7. The 12AU7 was selected on the basis of higher cathode emission and plate current ratings. The stability with the 12AY7 is slightly better, but it was rejected because its ratings are 50% lower than the 12AU7.

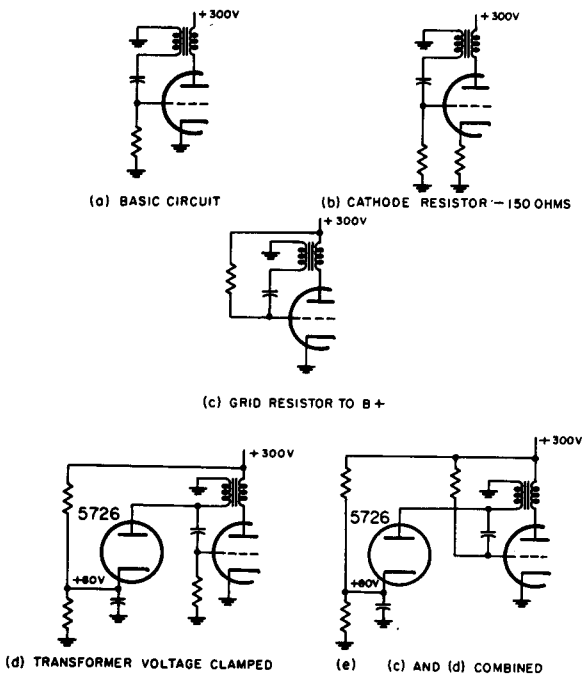


Fig. 5-7 BLOCKING OSCILLATOR P R F GENERATOR CIRCUITS TESTED FOR FREQUENCY STABILITY SIMPLIFIED SCHEMATICS TUBE TYPE - 5814 A

Using the 12AU7, several circuit configurations were tested for frequency stability versus supply voltage and tube changes (fig. 5-7).

The measurements of stability versus supply voltage change were made with twenty tubes covering the range of MIL specifications in transconductance and plate current. None of the circuits were sensitive to plate supply voltage changes or to increases in filament voltage. In the worst case, the frequency changed less than 2% for a 10% voltage change. Circuit performance deteriorates rapidly when the filament voltage drops below its rated value. For a 10% drop in filament voltage, the frequency change varied from ±2% in the case of circuit (b) to +12% in the case of circuit (c). The diode clamps in circuits (d) and (e) had little effect on performance at low filament voltages.

The effects of changing tubes without any adjustment in the circuit are shown in table 5-1, which summarizes the results with 13 tubes covering the range of MIL specifications. For comparison, a factor of merit is obtained by dividing the range over which the frequencies varied by the average frequency. In this case, the circuits with the clamping diodes gave the best results, but frequency adjustment is still required because of the 11% frequency change with change in tubes. The improvement in frequency stability did not justify the use of an extra cathode, and circuit (b) was selected for the preferred circuit on the basis of its performance at low filament voltages.

TABLE 5-1—*Effect of Tube Changes on PRF of Blocking Oscillator Circuits*

Circuit (Fig. 5-7)	Lowest frequency	Highest frequency	Average frequency	Range	Range/ Average f
	cps	cps	cps	cps	Percent
(a)	940	1075	990	135	13.6
(b)	949	1103	1002	154	15.4
(c)	975	1153	1044	178	17.0
(d)	957	1058	992	101	10.2
(e)	981	1091	1022	110	10.8

NOTE: Thirteen tubes representative of the range of MIL specifications were used in making these tests. The frequency of each circuit was adjusted to 1000cps with a tube near the center of the MIL range, after which no circuit adjustments were made.

6. TRIGGERED BLOCKING OSCILLATORS

Triggered blocking oscillators are used to produce high-amplitude pulses of current or voltage. They are often used for modulator triggers, multivibrator triggers, and pulse shapers.

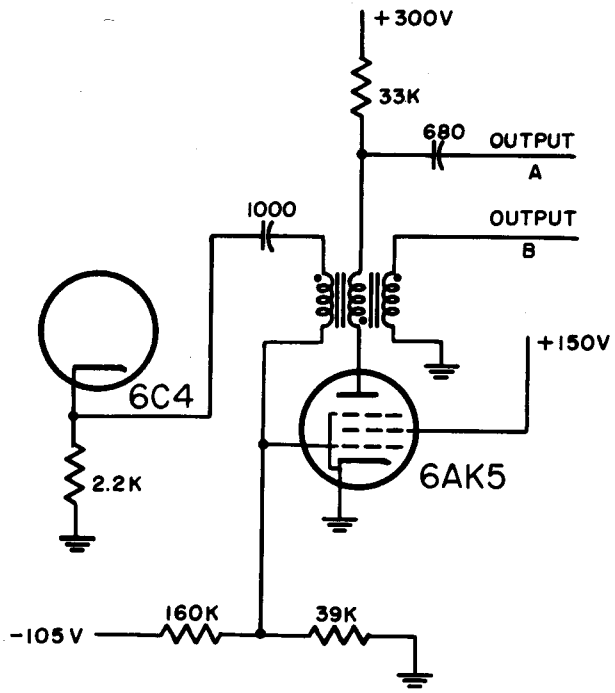
6.1 *Examples of Circuits in Current Use:* To determine the ranges of performance required for triggered blocking oscillators, 31 circuits were examined. The five examples shown in figures 6–1 through 6–5 represent the different configurations. Table 6–1 summarizes the characteristics of all 31 circuits. In the table the use has been designated "display" when the blocking oscillator output is presented as video information, and "trigger" when the function is one of shaping or triggering. In most cases the load impedance was estimated from the circuit diagram.

(*a*) Bias methods:

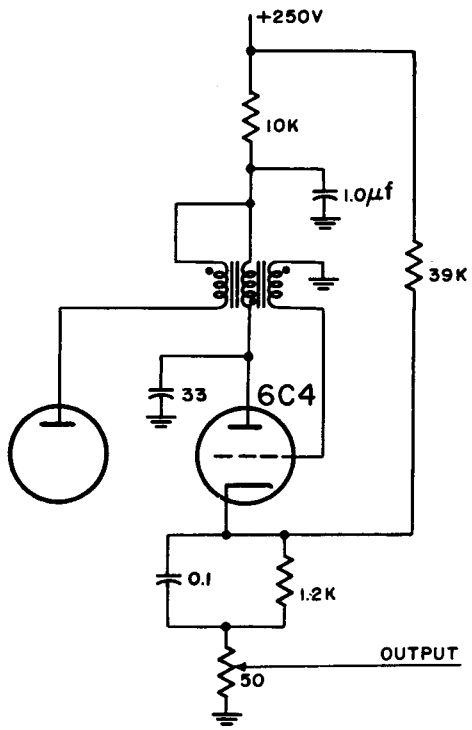
(1) Negative bias: More than two-thirds of the circuits obtained bias by applying a negative voltage to the grid as shown in figure 6–1. This method has the conflicting requirements of low resistance in the grid circuit and low current drain from the bias supply. Some saving in the size of the bypass capacitor is possible, since the grid current is smaller than the cathode current.

(2) Positive bias: About a quarter of the circuits used a positive voltage obtained from the plate supply for cathode bias (fig. 6–2). Positive bias wastes more power than negative bias, but in the majority of these circuits it eliminated the need for a negative supply voltage on the chassis.

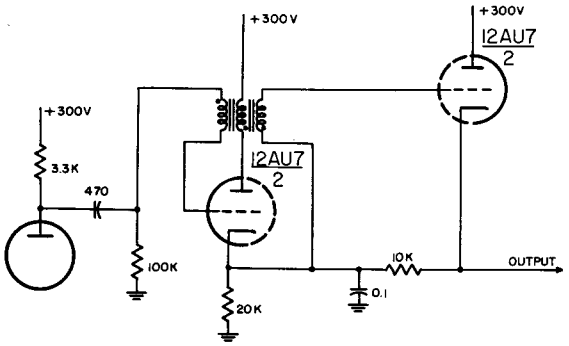
(3) Series cathodes: This less generally applicable method, shown in figure 6–3, was used



TRIGGERED BLOCKING OSCILLATOR
NEGATIVE BIAS
Fig 6-1



TRIGGERED BLOCKING OSCILLATOR
POSITIVE BIAS
Fig. 6-2



TRIGGERED BLOCKING OSCILLATOR
SERIES CATHODE BIAS
Fig. 6-3

in only two cases. An adjacent tube whose cathode resistance can be tapped to furnish the blocking oscillator bias is required. Apart from the fact that such a tube is not always available, this method is likely to result in interaction between the two circuits.

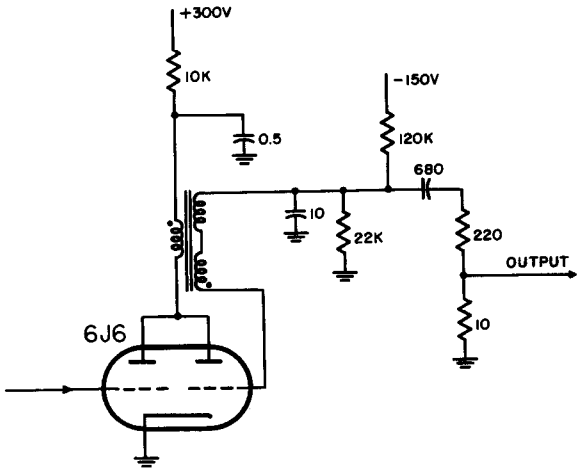
(*b*) Trigger methods: The triggering methods were equally divided between series and parallel.

(1) Series trigger: Most examples of this type used a cathode follower in series with the grid return to furnish a positive trigger (fig. 6–1). A few used the plate circuit of an amplifier as the series element (fig. 6–3), requiring a normally-conducting amplifier to furnish the positive trigger and resulting in a higher series resistance in the grid circuit.

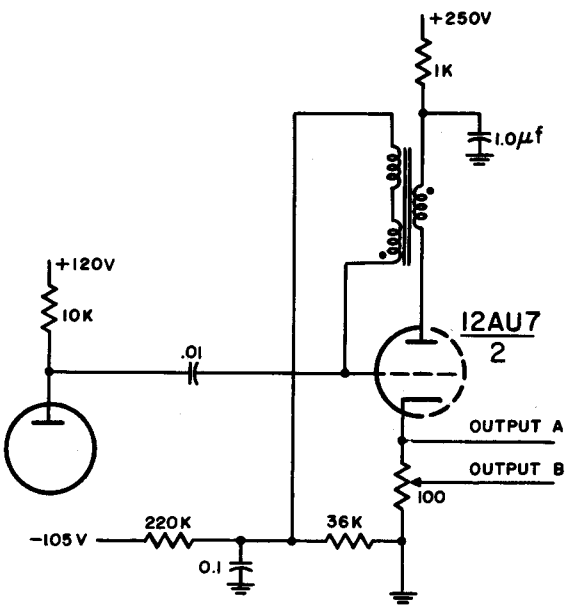
The series trigger minimizes the time delay between the start of the trigger and the blocking oscillator pulse. The principal disadvantage is the blocking oscillator reaction on the trigger source because of the heavy grid current flow.

(2) Parallel trigger: In all but one of these cases, the trigger was applied in parallel with the plate. The majority of the circuits used one winding of the blocking oscillator transformer as a common load for the trigger amplifier and blocking oscillator as in figure 6–4. Some used inductive coupling between the trigger amplifier and the blocking oscillator (fig. 6–2), while in the circuit of figure 6–5, the trigger is applied directly to the grid.

There is more delay associated with parallel triggering than with series, but there is less reaction on the trigger source. Because of the differentiating action of the transformer, a slowly



TRIGGERED BLOCKING OSCILLATOR
GRID WINDING OUTPUT
Fig. 6-4



TRIGGERED BLOCKING OSCILLATOR
PARALLEL TRIGGER TO GRID
Fig. 6-5

TABLE 6-1—*Blocking Oscillators Survey—Summary*

Example		Tube type	Use	Trigger method	Input trigger spacing (μsec)	Output			
Equipment	Circuit					Output from	Duration (μsec)	Amplitude (volts)	Approximate load impedance (Ω)
A	1	12AU7	Trigger	Series	3333	Cathode	1.2	9	40K
	2	12AU7	Display	Series	12.2	Cathode	0.66	5	100K
	3	12AU7	Trigger	Series	3333	Tertiary	1.2	*150	50K
			Trigger			Plate		*150	22K
	4	12AU7	Display	Parallel	3333	Tertiary	1.2	*150	100K
			Trigger			Plate		*150	22K
	5	12AU7	Display	Parallel	3333	Tertiary	1.2	*150	100K
			Trigger			Plate		*150	110K
			Trigger			Cathode		*10	1.5K
	6	12AU7	Trigger	Parallel	3333	Tertiary	2*	*150	50K
	7	12AU7	Trigger	Parallel	3333	Tertiary	2*	*150	50K
	8	12AU7	Trigger	Parallel	3333	Tertiary	2	*150	50K
	9	2C51	Display	Parallel	3333	Cathode	2*	*10	1K
B	1	6J6	Trigger	Parallel	3333	Tertiary	3	340	10K
	2	6J6	Trigger	Parallel	3333	Cathode	3	9	10K
	3	12AU7	Trigger	Parallel	3333	Cathode	2*	10	30K
	4	6J6	Display	Parallel	3333	Grid	1	3	100K
C	1	6AK5	Display	Series	625–5000	S.P.R.	2*	40	30K
			Trigger			Cathode		20	100K
	2	6J6	Trigger	Series	625–5000	S.P.R.	2*	60	100K
			Display			Cathode		15	50K
	3	6AK5	Trigger	Series	625–5000	S.P.R.	1*	80	30K
			Trigger			Tertiary		80	50K
	4	6AK5	Display	Parallel	625–5000	Cathode	1*	20	100K
	5	6C4	Trigger	Parallel	625–2500	Tertiary	2*	20	50K
D	1	12AT7	Display	Series	305	Cathode	1*	13	100K
	2	12AT7	Display	Series	12.2	Cathode	1*	15	50K
E	1	12AU7	Display	Parallel	1250–5000	Tertiary	0.75 or 3.5	32	30K
			Trigger			Cathode		5	100
	2	6C4	Display	Parallel	1250–5000	Cathode	0.75 or 3.5	15	50K
F	1	12AU7	Trigger	Series	3700	Tertiary	2*	250	50K
	2	5702	Trigger	Series	3700	Tertiary	2*	56	30K
	3	5702	Trigger	Series	3700	Tertiary	2*	80	100K
			Trigger			Plate		60	30K
	4	5702	Trigger	Series	3700	Tertiary	2*	60	30K
			Trigger			Plate		60	50K
	5	5702	Trigger	Series	3700	Tertiary	2*	*60	50K
			Trigger			Plate		62	50K
	6	5702	Trigger	Series	3700	Tertiary	2*	60	100K
	7	5702	Display	Series	3700	Cathode	0.4*	5	100K
	8	5702	Display	Parallel	61	Tertiary	0.4	22	40K
G	1	5703	Display	Parallel	247	Cathode	1*	20	100K

NOTES: * = Estimated.
S.P.R. = Series plate resistor.

rising trigger is not as effective as when applied directly to the grid.

(*c*) Outputs: The outputs from the blocking oscillators were of one or more of the following types.

(1) Cathode: A majority of the circuits obtained one of the outputs from a cathode resistor (figs. 6–2 and 6–5). This gives a positive output from a low impedance source. Amplitudes up to 50v can be obtained with cathode resistors of 220Ω or less.

(2) Tertiary: A third winding on the blocking oscillator transformer (fig. 6–1) was frequently used. Either polarity may be obtained by this method and the output can be isolated from ground (fig. 6–3). Overshoot can be eliminated by means of a diode if necessary.

(3) Plate: A negative output from the plate was used frequently where more than one output was required.

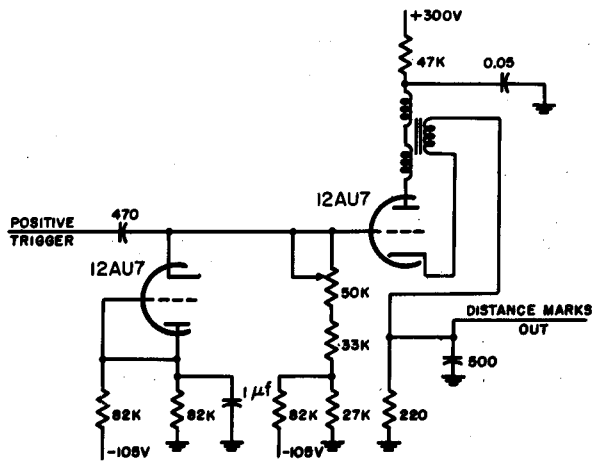
(4) Series resistor in plate circuit: There were a few cases of series resistors in the plate circuit (fig. 6–1). The output is the same as the cathode output but negative in polarity.

(5) Grid winding: There was one example of a positive pulse output obtained from the grid circuit (fig. 6–4).

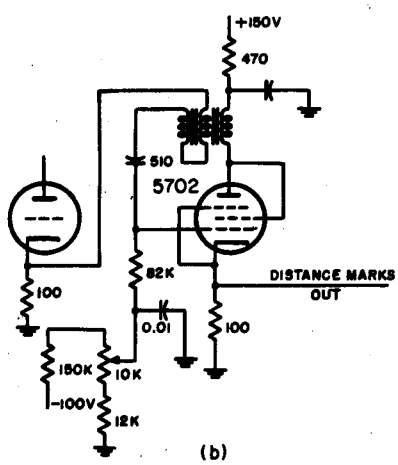
6.2 *Summary of Circuits in Current Use:* From this survey the conclusion was drawn that most triggered blocking oscillator requirements can be met with two very similar preferred circuits: one for low pulse rates and one for high pulse rates. The requirements for various outputs can be met by allowing choice of load resistor and point of taking output. The series-triggered blocking oscillator was added to cover applications where the trigger rise is too slow for parallel triggering.

7. BLOCKING OSCILLATOR PULSE-FREQUENCY DIVIDERS

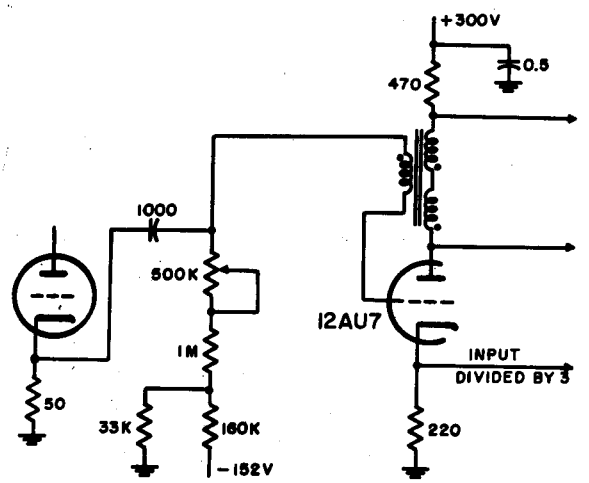
Blocking oscillator pulse-frequency dividers are used to divide from a high to a low pulse frequency. Although usually employed in the generation of distance-marks for radar indicators, they are sometimes used in a master-trigger circuit to produce pulse repetition frequencies.



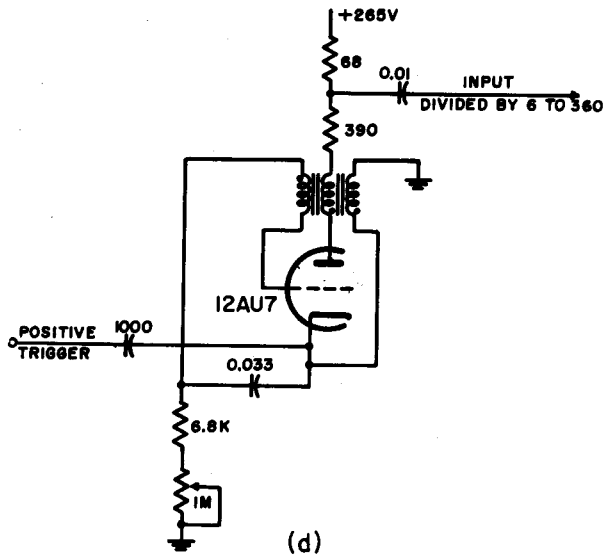
(a)
PLATE-TO-CATHODE COUPLED



(b)
Fig. 7-1 PLATE-TO-GRID COUPLED



(c)
PLATE-TO-GRID COUPLED



(d)
Fig. 7-1 PLATE-TO-CATHODE-TO-GRID COUPLED

7.1 *Examples of Dividers in Current Use:* The following is a summary of the various blocking oscillator pulse-frequency dividers found in equipments during a survey. The circuits are shown in figures 7-1a through 7-1d.

(a) *Plate-to-Cathode Coupled:* The turns ratio of the plate winding to the cathode winding is 2 to 1, which is a convenient ratio with ordinary pulse transformers. It is necessary for this ratio to be greater than unity to enable the plate circuit to drive the lower impedance cathode circuit, thus permitting a loop gain greater than unity. A turns ratio of 2 to 1 is satisfactory for most purposes. [1] Although this type of circuit is

[1] Britton Chance, ed., *Waveforms, Rad. Lab. Series*, vol. 19, McGraw-Hill, 1949, p. 228.
[2] Ibid.

more stable with heater voltage variations than other blocking oscillator circuits, the delay from the start of the input pulse to the start of the output pulse is greater. This is because the initial slope of the output pulse is smaller in the plate-to-cathode coupled type.[2] The diode in the grid circuit is used to insure that the capacitor discharge starts from the same voltage at the end of each output pulse. The shunt capacitor on the cathode resistor serves to eliminate the overshoot on the output pulse.

(*b*) *Plate-to-Grid Coupled:* This arrangement of the feedback circuit with step-up turns ratio yields higher output pulse amplitudes than a 1 to 1 turns ratio. The pulse delay, however, for a given input-trigger rise time is greater than when the turns ratio is 1 to 1. Controlling the circuit by varying the grid bias is undesirable for general application. The range of control by bias variation is not as wide as by variation of the grid resistance. If the original bias is set higher to increase the control range, then the required trigger amplitude becomes correspondingly greater, increasing the chances of instability.

(*c*) *Plate-to-Grid Coupled:* This connection of the transformer windings to give a voltage step-down to the grid yields maximum peak pulse voltages at the plate and maximum pulse duration from a given transformer. The latter is true because this arrangement increases the inductance of the plate winding and lowers the magnetizing current. However, the pulse delay is greater for a given trigger rise time than when the turns ratio is 1 to 1.

(*d*) *Plate-to-Cathode-to-Grid Coupled:* Since the grid-to-cathode loop of this circuit is not connected to ground, parallel triggering must be employed. Output pulses cannot be taken from the cathode since the trigger is applied at that point. The voltage and current pulses obtained from this circuit are smaller than from other types. The division ratios are much higher than recommended because stability of count is unimportant in this case. This circuit will operate free running when no input triggers are received because of the absence of fixed bias.

7.2 *Summary of Types in Current Use:* The circuits previously discussed were designed for specific purposes. Although the disadvantages pointed out may be tolerated, they become detrimental in a general application. The characteristics desired are as follows: (1) small pulse delay, (2) wide range of control, (3) provisions for operation with a periodic pulse train, and (4) the feasibility of obtaining positive voltage pulses of reasonable amplitudes. From the discussion of this survey it appears that most blocking oscillator pulse-frequency divider applications can be met by the use of a circuit with a 1 to 1 feedback ratio from plate to grid, fixed grid bias, and control of the grid circuit resistance.

7.3 *Additional Design Data for PC 50 and 51:* Fixed bias is necessary when operation is intermittent to keep the frequency divider cut off when no synchronizing triggers are received and to insure that operation begins at the start of the gate. The bias voltage used should be large enough so that a -10% change does not bring the tube within the conducting region when no input pulses are received, and small enough so that the trigger amplitude may have a reasonably small value.

At the end of the output pulse the bias of any blocking oscillator has increased to several times the quiescent value due to the grid current flow during the pulse. The time required for the bias to recover to the quiescent value is a function of the grid circuit time constant. The bias level at which the blocking oscillator fires is not only a function of the grid circuit time constant, but also of the trigger amplitude. In frequency dividers it is necessary to trigger on the relatively steep portion of the discharge curve for maximum discrimination between the desired trigger and the ones immediately adjacent. A method of calculating the points at which the change in grid voltage is maximum between the nth and $(n-1)$st trigger pulses follows:

The magnitude of the grid voltage at any instant after termination of the output pulse is

$$e_g = E\epsilon^{-t/RC} + E_{cc}.$$

where E is the voltage across the grid capacitor at the beginning of the discharge, E_{cc} is fixed bias (fig. 7-2), and ϵ is the natural logarithm base.

The change in the grid voltage in the interval between the nth and the $(n-1)$st triggers is

$$\Delta e_g = E[\epsilon^{-t/RC} - \epsilon^{-mt/RC}]$$

where $m = \frac{n-1}{n}$.

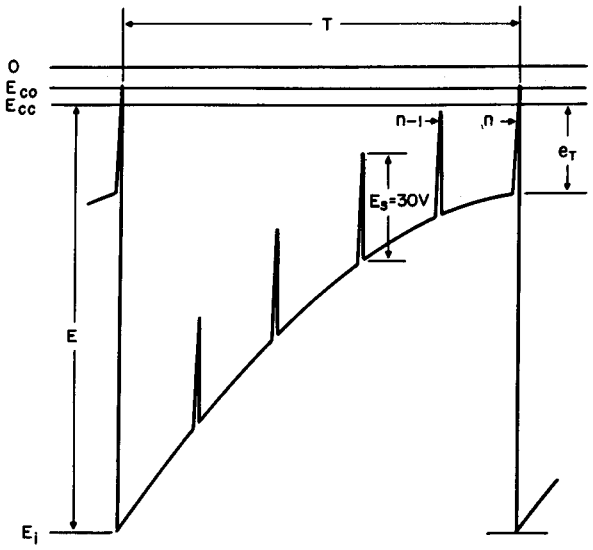


Fig. 7-2 VOLTAGE ACROSS C_1

By differentiating and equating the derivative to zero, Δe_g maximum occurs when

$$\epsilon^{-t/RC} = m\epsilon^{-mt/RC}$$

or when $T/RC = n \ln \frac{n}{n-1}$.

This is the general formula used in figure 7-3.

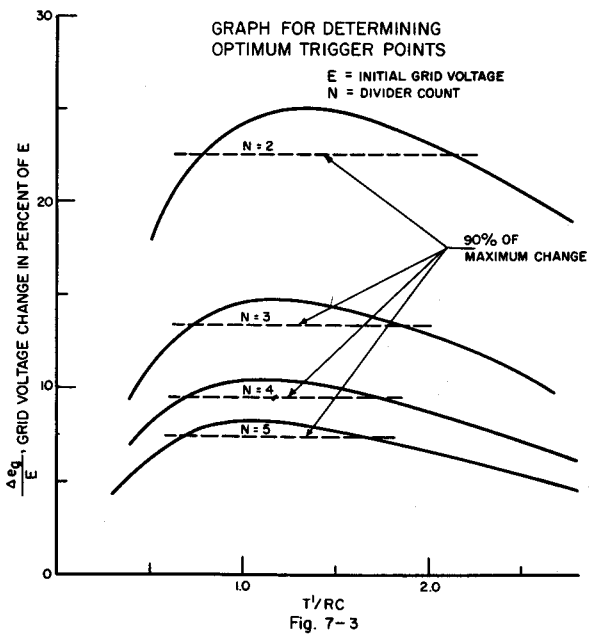


Fig. 7-3

The optimum values of T/RC for counts of 2, 3, 4, and 5 are 1.4, 1.2, 1.14, and 1.12 respectively. These results have been verified experimentally.

The magnitude of this change depends on the capacitor voltage, E, at the beginning of the discharge. This capacitor (C1 in PC 50 and 51) is charged to E by grid current. The major portion of the grid current flows in a series circuit consisting of the output impedance of the trigger source, the capacity C1, the impedance of the grid winding of the transformer, and the internal grid-to-cathode resistance of the blocking-oscillator tube. Hence, the magnitude of E depends on these quantities.

First, the initial voltage to which the coupling capacitor charges is partially governed by the impedance of the trigger source. This impedance is in series with the coupling capacitor; hence as the source impedance increases, the capacitor voltage decreases. When the source impedance is 400Ω or less, it is a small portion of the total impedance in the charging circuit and therefore has negligible effect on the initial voltage. If the impedance is increased to 1500Ω, however, the initial voltage is reduced to 50% of the value at 400Ω.

The initial voltage to which the capacitor charges is inversely proportional to the capacitance; therefore C1 must be small to realize a large initial voltage. However, to obtain the desired pulse width and minimum attenuation of the synchronizing trigger, C1 must be large. The effect of C1 on trigger attenuation, pulse width, and E for typical transformers rated for pulse widths between 0.5 and 2.0μsec is shown in figure 7-4.

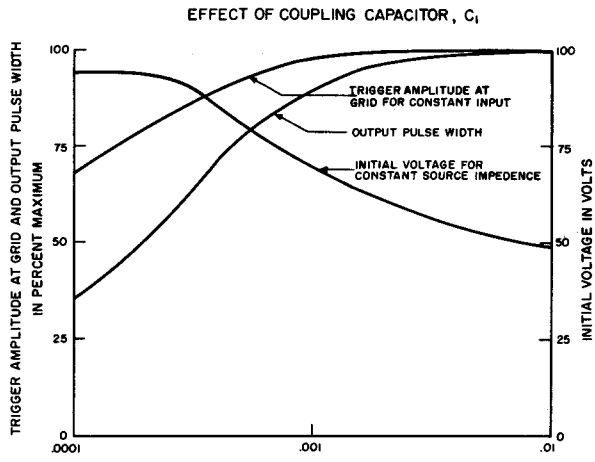


Fig. 7-4 COUPLING CAPACITOR IN MICROFARADS

AT $T/RC = 0.7$ "

The combined impedance of the transformer grid winding and the grid-to-cathode resistance of the tube ranges from 1000 to about 2000Ω.

The maximum and minimum trigger amplitudes for tubes and limit transformers (the transformers for which the initial voltage E across the coupling capacitor is 50v for the low limit and 150v for the high) are shown in figure 7–5. To permit triggering with a 30v pulse, the grid circuit time constant must be variable over the limits shown. It will be noted that the range over which T/RC must be adjusted to cover the limit transformers and tubes is comparable to that shown in figure 7–3 over which the capacitor voltage change between the nth and the $(n-1)$st triggers is within 10% of the maximum change.

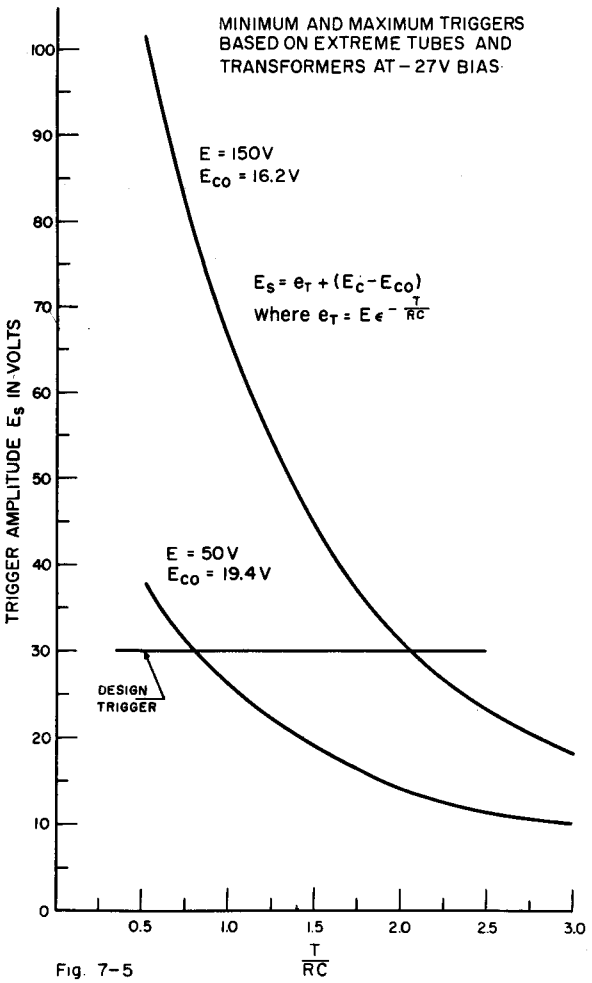


Fig. 7–5

The grid resistors, R1, R2, R3, and R4 in PC 50 along with C1 comprise the grid discharge circuit. In consideration of the fact that the total grid resistance should not be excessive, the coupling capacitor employed is large for a large output pulse spacing. With 1500μμf, the maximum grid resistance, which occurs at an output PF of 200, is 4.75MΩ. The maximum grid resistance, R_g (max.), is based on the lower limit of $T/RC = 0.7$ and the minimum is based on the upper limit of $T/RC = 2.2$. The difference between R_g (max.) and R_g (min.) is the value for the potentiometer, R1, which can be adjusted to cause triggering between the desired limits. R1 thus becomes more than sufficient to allow for variation in grid current in the positive grid region. Although grid current data are not ordinarily given in tube manuals, these data can be determined by test. For a large sample of 12AU7's, this variation was found to be in the order of ±20%. Clamping the grid has little effect on reducing this variation.

A circuit showing a method of cascading dividers to obtain up to 50-mile range markers from one-mile markers is shown in figure 7–6.

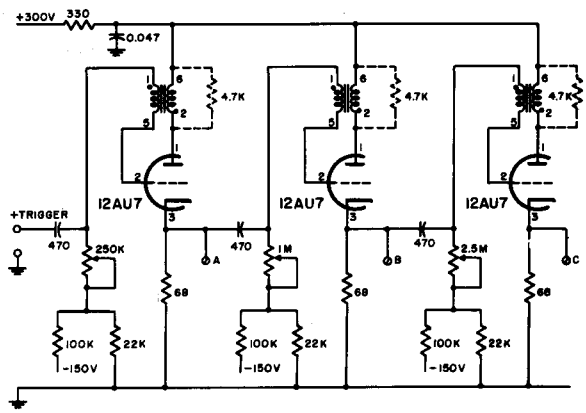


Fig. 7–6 CASCADED DISTANCE MARK DIVIDERS

A, B, and C are the points at which 2 to 5, 10 to 25, and 20 to 50-mile distance marks, respectively, may be obtained. The cathode resistor used should be that which gives an open circuit output of 30v. If 10 and 20-mile distance marks are desired from the second and third dividers, the grid potentiometers may be replaced by 500KΩ and 1MΩ potentiometers, respectively.

The width of the pulse obtained from this circuit depends partly on the primary inductance of the transformer and partly on the coupling

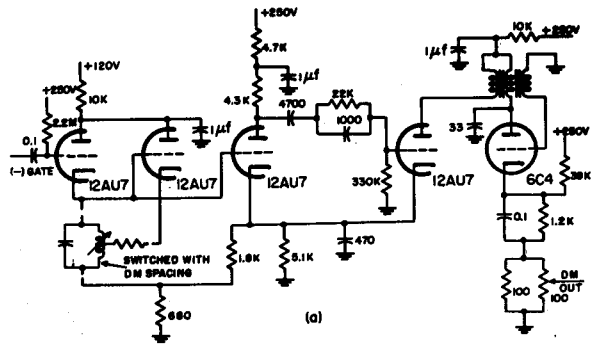
capacitor, with the effect of the coupling capacitor becoming more predominant as the primary inductance is increased. The width will be less than that specified for the transformer if the transformer is rated for the pulse duration obtainable when the primary inductance alone is the determining factor. Therefore, if the pulse width is critical, the choice of transformer must be made empirically.

8. DISTANCE-MARK GENERATORS

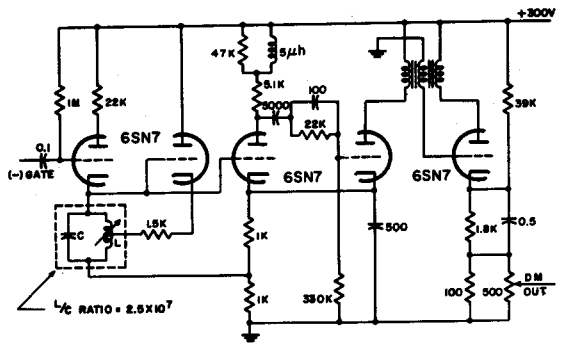
Eight distance-mark generators which are used in airborne search radars were examined. The distance-mark (DM) generator is composed of a series of circuits which form timed pulses. These circuits are a switched Hartley oscillator, a trigger shaper, and a blocking oscillator. The switched oscillator and shaping circuit are interdependent in operation and should be treated together. The blocking oscillator which terminates the chain is also discussed in section 7. A tabulation of DM generator characteristics is given in table 8–1, and schematic diagrams are shown in figures 8–1, 8–2, 8–3, and 8–4.

These medium-precision DM generators all use a Hartley oscillator to determine the marker interval. A distinction must be made between the spacing and mileage range. DM spacing is a uniform spacing such as a marker every five miles, whereas the range is the sum of the spacings and is determined by the length of the input gate.

The sequence of operation of the generator is as follows. The switch tube is normally conducting through the inductance and prevents oscillation. When a negative gate is applied, the switch tube is cut off, starting the oscillation. The sine-wave is initially negative-going, and the spacing must be determined by the interval between the negative-going portions of the sine-wave. The trigger shaper squares and peaks the wave and provides the trigger for the blocking oscillator which is the



DM GENERATOR USING MV SHAPER, BIASED CATHODE BLOCKING OSCILLATOR



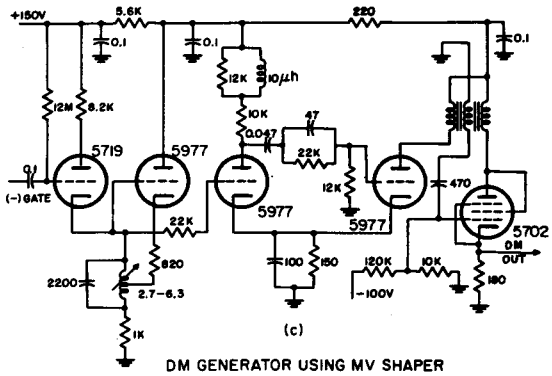
DM GENERATOR USING MV SHAPER, BIASED CATHODE BLOCKING OSCILLATOR
Fig. 8-1

TABLE 8–1—*Distance-Mark Generator Characteristics*

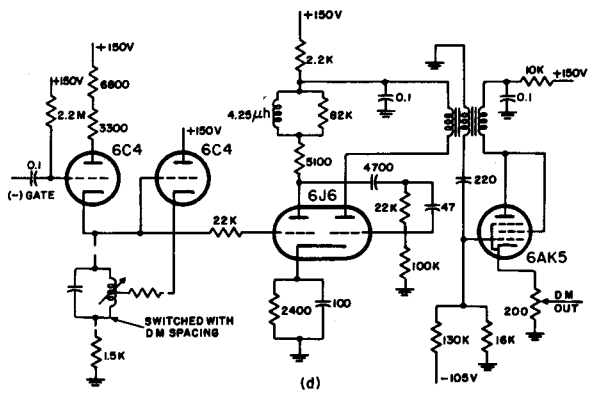
Example	DM spacing, miles	Type shaper	Type triggering	Switch	Tube types oscillator	Trigger shaper		Blocking oscillator
A	2,5,25	MV [1]	Parallel, Third W. [2]	½ 12AU7	½ 12AU7	½ 12AU7	½ 12AU7	6C4.
B		MV	Parallel, Third W.	½ 6SN7	½ 6SN7	½ 6SN7	½ 6SN7	½ 6SN7.
C	1⅔ uses divider for 5 and 10.	MV	Parallel, Third W.	5719	5877	5977	5977	5702.
D	2,5,10,20,50	MV	Parallel, Third W.	6C4	6C4	½ 6J6	½ 6J6	6AK5.
E	1,divider,10,20.	Amp [1]	Series	½ 12AU7	½ 12AU7	6AU6	½ 12AU7	½ 12AU7.
F	20	Amp	Series	5703	5703	5702	5703	5703.
G	2,5,25	Amp	Series	½ 12AU7	½ 12AU7	6BN6	½ 12AT7	½ 12AT7.
H	10,40	Amp	Parallel	½ 12AU7	½ 12AU7	½ 12AT7	½ 6J6	½ 6J6.

NOTES:

1. MV, monostable multivibrator; Amp, over-driven amplifier.
2. Third winding of blocking oscillator transformer.



DM GENERATOR USING MV SHAPER



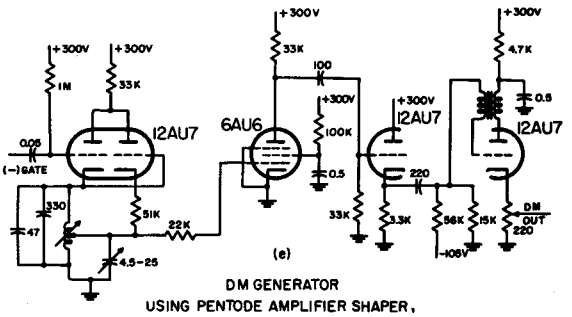
DM GENERATOR USING MV SHAPER
Fig. 8-2

source of the narrow marker pulses. These pulses are mixed into the video chain.

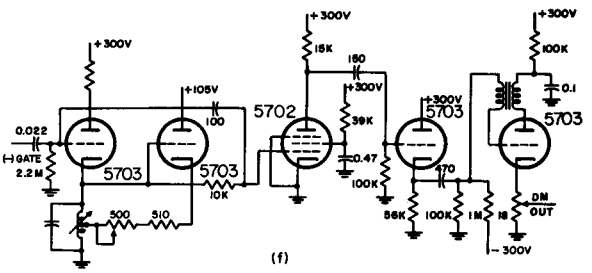
Although only one type of oscillator is used, there are two basic trigger circuit configurations: these are the squaring-and-peaking amplifier and the monostable multivibrator which can also be looked upon as an amplifier with positive feedback. The amplifier shaper is used in circuits *e*, *f*, *g*, and *h*; the multivibrator is used in *a*, *b*, *c*, and *d*.

The method of triggering the blocking oscillator is similar for all circuits using the monostable multivibrator; in this instance parallel triggering is accomplished through a third transformer winding. Parallel triggering is also used with the shaper-amplifier circuit, figure 8-4h. The other amplifier circuits, *e*, *f*, and *g*, use series triggering.

Two methods are used to obtain different DM spacings. One method is to switch *L*,*C* and *R* such as is done in figures 8-1(a and b), 8-2d, 8-4(g and h). The second method used is to employ a basic spacing such as 1 mile, and for greater spacing to divide the markers by means of blocking-oscillator frequency dividers. Circuits *c* and *e* use this method, although the frequency divider is not shown.

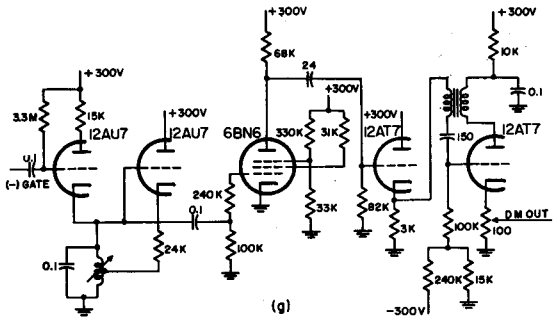


DM GENERATOR
USING PENTODE AMPLIFIER SHAPER,
SERIES TRIGGERED BLOCKING OSCILLATOR

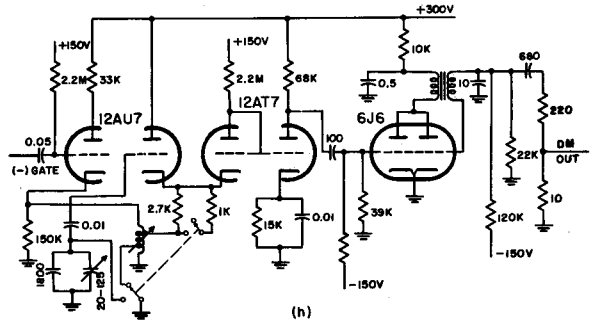


DM GENERATOR
USING PENTODE AMPLIFIER SHAPER,
SERIES TRIGGERED BLOCKING OSCILLATOR
Fig. 8-3

The triode is used extensively in DM generators; of the 40 tube sections only five are not triodes. The two pentodes used in the blocking-oscillator section are connected as triodes. In the trigger-shaper amplifiers, two use pentodes and one uses a gated beam amplifier. The DM generators using the MV shaper use triodes throughout, and the generators using amplifier-shaper use all triodes except for the squaring stage, where a pentode is used.



DM GENERATOR
USING GATED BEAM AMPLIFIER SHAPER
SERIES TRIGGERED BLOCKING OSCILLATOR

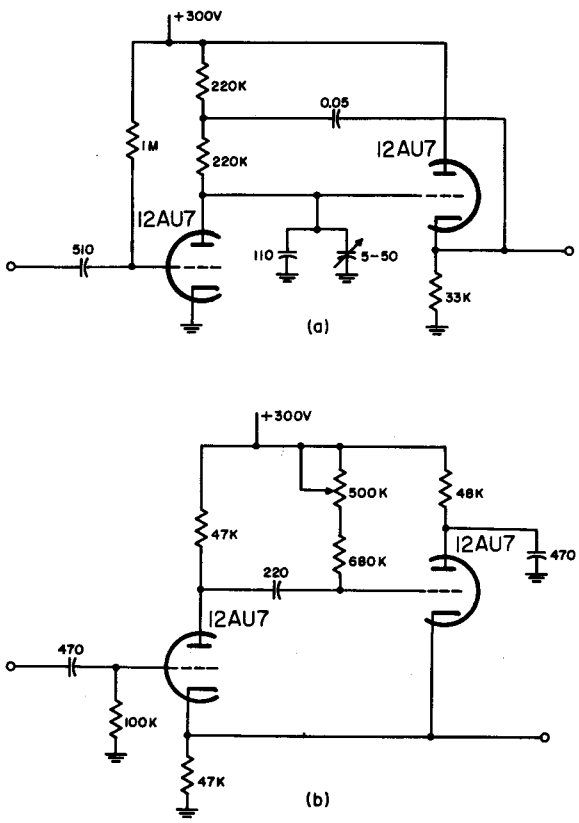


GENERATOR USING AMPLIFIER SHAPER.
BLOCKING OSCILLATOR OUTPUT TO GRID
Fig. 8-4

9. DELAY CIRCUITS

Means of obtaining time delays are an essential part of pulse systems in which the control and measurement of time relationships are necessary. Vacuum tube circuits provide a versatile means of obtaining both fixed and variable delays. Passive delay networks are also used but will not be considered in this section.

In the equipment surveyed, two types of time delay circuits were common: fixed delays of less than 100μsec and delays which are variable from 0 to 2500μsec. The principal circuit types used to perform these functions were the multivibrator, bootstrap, and phantastron. There were one or two examples of simple *RC* circuits used to generate fixed delays by triggering a blocking oscillator, but these were a minority. Phantastrons and bootstraps used as a part of sweep circuits, automatic tracking circuits, and automatic frequency control systems are not included here since, in general, these circuits must be considered as a unit.



30 μsec FIXED DELAY

Fig. 9-1

9.1 *Fixed Delays:* Figure 9–1 shows examples of fixed delay circuits. Example 9–1a is a simple type of bootstrap and 9–1b is a multivibrator; both are used to provide a buffer interval between synchronizing and video information in a radar relay transmitter. In each case an accuracy of $\pm 10\%$ is sufficient.

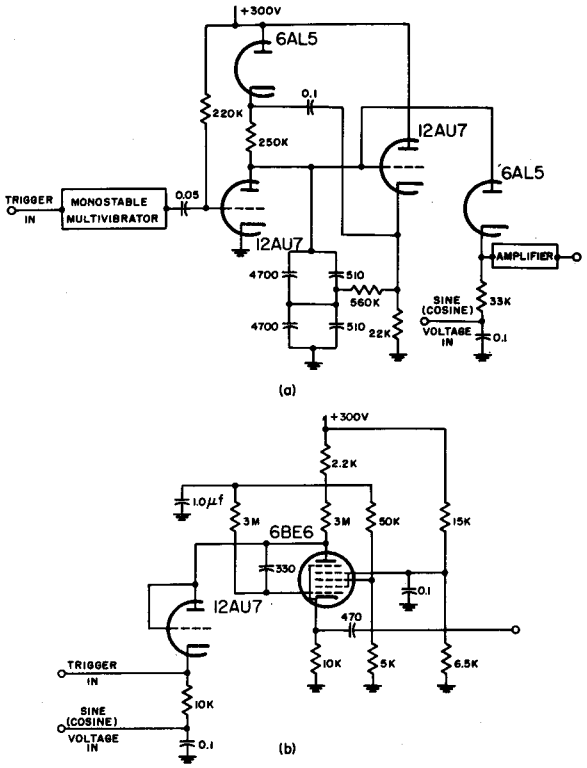
There is little choice between the two circuits on the basis of complexity, number of tubes, or accuracy. The accuracy of the multivibrator is not as good as the bootstrap but is more than adequate for the application. The bootstrap suffers from the disadvantage of requiring a gate at least as long as the desired delay. In the system in which the bootstrap is used, the gate was needed for other applications and therefore was available without additional circuits. However, the multivibrator is a better choice for general applications since it can be triggered by a pulse (see PC 41).

The phantastron was not considered in this application since it offers no advantages when accuracy is not required. For accurate fixed delays it is better than the multivibrator because its performance is less dependent on tube characteristics. The smaller capacitor required to generate a given delay may be an advantage in some cases.

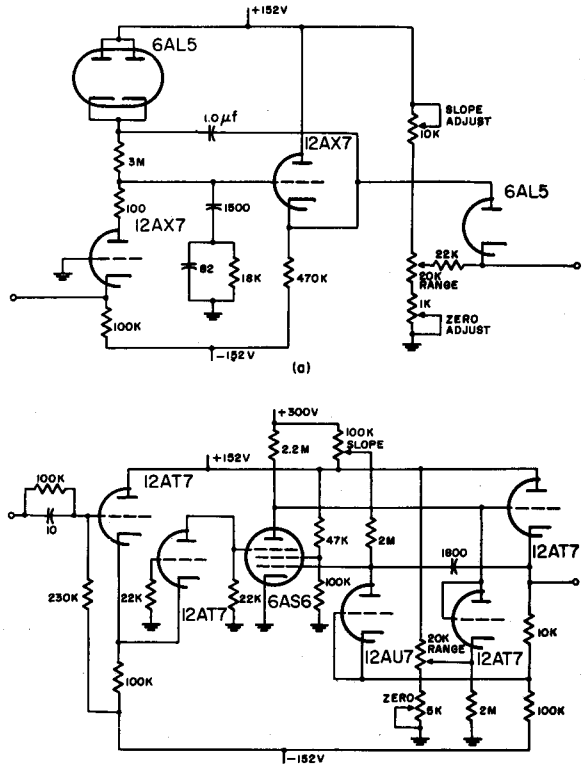
9.2 *Variable Delays:*

(*a*) Precise: For variable delays, the bootstrap and phantastron are used interchangeably. Figures 9–2a and 9–3a show two bootstrap circuits which were replaced in later models of the same equipment by the phantastron circuits shown in 9–2b and 9–3b.

The phantastron circuit of figure 9–2b with two cathodes developed the 50 to 350μsec delay that had formerly been generated by the bootstrap circuit of figure 9–2a using eight cathodes. Both circuits are capable of the required 0.5% accuracy. The circuits preceding and following those shown are almost identical; that is, the trigger and control voltage are furnished by similar circuits and the outputs of both circuits drive blocking oscillators. The bootstrap circuit requires a multivibrator to generate the necessary gate and two stages of amplification following the comparator diode to sharpen the output waveform. The phantastron circuit furnishes its own gate, and



50 TO 350 μsec DELAY
Fig. 9-2



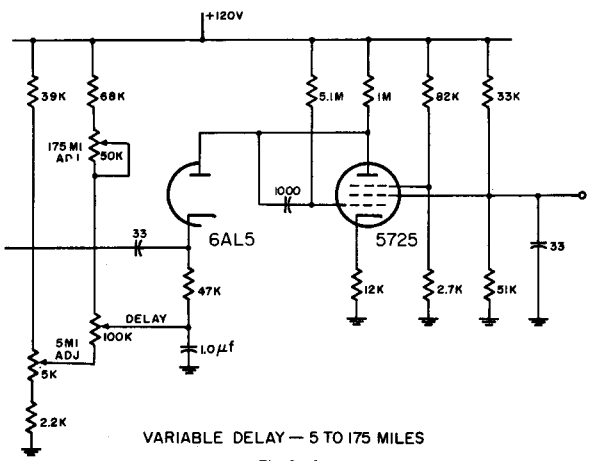
0-200 MILE DELAY
(b)
Fig. 9-3

eliminates the necessity for the amplifiers by using a higher than normal cathode resistor and triggering the blocking oscillator with the trailing edge of the cathode waveform.

In figures 9-3a and 9-3b, a bootstrap circuit and a phantastron are again used interchangeably. The two circuits are triggered by a gating multivibrator, both receive their control voltages from ten-turn potentiometers calibrated in distance units, and both drive blocking oscillators through transformers of similar construction. The accuracy required is 6μsec or 1% of the delay setting, whichever is greater.

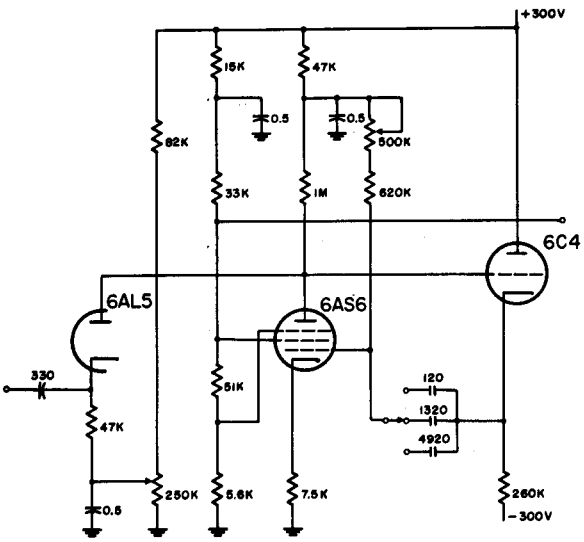
In this case the gate-generating multivibrator cannot be eliminated with the change to the phantastron, and no saving in tubes results. Some economy of cathodes in the phantastron circuit could have been obtained by more conventional methods of triggering and obtaining the output. The cathode follower in the phantastron circuit is necessary to minimize the recovery time (the duty factor is 75% in this case) and the diode-connected 12AU7 is used to compensate for heater voltage changes.

(*b*) Nonprecise: Figures 9-4 through 9-6 show phantastron circuits from three different equipments. Each of these circuits is used to delay the beginning of a cathode-ray tube sweep for expanded displays. The accuracy requirements are low since no measuring is done with the delay circuit, but good stability is required. The circuits all use the 6AS6 or one of its equivalents for the phantastron.



VARIABLE DELAY — 5 TO 175 MILES
Fig. 9-4

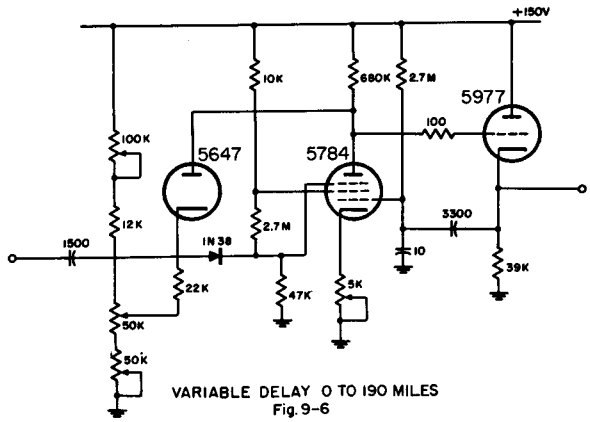
Circuit 9–4 is a true cathode-coupled phantastron. The recovery time is minimized by using a small grid capacitor and limiting the maximum control voltage to about 70v. The $R_g C_g$ product must be correspondingly increased by using a large grid resistance. The trailing edge of the screen waveform is differentiated and used to trigger a blocking oscillator through a trigger amplifier.



VARIABLE DELAY – 0 TO 5, 60, AND 200 MILES
Fig. 9–5

Circuit 9–5 is a cathode-coupled phantastron with some additional coupling obtained by returning suppressor and screen to the same divider. The cathode follower reduces the recovery time and also provides a low-impedance point for the range switching. The trailing edge of the screen waveform is again used to trigger a blocking oscillator.

Circuit 9–6 is similar to 9–5 but employs subminiature tubes and is triggered by a positive pulse on the suppressor rather than a negative one on the plate. The crystal diode is used to prevent the phantastron operation from being interrupted by the trailing edge of the trigger. A positive



VARIABLE DELAY 0 TO 190 MILES
Fig. 9–6

trailing edge is required in this case and the plate waveform is used because its amplitude is greater than the cathode signal. The cathode follower is helpful in this application because of its low-impedance output and because it sharpens the plate rise at the end of rundown by reducing the recovery time.

It can be shown theoretically that both the phantastron and the bootstrap are capable of 0.1% linearity. For this accuracy the number of tubes in the two circuits is about the same. The bootstrap has a slight advantage over the phantastron in this respect because the tube types used are diodes and triodes, which are usually very common in pulse equipment, while the tube used for the phantastron may be the only one of its kind in the set.

The bootstrap requires a gate at least as long as the maximum delay; in many cases an additional multivibrator must be added for this purpose. Since the phantastron produces its own gate, a short trigger pulse is all that is required. Positive or negative outputs with well-defined leading edges may be obtained readily from the phantastron. The bootstrap output is usually positive and has a slower rise than the phantastron.

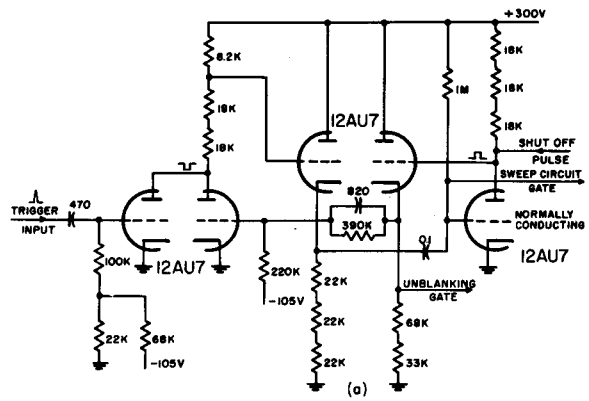
The phantastron was picked as the preferred variable time delay circuit on the basis of its flexibility in triggering and outputs. In many cases the use of the phantastron will result in a saving in tubes as well.

10. MAIN GATE MULTIVIBRATORS

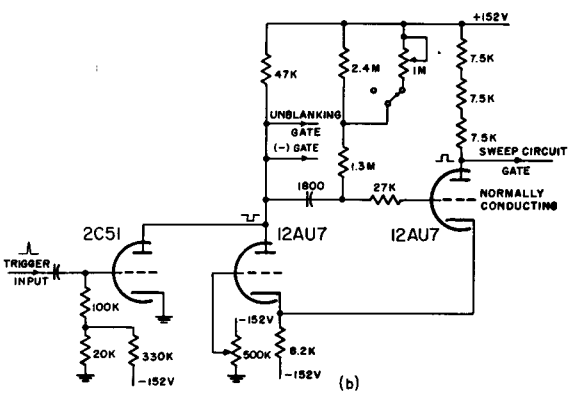
The main gate multivibrator used in radar equipment and other applications provides the gate during which the display sweep is generated, together with gates for generating waveforms which must be coincident with the display sweep. In nearly all cases, the gate for unblanking the cathode ray tube is obtained from this source. In those equipments in which no delayed sweeps are used, the gate for opening the range-mark switch tube may also be obtained from this circuit. The main gate multivibrator sometimes provides gates for generating the range strobe and for sweep centering. In some instances, an output from this multivibrator is differentiated to provide a pulse either at the leading or trailing edge of the main gate.

The main gate multivibrator must provide as many different gate lengths as there are range sweeps on the associated display. When only two different range sweeps are used, this is usually accomplished by ganging the timing elements in the multivibrator with those in the sweep circuit. When a continuously-variable range sweep or more than two fixed range sweeps are used, however, the gate is often terminated by a shutoff pulse applied to the multivibrator. In these cases, it is only necessary that the period of the multivibrator as determined by its own *RC* circuit be longer than the longest gate period desired. To insure reliable triggering by the shutoff pulse, however, some circuit refinements in the multivibrator may be necessary. The use of a shutoff pulse, besides requiring another tube, also has the disadvantage that, in some cases, no output can be taken from the multivibrator electrode to which the shutoff tube is connected, since the shutoff tube may introduce a disturbance at this point prior to the actual transistion.

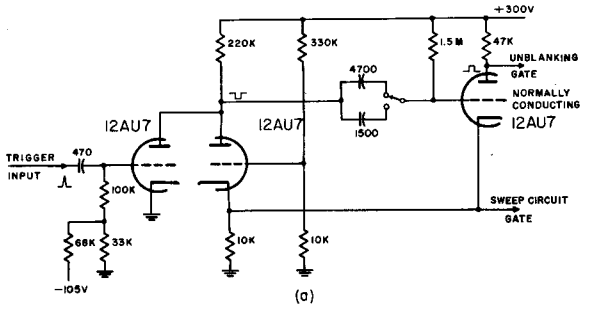
In most cases, it is only the leading edge of the main gate that must be extremely fast, the trailing edge serving no critical timing function. Negative-going leading edges are used whenever possible, since a fast negative-going gate is relatively easy to obtain from almost any electrode except the cathode. A fast rise on the plate of a multivibrator tube can be obtained only if no cross-coupling capacitor is tied to this point. When a plate-to-grid coupled monostable multivibrator is used, a positive gate with a fast leading edge may be obtained from the plate of the multivibrator that is dc coupled to the opposite grid. In such cases, the value of the commutating, or speed-up, capacitor in parallel with the resistor connected between the plate and the grid of the opposite multivibrator tube should not be much larger than that necessary to match the input capacity of the opposite tube. Otherwise, the voltage rise on the plate will be delayed. A positive gate with a fast leading edge may also be obtained from a cathode-coupled monostable multivibrator, since this type has a free plate not entering directly into the multivibrator action. In any case, however, a positive gate at the plate of a multivibrator tube will always be generated at a higher impedance than the negative gate at the same plate. A fast-rising leading edge at low impedance may be obtained across a cathode resistor in the normally-off tube of the multivibrator, but at the expense of amplitude.



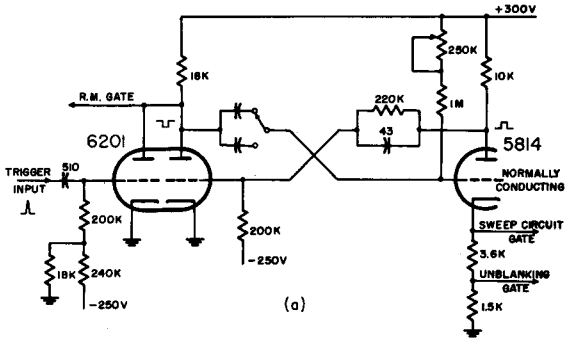
MONOSTABLE MULTIVIBRATOR
PLATE TO GRID COUPLING THROUGH CATHODE FOLLOWER



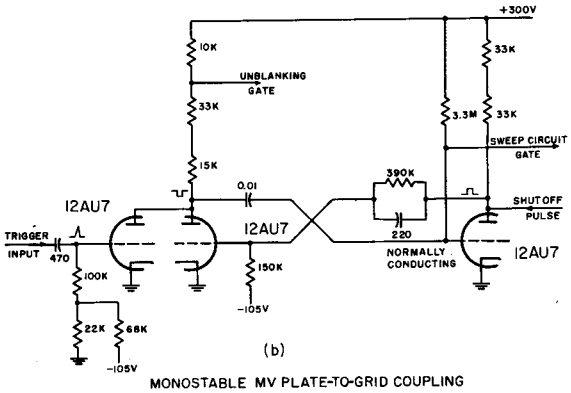
MONOSTABLE MV CATHODE COUPLED
Fig. 10-1



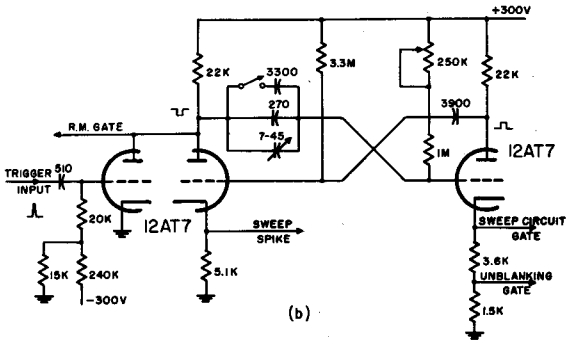
MONOSTABLE MV CATHODE-COUPLED



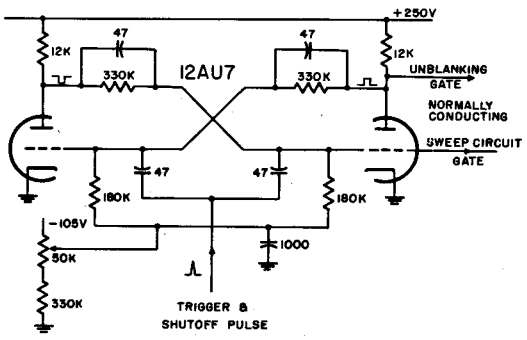
MONOSTABLE MV PLATE-TO-GRID COUPLING



MONOSTABLE MV PLATE-TO-GRID COUPLING
Fig. 10-2



ASTABLE MV SYNCHRONIZED
Fig. 10-3

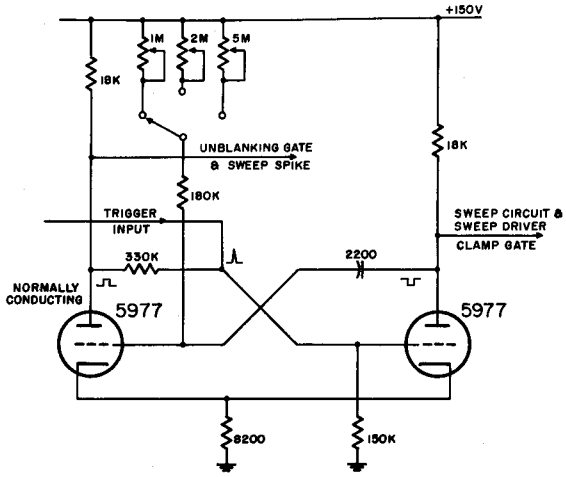


BISTABLE MV
Fig. 10-4

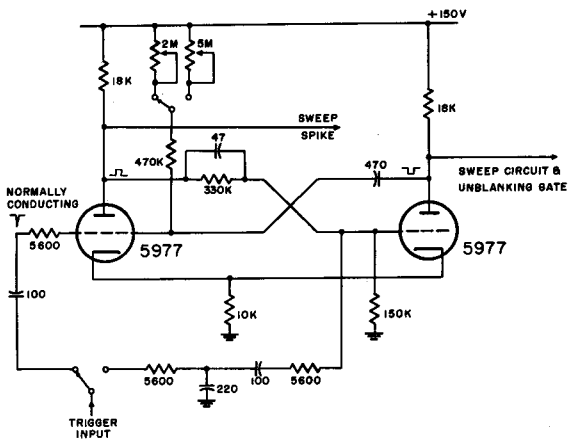
10.1 *Circuit Examples:* The eleven main gate multivibrators shown in figures 10–1 through 10–8 are taken from seven different equipments. The multivibrators shown in figures 10–1a through 10–2b are from a single equipment, as are those shown in figures 10–5 and 10–6. Figures 10–3a and 10–3b are the main gate multivibrators used in two different models of a combination search and gun-laying radar. Figure 10–3a was the circuit used in the later version. The diagrams of these last two multivibrators have been simplified by showing provisions for switching capacitors to obtain only two different gate lengths, whereas four are used in the actual equipments.

10.2 *Types of Multivibrators:* Although an astable multivibrator (fig. 10–3b) or a bistable multivibrator (fig. 10–4) may be used to generate the main gate, the monostable type is preferred for this application. Of the eleven main-gate multivibrators shown in the diagrams, nine are of this type. Of these nine, two (figs. 10–1b and 10–2a) are cathode-coupled types, two (figs. 10–5 and 10–6) have both cathode and plate-to-grid coupling, and the remaining five are plate-to-grid coupled types. Of these five, however, only two (figs. 10–2b and 10–3a) show no added circuit complexity over the basic type. The plate-to-grid coupled multivibrator shown in figure 10–1a uses cathode followers in both plate-to-grid paths. The circuit shown in figure 10–7 has a triode connected to the grid of the normally-on tube in order to limit the negative swing of this electrode. The circuit shown in figure 10–8 uses a diode-connected triode in parallel with the plate of the output tube in order to limit the positive swing at this point.

10.3 *Triggering Methods:* The most common method of triggering the main gate multivibrators shown in the diagram is by connecting the plate of a trigger inverter, or switch tube, in parallel with the plate of the normally-off tube of the multivibrator. This method is used in six cases (figs. 10-1a, 10-1b, 10-2a, 10-2b, 10-3a, and 10-3b). Except for the multivibrator of figure 10-8, which is triggered by a blocking oscillator pulse through the normally-on tube cathode resistor, all the other multivibrators are grid-triggered.



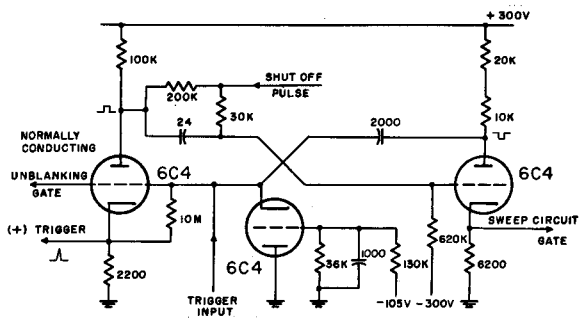
MONOSTABLE MV CATHODE AND PLATE-TO-GRID COUPLING
Fig. 10-5



MONOSTABLE MV CATHODE AND PLATE-TO-GRID COUPLING
Fig. 10-6

In the circuit shown in figure 10-6, the differentiated negative gate from a delay multivibrator is applied to either the grid of the normally-on tube, if an undelayed range sweep is desired, or to the grid of the normally-off tube, when a delayed sweep is used. The negative pulse at the leading edge of the delay gate will trigger the normally-on tube, but will have no effect on the normally-off tube. Conversely, the positive pulse that appears at the trailing edge of the delay gate will trigger the normally-off tube, whereas the negative pulse at the leading edge will have no effect on this tube.

The application of the trigger pulse to both grids of the multivibrator shown in figure 10-4 illustrates a triggering precaution that generally must be observed when a bistable multivibrator is used to generate the main gate. With a bistable multivibrator, a shutoff device must necessarily be used to terminate the gate. During the transient associated with turning on the power, the multivibrator may be forced into the state existing during the generation of the sweep gate with the coupling capacitors so charged that no shutoff signal will be generated. By applying the input trigger to both tubes, the multivibrator can be kept from stalling in this condition.

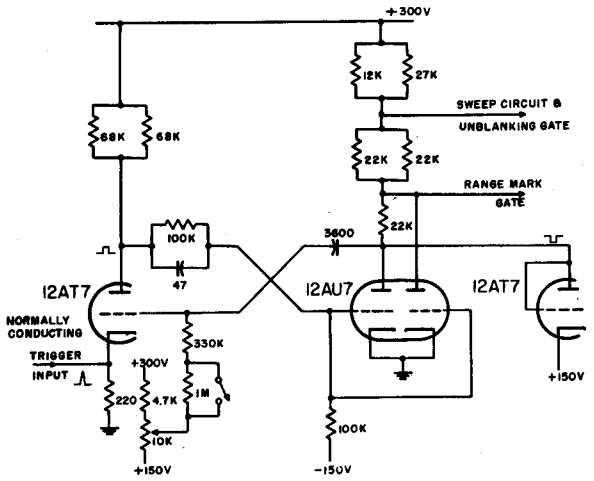


MONOSTABLE MV PLATE-TO-GRID COUPLING
Fig. 10-7

10.4 *Sweep Gate:* Triodes are used as clamp tubes in nine of the sweep circuits associated with the main gate multivibrators shown in the diagrams. These multivibrators must therefore provide negative gates to unclamp the sweep circuit.

A convenient method of coupling a negative gate from the multivibrator to a sweep circuit triode clamp is to tie the grids of the sweep clamp and the normally-on tube of the multivibrator. This can be done, however, if the cathode of the normally-on tube is at the same potential as the cathode of the clamp tube, usually ground. This method of coupling the sweep gate is used in the three multivibrators (figs. 10-1a, 10-2b, and

10–3a). The tube that is cut off during the duration of the main gate in the bistable multivibrator shown in figure 10–4 may be considered the normally-on tube.



MONOSTABLE MV PLATE-TO-GRID COUPLING
Fig. 10-8

In two cases (figs. 10–1b and 10–7), the sweep circuits associated with the main gate multivibrators are clamped by diodes. In these two instances, a positive sweep circuit unclamping gate is required. In the circuit shown in figure 10–1b, a positive gate is dc coupled from the plate of the normally-on tube to a cathode follower, the cathode resistor of which is common with the diode clamp. In the circuit shown in figure 10–7, the cathode of the diode clamp is tied directly to the cathode of the normally-off tube, and the gate is developed across the common cathode resistor. As these positive gates are developed across a cathode resistor in one case, and at a "free" plate in the other case, fast-rising leading edges can be obtained.

A disadvantage of obtaining a positive sweep gate for a diode clamp from a multivibrator cathode resistor is that the amplitude of the sawtooth wave is thereby limited to the amplitude of the voltage across the cathode resistor.

The sweep circuit clamp used with the six other main gate multivibrators shown in the diagrams are all ac coupled. As these require negative-going gates, no special precautions have to be observed to obtain fast waveforms. Too fast a leading edge may, in some cases, even be detrimental to the operation of the circuit, as the negative leading edge may be coupled by the tube interelectrode capacity into the sweep circuit.

10.5 *Unblanking Gate:* Unblanking of the display tube may be accomplished by applying either a negative gate to the cathode of the tube or a positive gate to one of the grids. In the eleven cathode ray tubes associated with the main-gate multivibrators shown in the diagrams, unblanking with a positive gate is the more common, being used in seven cases. In four of the seven cases in which a positive unblanking gate is used at the CRT, the gate is taken as a negative output from the multivibrator and inverted by an amplifier before being applied to the display tube. This is done with the unblanking gates taken from the multivibrators shown in figures 10–3a, 10–3b, 10–7, and 10–8. In these cases, the positive output from the plate of the amplifier is either dc coupled to the CRT or to the grid of a cathode follower if the indicator is located at a great distance from the amplifier. In the three instances in which the positive unblanking gate is taken as a positive output from the main gate multivibrator (figs. 10–1a, 10–2a, and 10–4), the output is derived from an electrode at which the voltage can rise rapidly.

In three of the four displays in which a negative gate is used for unblanking, the gate is generated at the multivibrator as a negative output (figs. 10–1b, 10–2b, and 10–6). In these cases, it is feasible to take the output from a plate that is ac coupled to the opposite grid of the multivibrator. In the one case (fig. 10–5) in which the negative unblanking gate begins as a positive output at the multivibrator, this output is taken from a plate that is dc coupled to the opposite grid. One stage of amplification is required, both to increase the amplitude and to invert.

10.6 *Gate Length:* The length of the gate provided by four of the multivibrators shown in the diagrams is determined by a shutoff pulse. This pulse is derived from a tube which is connected into the sweep circuit so that the voltage on one of its electrodes varies with the sweep voltage. The bias on the shutoff tube is adjusted to a value which will cause the shutoff tube to conduct when the sweep voltage reaches the amplitude necessary to deflect the sweep to the edge of the display tube.

In two of these four cases (figs. 10–1a and 10–2b), the control grid of a sharp cutoff pentode, which is used as the shutoff tube, derives its voltage from the sweep circuit. The plate of this tube is connected in parallel with the plate of the normally-on tube of the multivibrator, causing a negative pulse to appear at this point when the shutoff tube conducts. A slight modification of this arrangement is used with the multivibrator shown in figure 10–7. In this circuit, the plate of the shutoff tube is tied to a point in the dc coupling network between the plate and grid, thus permitting greater flexibility in setting the plate voltage level of the shutoff tube. The shutoff pulse used to terminate the gate generated by the multivibrator shown in figure 10–4 is derived from a thyratron, the plate voltage of which varies with the sweep voltage. When the thyratron conducts at the end of the sweep, a positive pulse which appears across the thyratron cathode resistor is coupled to both grids of the bistable multivibrator.

To insure reliable triggering by the shutoff pulse, it is advantageous to keep the negative voltage on the grid of the multivibrator tube, that is off during the gate period, at a fairly constant value not too far below cutoff. In the circuit shown in figure 10–7, the negative voltage to which this grid can fall is limited by the triode connected to this grid. Because of the long time constant of the *RC* circuit connected to this grid (10MΩ, 0.002μf), the voltage on the grid remains almost constant for the duration of the gate period. In the circuit shown in figure 10–1a, the grid of the tube that is off during the gate period is ac coupled to the opposite plate circuit through a cathode follower. By connecting the grid of this cathode follower to a point close to B+ in the plate circuit resistance network, the voltage swing on the cathode follower is held to a small value. This in turn limits the voltage to which the grid of the cutoff multivibrator tube can fall. Again, the long time constant of the *RC* circuit connected to this grid (1MΩ, 0.1μf) holds the voltage on this grid almost constant for the duration of the gate period. As the main gate multivibrator shown in figure 10–4 is a bistable type, no provision has to be made to hold the grid of the off tube at a constant value. In this circuit, it is only necessary to design the coupling network between plate and grid to maintain a voltage not too far below cutoff on the grid of the tube during the off period.

In the circuit shown in figure 10–2b, the voltage on the grid of the tube that is conducting during the gate period is maintained slightly negative by the resistance values used between the opposite plate and the negative supply. Although this insures that this tube can be easily cutoff by the shutoff pulse, maintaining the grid of this tube slightly negative during its conducting period makes the amplitude of the output from its plate very sensitive to variations in resistor values and supply voltages.

In three of the main gate multivibrators (figs. 10–3a, 3b, and 10–4a), the different gate lengths are obtained by switching components in the *RC* timing network, even though more than two different gate lengths are used. The four different gate lengths provided by the multivibrators shown in figures 10–3a and 10–3b are obtained by switching capacitors, whereas three different potentiometers are used with the multivibrator shown in figure 10–5a.

TABLE 10–1—*Summary of Main Gate MV Parameters*

Example	Gate lengths, miles	PRF pps.	Duty cycle, percent
1	20, 50, 100, 200	300	74.2
2	2, 10, 100, 200	300	74.2
3	50, 150	300	55.7
4	80, 200	300	74.2
5	8, 24, 100, 200	300, 550, 2000	74.2
6	5, 10, 100, 200 variable time delay.	200, 300, 800	49.5
7	Variable 0–5 to 0–10 Variable 0–10 to 0–25 Variable 0–25 to 0–50, 0–120, 0–200, 80–200.	200, 400, 800	59.0
8	15, 30	270	10.0
9	30, 80, 200	270	66.7
10	50, 200	300	74.2

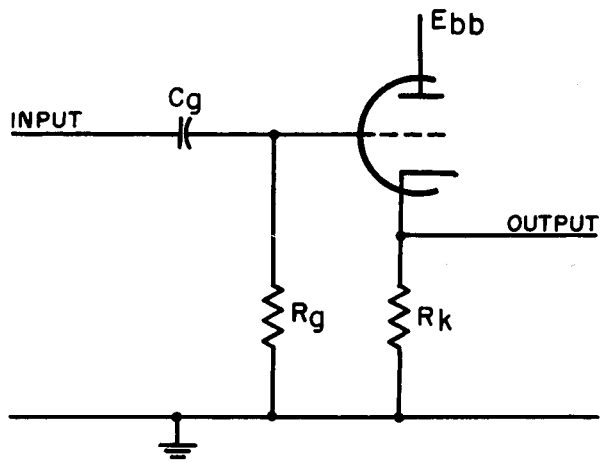
11. PULSE CATHODE FOLLOWERS

There are two major applications of the cathode follower found in the survey; one application is the use of its low output impedance when feeding a line and the second is the isolation of critical circuits which are sensitive to loading. The first application is also discussed in section 3.

11.1 *Circuits in Current Use:* The cathode follower is used to isolate critical circuits such as blocking oscillators, sweep circuits, multivibrators, and so forth, in addition to video circuits. The operating level range may be from a few volts to several hundred. The signal polarity is usually positive: a negative signal is avoided since it tends to drive the tube to cutoff. The rise time required is not extreme for most applications and is in the order of 0.035μsec. Figures 11–1 through 11–4 show representative circuits used in various radar sets. The circuit is simple; however, there are wide variations in tube types, operating supply voltages, and component parts.

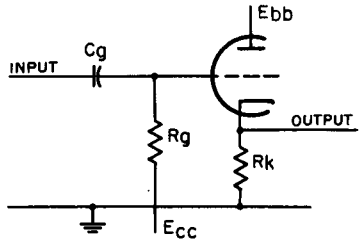
In this survey the circuits have been divided into five groups. Group 1 includes conventional circuits in which a triode is used and the grid and cathode resistors are returned to ground. Group 2 is slightly different in that a grid bias supply is used. Group 3 is also conventional but uses twin triodes in parallel. Group 4 is an example of circuits using pentode-type tubes. Group 5 uses a negative supply connected to the cathode resistor with the grid resistor returned to the cathode instead of ground.

In these circuits the cathode resistor values range from 150 to 50,000Ω. The cathode resistor fulfills several functions: in the conventional cir-



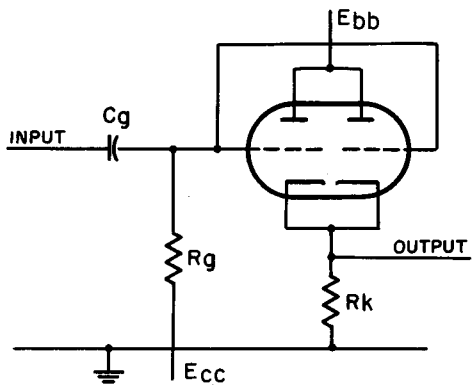
Tube type	E_{bb}	R_k (Ω)	R_g,C_g	Use
5703	150v	4.7K	1M, 0.1μf	Video.
5977	150v	39K	Direct coupled	Blocking oscillator.
5977	150v	8.2K	470K	Pulse amplifier.
12AU7	250v	27K		Video.
12AU7		3.3K	Direct coupled	Blocking oscillator.
12AU7	300v	2.2K	Trans. coupled	Blocking oscillator.
12AT7	300v	3K	82K, 24μμf	RM block-osc. input.
12AT7	150v	5.1K	510K, 0.1μf	Video (IN70 restorer).
2C51	152v	18K	Direct coupled	Gate gen. output.
6C4	250v	10K		Master trigger input.

Figure 11–1.—Conventional Cathode Follower



Tube type	E_{bb}	R_k (Ω)	R_g (Ω)	C_g	E_{cc}	Use
12AT7	150v	5.1K	510K	0.01μf	−1.5v	Video.
5977	110v	150	470K	0.1μf	−4.5	Video.
5977	150v	150	560K	0.1μf	−6.5	Video.

Figure 11-2(a).—Conventional Cathode Follower With Fixed Bias



Tube type	E_{bb}	R_k (Ω)	R_g (Ω)	C_g	E_{cc}	Use
12AU7	150v	510	220K	0.01μf	−6v	Video.
5687	110v	560	1M	0.1μf	+6.4v	Video.
6J6	350v	15K	2.2M	0.22μf	0	Video.

Figure 11-2(b).—Twin Section Cathode Follower

cuit it determines the operating point and consequently the operating plate current and operating voltage levels. Secondarily, the resistor also affects the output impedance, rise and decay times. Operating levels associated with various ranges of resistors fall roughly in the following groups. For resistor values of 100 to 500Ω the level would be less than 10v, since the current required for this output would be at the maximum for the tube, and also the tube would be in or near the grid current region. Under similar conditions for resistors in the 5K to 10KΩ range, the level would be under 100v. For resistors above 20KΩ the level would be several hundred volts and would be

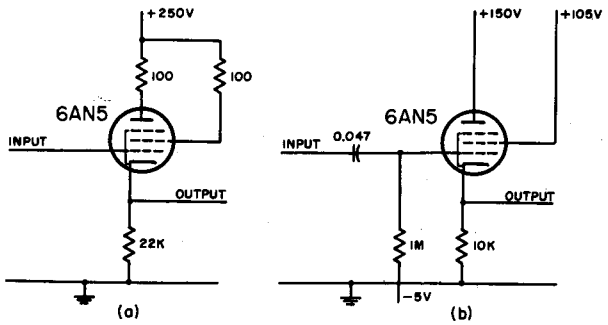


Fig 11-3 CATHODE FOLLOWER USING PENTODE TUBES

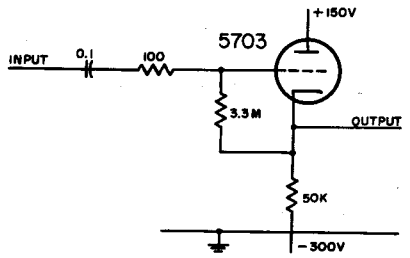


Fig. 11-4 CATHODE FOLLOWER USED FOR BOOTSTRAP INPUT

limited by the supply voltage or the heater-cathode breakdown voltage.

The tube types are mainly triodes and the transconductance ranges from about 2000μmhos to 5000μmhos. When two sections are connected in parallel, the transconductance is doubled with a resultant decrease in output impedance. The electrode capacities are also doubled, but the adverse effect on rise time is balanced by the increased transconductance.

In figure 11-2 the circuits use a separate bias supply. In the case of a small cathode resistor, the current tends to be high. To obtain a suitable operating range it is desirable to use a fixed grid bias and thereby operate at lower plate current. Also when higher value resistors are used, the plate current tends to be low, and biasing with a positive supply permits operation at higher plate-current level.

The use of a pentode in the cathode follower is shown in figure 11-3. Figures 11-3a and 11-3b are connected as triodes. The advantage of the high transconductance of the 6AN5 remains approximately the same as when pentode-connected, about 6000μmhos.

Figure 11-4 shows a circuit variation with the cathode resistor returned to a negative supply and the grid resistor returned to the cathode. Returning the cathode resistor to a negative supply results in a straighter characteristic curve, since the usual curving to cutoff is avoided and operation into the negative region is permitted (fig. 11-5). In effect the two supply voltages are

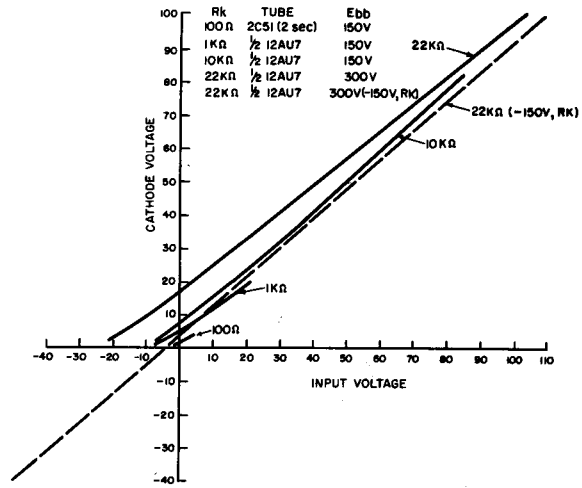


Fig. 11-5 CATHODE FOLLOWER CHARACTERISTIC CURVES FOR VARIOUS CATHODE RESISTORS

additive and the quiescent current is higher than for the plate supply itself. For this reason the peak permissible positive signal will be less than in the conventional circuit. Returning the grid resistor to the cathode instead of ground increases the input resistance of the circuit and also shifts the operating point toward zero bias.

11.2 *Pulse Cathode Follower Circuit Analysis:* The main characteristics to be considered in a cathode follower used to isolate circuits are input loading, operating voltage level, gain output impedance, rise time, and supply voltage. The discussion will be essentially related to the conventional cathode-follower circuit where grid and cathode resistors are returned to ground, to positive pulse signals, and to the prototype miniature twin-triode tube.

(*a*) The input loading will depend mainly on the grid resistor and electrode and wiring capacities. For most applications, the conventional circuit is adequate, and no special connection, such as returning the grid resistor to the cathode to increase the input resistance, is necessary.

(*b*) The operating level of the cathode follower may cover a wide range from a few volts to

several hundred volts. Figure 11-5 shows the difference in the characteristic curve for various cathode resistors. The upper limit is set by the maximum plate current, grid current, or cathode-heater breakdown voltage. In the case of a low cathode resistor, e. g., 100Ω, the operating level is in the order of a few volts since the necessary current approaches the plate-current limit. The grid-current region is also encountered near this limit. As the cathode resistor is increased, the operating level increases until the heater-to-cathode breakdown voltage limits the level. This limitation is removed by raising the heater supply above ground.

The 2v operating level of the 100Ω resistor is associated with a follower which is used to match a low impedance line. To attain higher levels with the same resistor requires power-type tubes and shows that line transmission at high levels should be avoided. The grid current region is also near the levels listed. The plate voltage will affect the grid current region and is selected to have a margin above the operating level.

(*c*) The gain of the cathode follower using a cathode resistor of a few thousand ohms is near unity. However, since the expression for gain is $\frac{g_m R_k}{g_m R_k+1}$, for small resistors the value is considerably lower than unity. For example, in figure 11-5 the gain for the circuit using 100Ω resistor is about one-half.

(*d*) The output impedance is in the nature of an effective impedance since the cathode follower is an impedance changing device rather than a transformer. For resistors of large values, i. e., over 5000Ω, the impedance is approximately $1/g_m$. Otherwise the impedance is more accurately the parallel effect of the cathode resistor and $1/g_m$. With pulse signals the effective impedance depends upon the operating level since the transconductance increases with the plate current. The transconductance will correspond to the highest current attained since the pulse rises to that value quickly. In a conventional follower a negative signal will tend to cut off the follower and the output will therefore be high in impedance. The effective impedance should be specified with the level of the pulse.

(*e*) The rise time of the cathode follower depends mostly upon the tube transconductance, associated capacities, and cathode resistor. For most applications the conventional cathode follower will be adequate and the rise time will be usually less than 0.035μsec (10mc $BW=35/t_r$). The decay time is adversely affected by the follower and in some applications it may be necessary to take it into account. PC 43, figure 43-3, shows the decay time (fall time) for circuits using 10KΩ and 22KΩ cathode resistors and shows that it is several times the rise time. The negative-going portion of a pulse is the part affected: this is the decay time for a positive pulse and the rise time for a negative pulse, as mentioned in the previous paragraph. The follower drives the capacity across the cathode with an effective impedance of approximately $1/g_m$, and the RC charging time is that of the follower impedance and cathode load capacity. When the pulse falls to zero, in a short time the tube is in a low current condition and the voltage of the capacitor decays because of the cathode resistor. If the cathode resistor is appreciably larger than the driving impedance, a longer decay time for the negative-going trailing edge results.

(*f*) The supply voltage for the follower is not critical because of the degeneration inherent in the follower. The performance is only slightly affected if the supply voltage is decreased, for example, from 300 to 150v. As mentioned before, at the higher operating levels it is necessary to maintain a margin between the operating level and the supply voltage. The power dissipation within the tube is favorable for circuits using a high value cathode resistor since most of the power will be dissipated in the resistor.

12. RECEIVER AUDIO CIRCUITS

The audio circuits in communications equipment lend themselves very readily to circuit standardization. This conclusion is a result of a survey of a group of communication receivers whose signal levels, frequency range, and power output requirements were studied in detail.

The circuits considered as audio circuits in this survey are the signal detector and noise limiter, audio voltage amplifier, audio power amplifier, the automatic gain control, squelch, and the broad band cathode follower.

12.1 *Examples of Receiver Audio Circuits in Current Use:* Several receivers have been examined to show current practice in the design of audio circuits. Measurements were made on two of the receivers to obtain signal information that was not readily available.

(a) *Detectors and Detector-Noise Limiter Combinations:* These circuits were broken down into two groups because some of the circuits studied did not employ noise limiter circuits. Figures 12-1 and 12-2 show examples of simple signal detectors. Figures 12-3 through 12-5 show the more complex detector and noise limiter combinations.

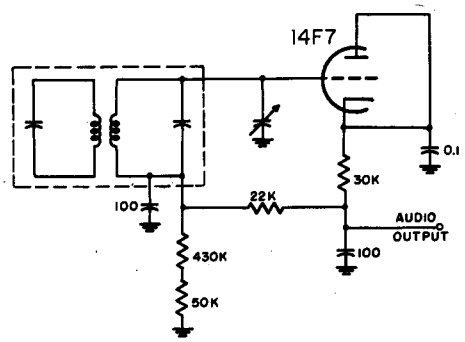
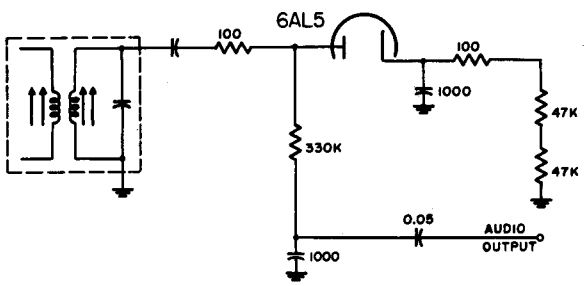
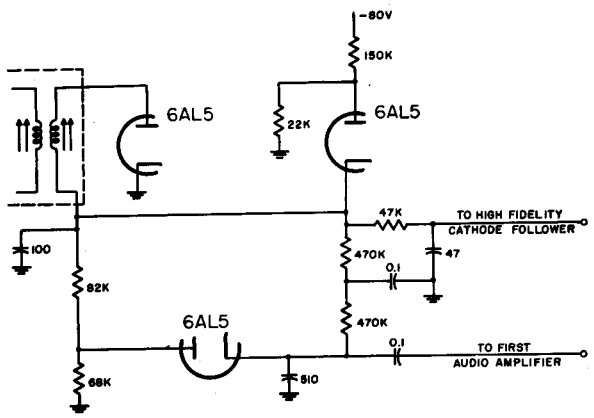


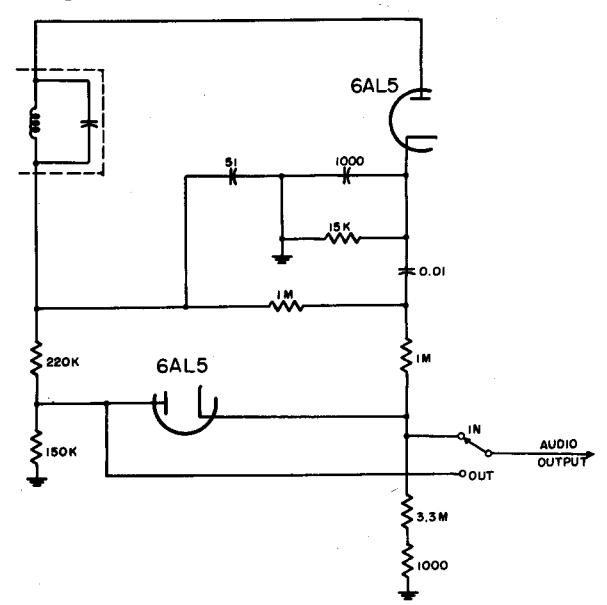
Fig. 12-1



SIGNAL DETECTORS
Fig 12-2

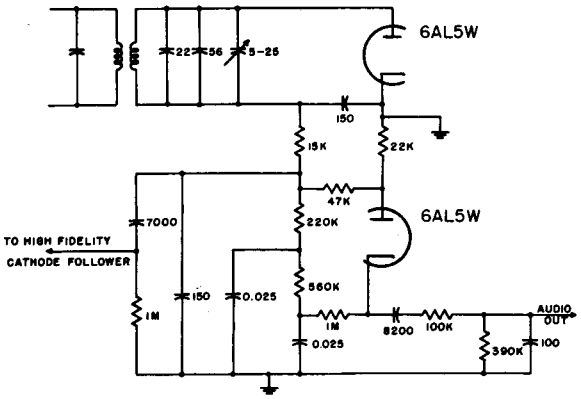


SIGNAL DETECTOR AND NOISE LIMITER
Fig. 12-3

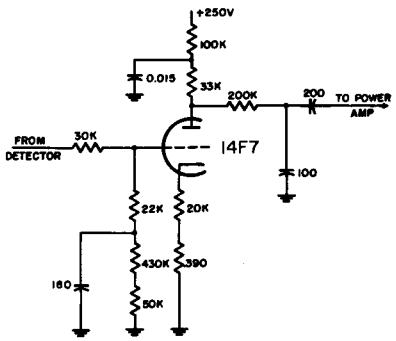


SIGNAL DETECTOR AND NOISE LIMITER
Fig. 12-4

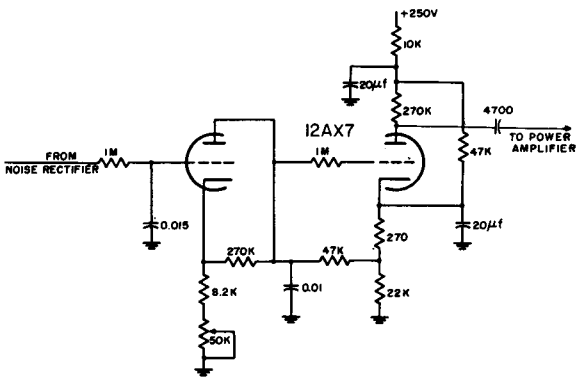
All but one of the examples studied used a 6AL5 detector; the remaining one (fig. 12-1) used a diode-connected triode. All of the examples employing noise limiter circuits used a 6AL5 series noise limiter. Figure 12-3 shows the use of a



SIGNAL DETECTOR AND NOISE LIMITER
Fig. 12-5



AUDIO VOLTAGE AMPLIFIER
Fig. 12-6



AUDIO VOLTAGE AMPLIFIER WITH SQUELCH
Fig. 12-7

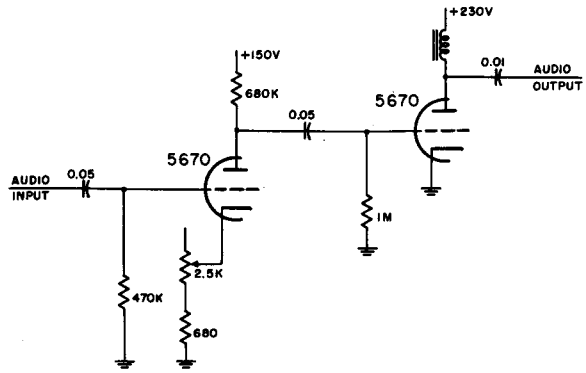
shunt limiter which is used in conjunction with the series limiter so that the noise pulse is prevented from operating the agc circuit and thus desensitizing the i-f amplifier. Two of the receivers had broad-band cathode followers whose inputs were taken from the output of the diode detectors (figs. 12-3 and 12-5).

(b) *Audio Voltage Amplifier and Squelch:* Several general comments can be made about these circuits. All the audio voltage amplifiers studied used a dual triode. However, the amplification factor and the type of triode varied considerably as shown in table 12-1. The amplifier circuit employed in all but one example was the resistance-capacitance coupled type. These circuits are shown in figures 12-6 through 12-9. The remaining example (fig. 12-10) used transformer and resistance-capacitance coupling. Plate load resistors ranged from 15KΩ to 680KΩ. In figure 12-8 the plate load was an inductance. Coupling capacitors ranged from 0.01 to 0.05μf. Most of the circuits used cathode degeneration for stable operation.

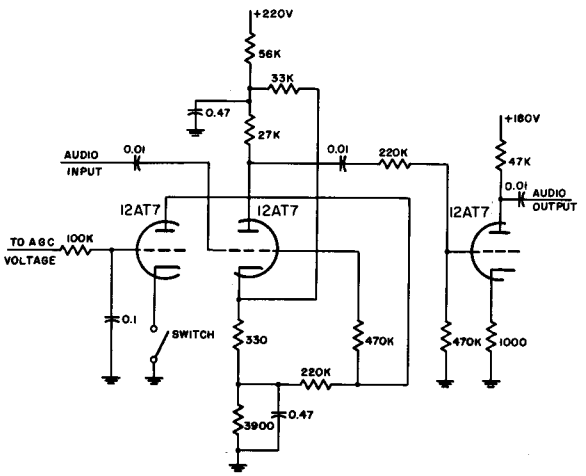
Figures 12-7, 12-9, and 12-10 show the use of squelch circuits in conjunction with the first audio stage. All were of the type that caused the first audio stage to be made inoperative during the no-signal condition. All of the examples studied used a triode type of tube for this operation. In two cases (figs. 12-9 and 12-10) the squelch tube received its input from the agc circuit. Figure 12-7 shows the squelch circuit input from a noise rectifier and amplifier circuit.

TABLE 12-1—*Summary of Voltage Amplifier Characteristics*

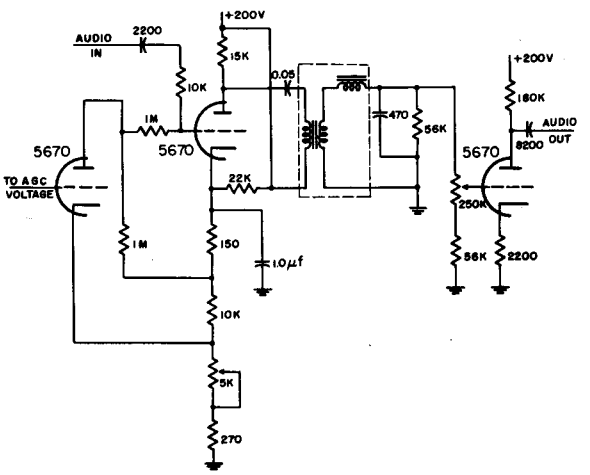
Key	Tube type	μ	Circuit type	Feedback	Supply voltage
A	12AT7	60	R-C coupled	Cathode degeneration	+250v dc.
B	5670	35	Transformer	None	+200v dc.
C	5670	35	R-C coupled	Cathode degeneration	+150v dc.
D	14F7	70	R-C coupled	Cathode degeneration	+280v dc.
E	12AX7	100	R-C coupled	None	+250v dc.
F	12AX7	100	R-C coupled	None	+250v dc.



AUDIO VOLTAGE AMPLIFIER
Fig. 12-8



AUDIO VOLTAGE AMPLIFIER WITH SQUELCH
Fig. 12-9



AUDIO VOLTAGE AMPLIFIER WITH SQUELCH
Fig. 12-10

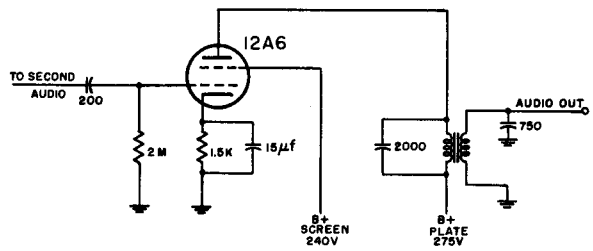
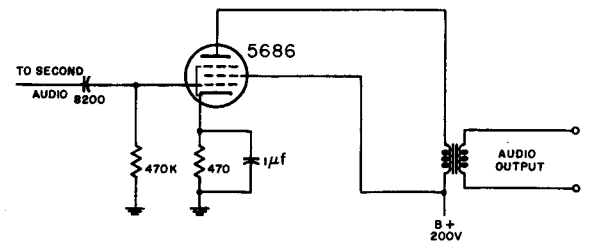


Fig. 12-11



AUDIO POWER AMPLIFIERS
Fig 12-12

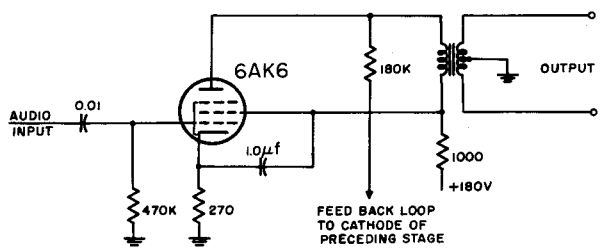
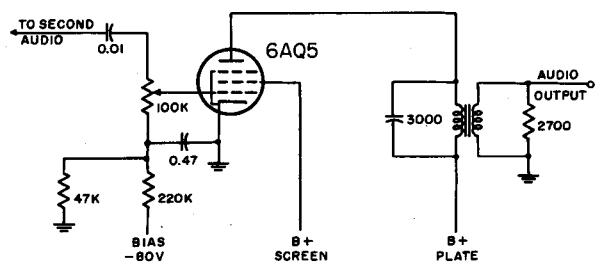


Fig. 12-13



AUDIO POWER AMPLIFIERS
Fig. 12-14

(c) *Audio Power Amplifier:* Following the voltage amplifier stage is the power stage which is usually designed to drive a line or a transducer. The examples studied were practically identical

in circuit configuration as shown in figures 12-11 through 12-16. All cases studied used a beam power pentode in the output stage. All but one example used cathode bias; the remaining one (fig. 12-14) used fixed bias. Figures 12-11, 12-14, 12-15, and 12-16 show the use of a capacitor across the primary of the output transformer to limit the high-frequency response of the transformer. The frequency range of the audio amplifier was in all cases from 300 to 4000cps. The output impedance of the stage was either 300 or 600Ω. The output transformer is a controlling factor in determining the frequency response of these amplifier systems. Table 12-2 shows the comparison between the different circuits studied. In each case the maximum power output was two watts.

(d) *Automatic Gain Control:* In order to keep the output of a receiver relatively constant with a varying input signal, an automatic gain control is used. Four of the examples examined had such a system (figs. 12-17, 12-18, 12-19, and 12-21). Three of the examples employed a dc amplifier

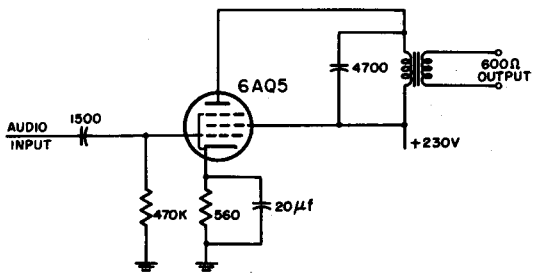
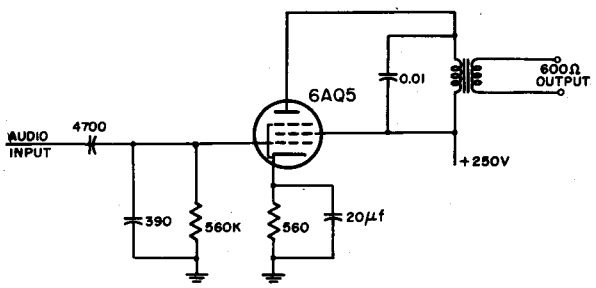


Fig. 12-15



AUDIO POWER AMPLIFIERS

Fig. 12-16

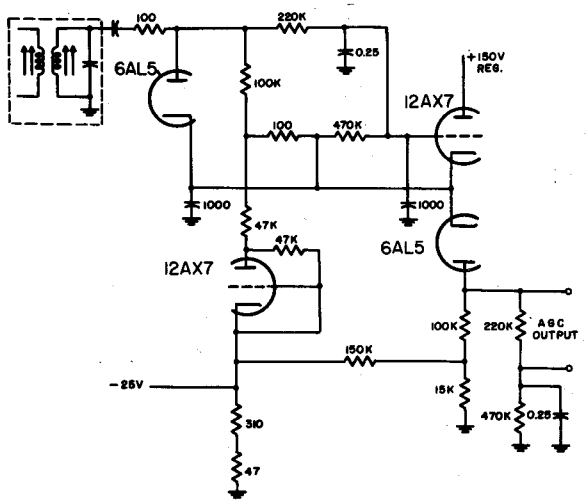


Fig. 12-17 AUTOMATIC GAIN CONTROL

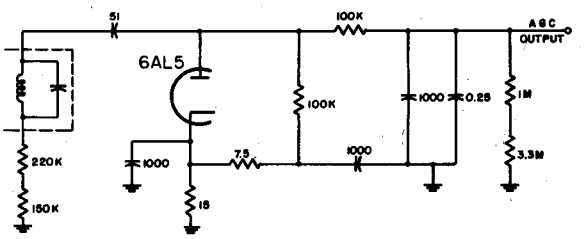


Fig. 12-18 AUTOMATIC GAIN CONTROL

TABLE 12-2—*Summary of Power Amplifier Characteristics*

Key	Tube type	Type of bias	Maximum power output	Output impedance	Supply voltage
A	6AQ5	Fixed	2 watts	300Ω	+250v dc.
B	5686	Cathode	2 watts	600Ω	+200v dc.
C					
D	12A6	Cathode	2 watts	300Ω	+280v dc.
E	6AQ5	Cathode	2 watts	600Ω	+230v dc.
F	6AQ5	Cathode	2 watts	600Ω	+230v dc.
G	6AK6	Cathode	2 watts	300Ω	+180v dc.

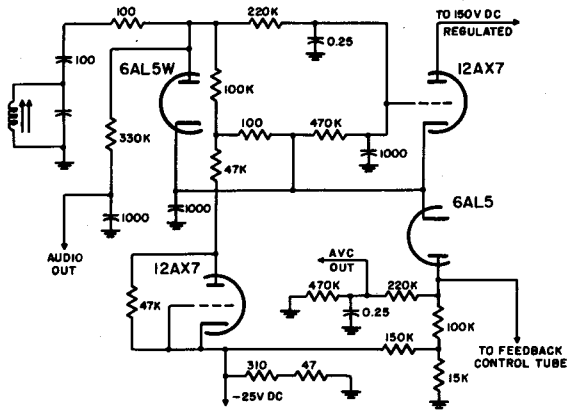


Fig. 12-19 AUTOMATIC GAIN CONTROL

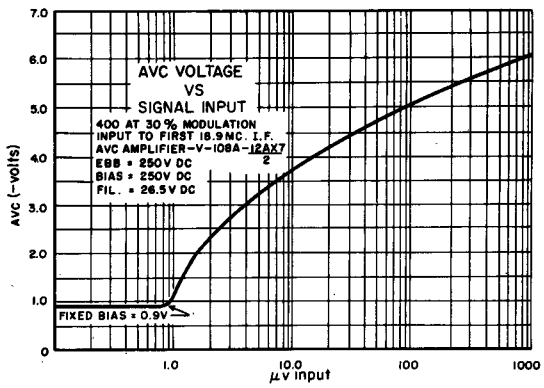


Fig. 12-20 AGC CHARACTERISTIC

in the agc circuit to obtain "amplified agc" (figs. 12-17, 12-19, and 12-21). The 12AX7 was the tube most used in the amplifier stage and the 6AL5 was the diode most used in the agc detector circuits. Figure 12-21 shows a diode-connected triode used as a detector. The circuit in each case was practically the same except for things peculiar to the separate circuits. A big disadvantage of this circuit is that when the plate current of the dc amplifier diminishes, the bias voltage appearing at the cathode of the dc amplifier increases the agc output. This biases the controlled stages to a point where their gain is low. A change in transconductance of the tube effects the agc output in the same manner as is shown in figure 12-22. Figures 12-20 and 12-22 also show agc characteristics. Figure 12-23 shows the effect on the agc voltage in one of the receivers as tubes of varied transconductance were inserted.

PC 63, an automatic gain control circuit, was designed to overcome these problems.

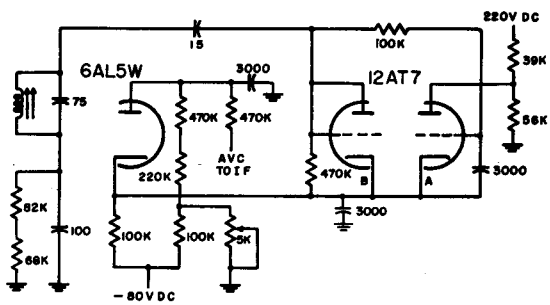


Fig. 12-21 AUTOMATIC GAIN CONTROL

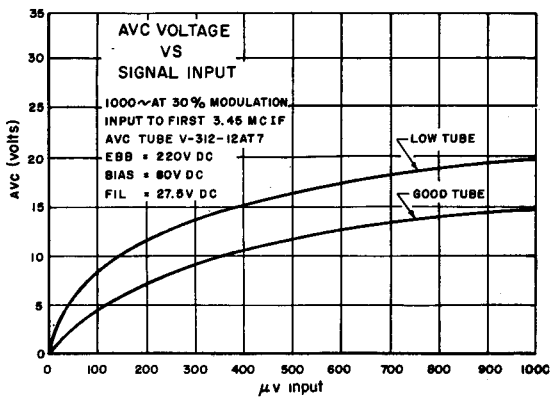


Fig. 12-22 AGC CHARACTERISTIC

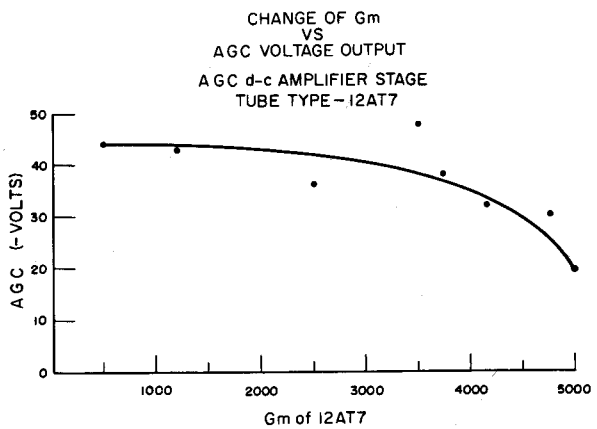


Fig. 12-23 AGC CHARACTERISTIC

(e) *Broadband Cathode Followers:* Broadband cathode followers are employed when modulation frequencies of 70 to 20,000cps are to be encountered. Two examples of these circuits are shown in figures 12-24 and 12-25. Cathode followers are discussed in detail in section 3 and section 11.

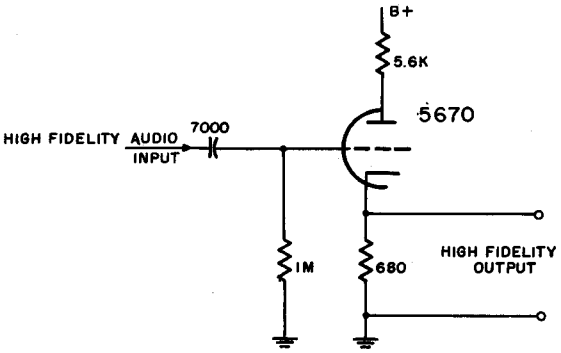
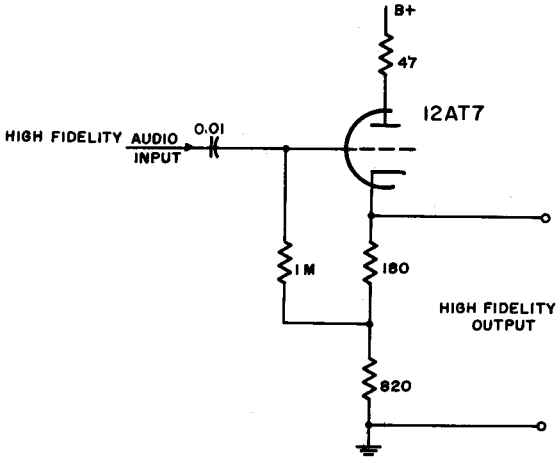


Fig. 12-24



WIDE BAND CATHODE FOLLOWER

Fig. 12-25

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13. AUTOMATIC FREQUENCY CONTROL

Automatic frequency control is necessary in most radar systems for two reasons: the transmitter and local oscillator frequencies cannot be adequately stabilized against changes in temperature and pressure, and the transmitter frequency is subject to pulling as the antenna rotates. A difference-frequency system is generally used to effect automatic frequency control, because maintenance of a constant difference between the transmitter and the local oscillator signals is the principal requirement rather than maintenance of either signal at an absolute frequency. With the transmitter signal as reference, the local oscillator frequency is controlled to maintain the intermediate frequency.

The usual afc system consists of:

(1) A mixer to which samples of the transmitter and local oscillator signals are fed.

(2) IF stages to amplify the difference-frequency component of the mixer output.

(3) A discriminator whose output is proportional in amplitude to the departure of the difference-frequency from the intermediate frequency and whose output polarity indicates the direction of that departure.

(4) A video amplifier to raise the level of the discriminator output to the level required to operate the control circuit.

(5) A control circuit which changes the local oscillator frequency in a direction to reduce the error signal.

Figure 53–1, p. 53–5 of the Preferred Circuits Manual, shows the location of these circuits relative to the receiver and transmitter. The design of afc systems is treated extensively in the literature.[1]

13.1 *Results of Survey:* In the preparation of PC 53, 12 airborne radar systems of recent design operating in the 3 and 10 centimeter bands were examined. The details of their afc systems are set forth in table N13–1. As a result of this survey it was concluded that a simple afc system of either the thyratron or diode-phantastron control type would satisfy the afc requirements in the majority of the systems. Such a circuit could be used in systems A through H, table N13–1, and could probably be used to replace the two Whitford circuits that were modified to obtain electronic (repeller) control of the klystron, systems I and J. The principal advantage of the Whitford circuit, systems K and L, is its ability to discriminate against the wrong sideband. When the thyratron and diode-phantastron control circuits are used, it is necessary to adjust the afc circuit so that the local oscillator frequency cannot pass through the wrong sideband, or improper locking will result. (See section 13.3 (b).)

The performance characteristics of the eight simple afc systems are listed in table N13–2. These characteristics form the basis for the input and output requirements of the preferred circuit, PC 53. It is evident from the table that the performance requirements do not govern the choice of circuit types; for instance, in system F a Foster-Seeley discriminator and a thyratron control circuit are used, while in system G, which meets approximately the same input and output requirements, a Weiss discriminator and diode-phantastron control circuit are used. The Weiss discriminator was selected for PC 53 because wide bandwidths are easily obtained without the use of a special transformer. Diode-phantastron control is used because it is generally more satisfactory than thyratron control. (See section 13.2 (d).)

13.2 *Examples of Circuits in Current Use:* A detailed examination of the afc systems shows that the differences are minor.

(*a*) IF amplifier: Although the ~~mixers and~~ IF circuits are not illustrated, their similarity is indicated in table N13–1. Note that a 30 mc intermediate frequency is used in most of the systems listed. The 6AK5, or its equivalent, the 5654/6AK5W, is almost universally used as an IF amplifier, the number of stages depending on the amplification and bandwidth required. The bandwidth of the afc IF is determined by the pulse width of the system,

[1] R. V. Pound and E. Durand, *Microwave Mixers, Rad. Lab. Series*, vol. 16, McGraw-Hill, New York, N. Y., 1948, Chap. 7. S. N. Van Voorhis, ed., *Microwave Receivers, Rad. Lab. Series*, vol. 23, McGraw-Hill, New York, N. Y., 1948, Chap. 3.

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TABLE N13–1—*Comparison of AFC Circuits*

System	Figure	Input mv	Input coupling	Minimum pulse width μsec.	AFC IF				Radar receiver bandwidth mc	Discriminator		Video amplifier	Control circuit
					Number of stages	Tube type	Center frequency mc	Bandwidth mc		Type	Peak separation mc		
A		400	T	0.5	1	5654	30	10	6	Weiss	4	Pentode	Thyratron.
B	13–2(b)	---	Transformer	0.67	1	5654	30	4	1.2	Weiss	2	Pentode and cathode follower.	Diode-phantastron.
C	13–2(a)	---	Transformer	0.5	3	5702	30	4	2	Weiss	4	Pentode and Triode.	Diode-phantastron.
D		---	L	0.5	3	6AK5	60	5	5	Weiss	3	Pentode	Diode-phantastron.
E	13–1(a)	---	π	0.75	1	6AK5	60	5	3	Weiss	3	Pentode	Thyratron.
F	13–1(b)	35	Transformer	1.8	2	5654	30	2	1.2	Foster-Seeley.	4	Triode	Thyratron.
G	13–2(c)	100	Transformer	0.5	*3	6AK5	30	9	4	Weiss	3.5	Pentode	Diode-phantastron.
H		---	Transformer	0.5	1	5654	30	4	3.5	Weiss	4	Triode	Diode-phantastron.
I		---	Transformer	0.5	2	6AK5	30	8	6.5	Weiss	2.5	Modified Whitford	
J		---		0.5	2	5654	30	----	4.5	Weiss	2.5	Modified Whitford	
K	13–3	---		0.5	2	5654	30	----	5	Weiss	4	Whitford	
L		---		0.4	2	5654	30	----	5.5	Foster-Seeley.	---	Whitford	

*Stagger Tuned

TABLE N13–2.—*Summary of AFC Circuit Performance*

System	Input				Output			
	Pulse width μsec.	Duty factor $\times 10^{-4}$	Frequency mc/sec.	Level mv	Sweep V	Sweep rate cps	Control range dc volts	
	Min. *Max.*	*Min.* *Max.*					*Min.*	*Max.*
A	0.5	4	30	400	40	0.2	−55	−140
B	0.67 2.0	2 6	30	----------	60	10	−45	−165
C	0.5 3.2	1.5 9	30	----------	40	0.2	−150	−250
D	0.5 5.0	4 10	60	----------	75	2	−100	−210
E	0.75 5.0	6 10	60	----------	40	2	−55	−140
F	1.8	8	30	35	40	1	−115	−200
G	0.5 3.25	4 10	30	100	40	3	−115	−200
H	0.5	10	30	----------	40	10 to 50	−110	−200

and is generally made wider than that of the radar IF to prevent "bottlenecking" the discriminator.[2]

To minimize hum in the discriminator, the signal level at the output of the IF amplifier must be 1 volt or more. Not all of this amplification must be realized in the IF stages. Because the equivalent noise of the crystal is low compared to the signal levels involved, the coupling network can be designed for maximum power gain. In addition, the over-all amplification of the afc system includes the amplification of the video amplifier. In any comparison of two circuits of the same bandwidth, it should be noted that low amplification in the IF amplifier is generally compensated by higher amplification in the video amplifier.

(*b*) Discriminator: As indicated by table N13–1, the Weiss discriminator (fig. N13–1 (a), p. N13–4) is more popular than other types. It eliminates the need for a special IF transformer and for large bandwidths; it is easier to adjust than the Foster-Seeley circuit of figure N13–1 (b). The differences in component values are necessary because of the differences in bandwidth requirements and center frequencies. In figure N13–2 (a), p. N13–6, the discriminator is biased about 18 volts positive to reduce the hum pickup from the heaters.[3]

The output of any of the discriminator circuits is a series of pulses whose amplitudes vary from zero at crossover to a maximum of 0.5 to 2 volts at the frequency of maximum response, with the envelope of the peaks following the familiar amplitude-versus-frequency discriminator characteristic. The pulse shape depends on the video response of the RC network connected to the discriminator output; the polarity may be either positive or negative depending on whether the incoming signal frequency is above or below the crossover frequency. In any of the circuits, the polarity of the output for a given frequency deviation from the crossover can be reversed by reversing the diodes; in the Weiss discriminator the polarity can also be reversed by interchanging the two tuning capacitors.

(*c*) Video amplifier: A video amplifier is necessary to bring the signal level up to an amplitude that can be used by the control circuit. Since the requirements for the amplifier are mainly determined by the control circuit, the two will be discussed together in the following section.

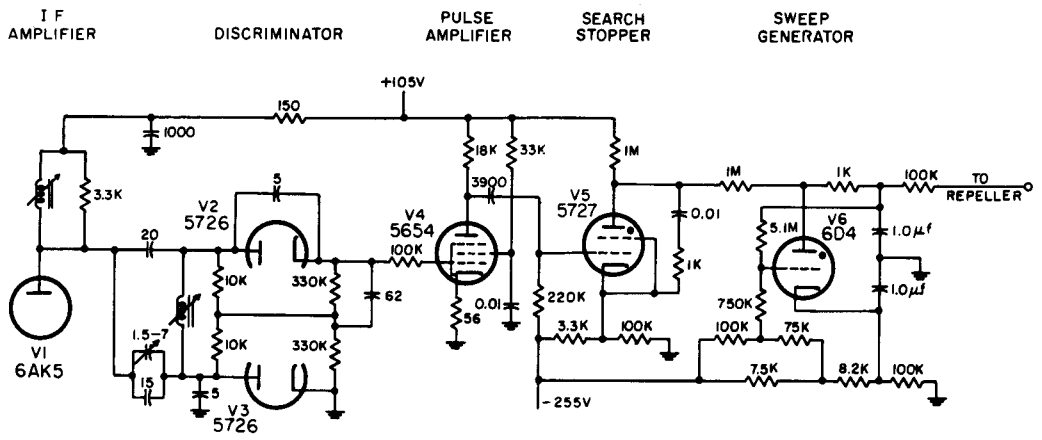
(*d*) Control circuit: The final link in the afc system is the control circuit which converts the error signal into a voltage capable of controlling the frequency of the local oscillator. In radar systems, a circuit capable of controlling the repeller voltage of a klystron is required. Because the drifts are likely to be large compared with the receiver bandwidth, a hunting system is used, that is, the local oscillator is swept over a large frequency range to find the correct operating point. Once the desired crossover frequency is reached, the circuit must stop sweeping and maintain the correct difference frequency between local oscillator and transmitter.

(1) Thyratron control circuits: The circuits of figure N13–1 are examples of thyratron control circuits. Two thyratron relaxation oscillators are employed. The sweep generator varies the klystron repeller voltage between the half-power points at a relatively slow rate when no signal is received from the discriminator. In the absence of positive input to the grid, the search stopper is biased to cutoff for any plate voltage encountered during the slow sweep. If the transmitter is operating, output pulses will be received from the discriminator when the local oscillator and the transmitter frequency differ by approximately the intermediate frequency. The discriminator output is amplified and inverted by the video amplifier; the slow sweep is arrested when the pulse input to the ~~2D21~~ becomes positive and of sufficient amplitude to overcome the fixed bias.

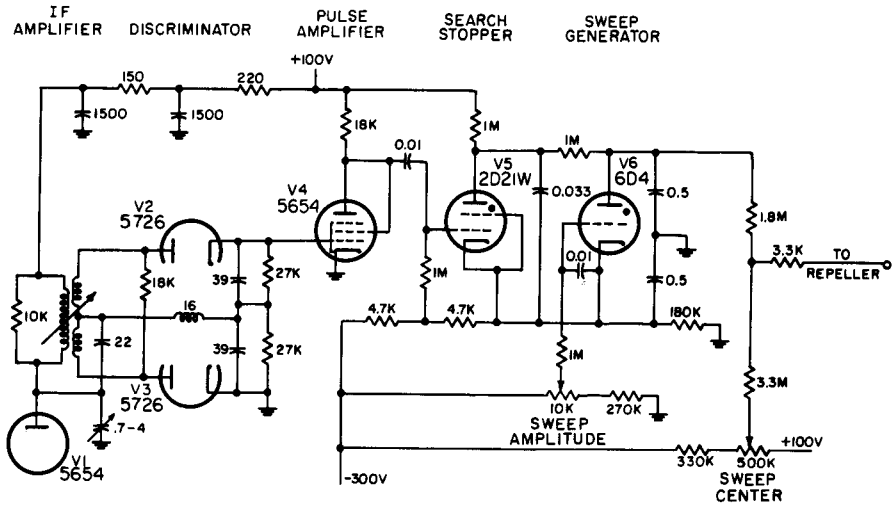
Although the plate voltage of the ~~2D21~~ is varied continuously by the slow sweep generator during search, the grid voltage at which it fires is nearly independent of the plate voltage over this range. When positive pulses of an amplitude sufficient to overcome the fixed bias are received from the video amplifier, the ~~2D21~~ fires, causing its plate voltage to drop to within 10 or 15 volts of the cathode potential. Under

[2] Van Voorhis, *op. cit.*, p. 49.
[3] Pound and Durand, *op. cit.*, p. 311.

* Search Stopper



(a) SYSTEM E



(b) SYSTEM F

Figure N13–1.—Examples of AFC circuits using thyratron control

these conditions, the plate voltage of the 6D4 never becomes sufficiently positive to permit it to conduct, and the slow sweep stops.

During lock-on, the repeller voltage is varied by changing the period of the sawtooth generated by the search stopper. The time constant of the circuit is adjusted so that the * ~~2D21~~ fires on every third to fourth transmitter pulse when the local oscillator frequency is at crossover. If the intermediate frequency changes in a direction to increase the amplitude of the discriminator output, the search stopper fires more frequently, resulting in a more negative repeller voltage. If the discriminator output becomes smaller, the search stopper fires less frequently, causing the repeller voltage to become less negative. In either case, if the search stopper loses control, the slow sweep will recommence and continue until the local oscillator again locks properly. The polarity of the discriminator output must be such that the repeller voltage changes are in the proper direction to correct the local oscillator frequency.

* Search Stopper

Although the sawtooth produced by the search stopper during lock-on is filtered by the RC network in the plate circuit, there is still a small amount of frequency modulation of the local oscillator due to ripple. Because the frequency and amplitude of the search stopper output vary during lock-on, the ripple is not constant over the range. The factors which govern the ripple voltage are the same as those which determine the rate at which the afc will follow the signal, and the one cannot be reduced without reducing the other.

A further disadvantage of the gas-tube control circuit is its dependence on tube characteristics, which are less uniform for thyratrons than for vacuum tubes; for instance, for a fixed bias of the magnitude used in the sweep generator circuit of figure N13–1 (a), the 6D4 may start to conduct at any plate voltage within a 100-volt range and still be acceptable under MIL specifications. Without correction, this might result in a 50% change in the sweep range when the 6D4 is replaced. Correction is provided by the resistive network between grid and plate which introduces negative feedback to minimize the spread in firing potential. In the sweep generator of figure N13–1 (b), the compensation is in the form of a bias adjustment which may be reset when the 6D4 is changed to bring the firing potential to the desired level.

The amplification of the video stage is not critical, because the gas-tube circuit operates on the frequency control principle. The minimum amplitude of the signal at the output of the video amplifier is determined by the voltage required to fire the search stopper and cause lock-on at the correct frequency. An upward limit to the over-all amplification of the system is set by the need to prevent locking on harmonics when the mixer output is a subharmonic of the intermediate frequency. The second harmonic, which is most likely to cause trouble when single crystals are used, is generally at least 20 db below the desired signal.

(2) Diode-phantastron circuit: The diode-phantastron circuit, examples of which are shown in figure N13–2, was used in almost one-half of the systems surveyed. The pentode is an astable phantastron during search and a dc amplifier during lock-on. The diode circuit acts as a search stopper to control the change from one type of operation to the other. When no signal is received from the discriminator, the diode is nonconducting, and astable phantastron operation results. The output waveforms are the same as those of the triggered phantastron, except that no triggering is required, and each cycle repeats as soon as the circuit has recovered from the preceding one. Since the output is connected to the klystron repeller through a voltage divider, the repeller is swept from a low to a high negative voltage. The values for the divider are chosen so that the klystron frequency is swept through the desired mode. The range set control is necessary to accommodate the variations among klystrons of the same type.

The plate voltage of the phantastron can be held at any point within the sweep range by supplying sufficient fixed bias to the grid. When the video amplifier output becomes positive, the diode will conduct during the pulses, and a negative voltage will be built up at the phantastron grid. The circuit is adjusted so that the bias will be sufficient to stop the phantastron near the middle of its sweep when the correct crossover frequency is reached. If now the transmitter or local oscillator frequency changes in a direction to decrease the negative discriminator output, the phantastron bias will decrease, and the proper IF will be restored by the increase in negative repeller voltage. If a frequency shift causes an increase in the negative discriminator output, the phantastron bias will increase, the repeller voltage will become less negative, and the intermediate frequency will be restored to its proper value.

During lock-on the double integration of the incoming pulses by the RC circuit in the search stopper and by the phantastron itself minimizes the ripple in the output. An incidental advantage is that the system will not start to search abruptly if the transmitter signal is momentarily interrupted because the diode capacitor must discharge before the sweep can commence. Thus, the afc circuit can recover the signal after momentary interruptions without resort to sweeping. This can also be a disadvantage, however, since the response to an

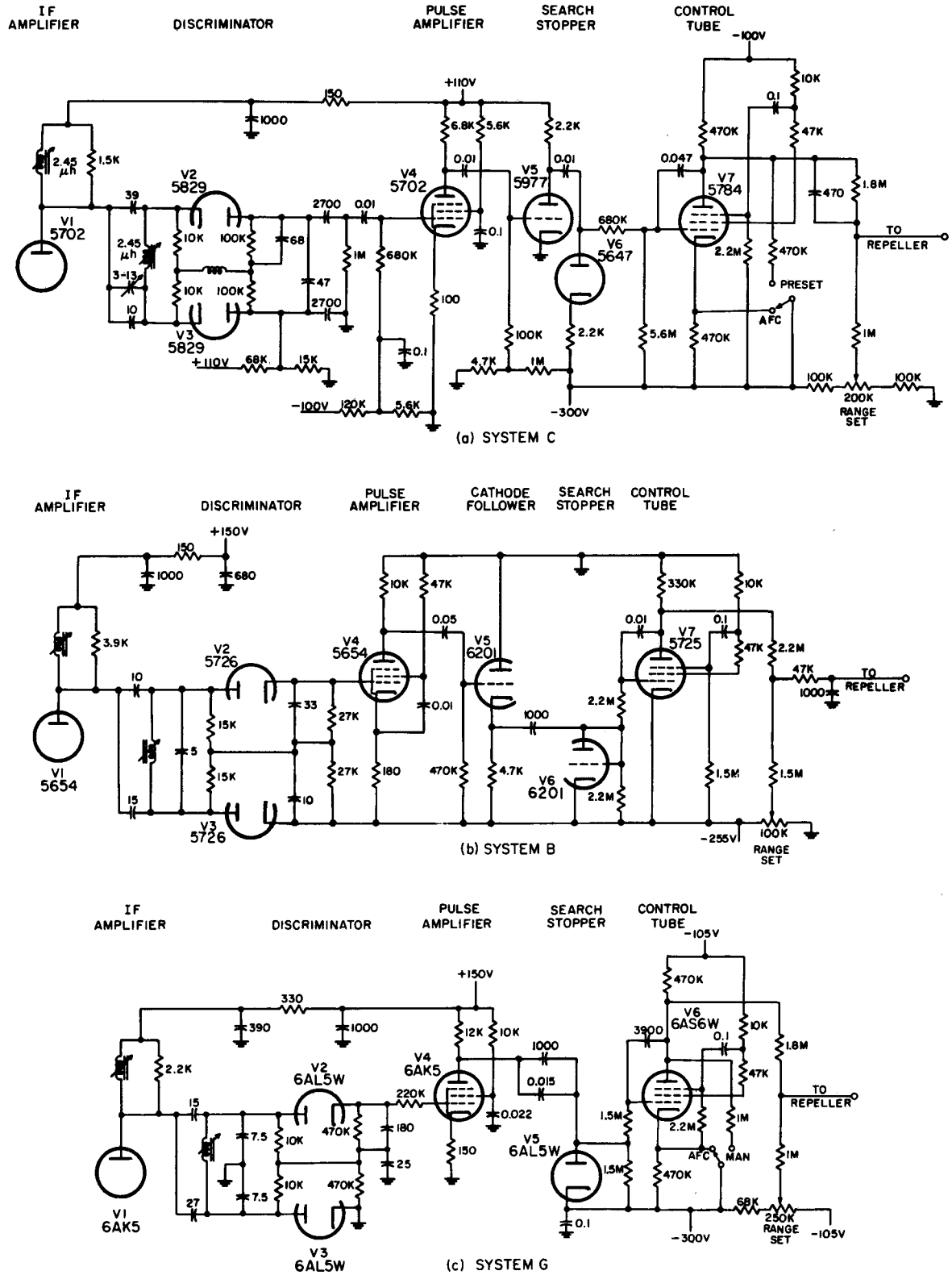


Figure N13–2.—Examples of AFC circuits using diode-phantastron control

input signal change which decreases the phantastron bias is also delayed by the time required for the search stopper capacitor to discharge. The holding properties are therefore obtained at the expense of a decrease in follow rate, and a compromise between the two must be reached.

Since the sweep rate is the maximum rate at which the phantastron output can follow signal changes which decrease the bias, rapid follow rates necessitate the use of high sweep rates. The maximum sweep rate is obtained when the number of pulses which reach the search stopper during the time that the signal sweeps through the discriminator peak is just sufficient to assure locking. A video amplifier is needed which is capable of transferring as much charge as possible to the diode-coupling capacitor during the transmitter pulse so that the required phantastron bias can be developed in as few pulses as possible. The number of pulses required to reach an equilibrium dc level across the phantastron grid return varies directly with the output impedance of the amplifier, and inversely with the pulse width, prf, and search stopper load resistance. The lower the output impedance of the video amplifier and the higher the resistance of search stopper load, the closer the dc bias developed will approach the no-load output voltage of the video amplifier. The effects of narrow pulse width and low prf can be offset by low output impedance and high amplification in the video stage. All of the video amplifiers shown in figure N13–2 will operate satisfactorily in the systems for which they were designed. Of the circuits shown, however, the operation of the pentode-cathode follower system of figure N13–2 (b) is the least affected by change of prf and pulse width. The low output impedance of the cathode follower makes it possible to realize about one-half of the open circuit output voltage of the video amplifier as dc bias on the phantastron, and the low charging time constant permits generation of the full bias in a few pulses.

Other advantages of the diode-phantastron circuit are:

(a) The operation is nearly independent of the tube characteristics; the circuit will work well with any tube of the specified type.

(b) Slow sweeps can be obtained using small capacitors. For example, the circuits of figures N13–1 (b) and N13–2 (c) each sweep the repeller voltage through a 40-volt range. In the thyratron circuit (fig. N13–1 (b)), a 2MΩ resistor and a 0.25 μf capacitor are used to sweep the output voltage through its range once a second, while in the phantastron circuit (fig. N13–2 (c)), three times this sweep rate is obtained by use of an RC product that is about ~~one-fifth~~ one-fiftieth as large. (R=3MΩ and C=3900 μμf.)

(c) Tighter control of the local oscillator frequency is maintained during lock-on because the pentode acts essentially as a dc amplifier to furnish direct control of the klystron repeller. The diode phantastron is an amplitude control system, and every transmitter pulse is effective in furnishing information to the afc circuit.

(d) The resistances which determine the sweep rate are located in the grid circuit and can be made as high as necessary (within the limitations of the tube) without affecting the output impedance.

(3) Whitford circuit: A third type of control circuit is illustrated in figure N13–3. The Whitford circuit provides a wider sweep range than that of either the thyratron or diode-

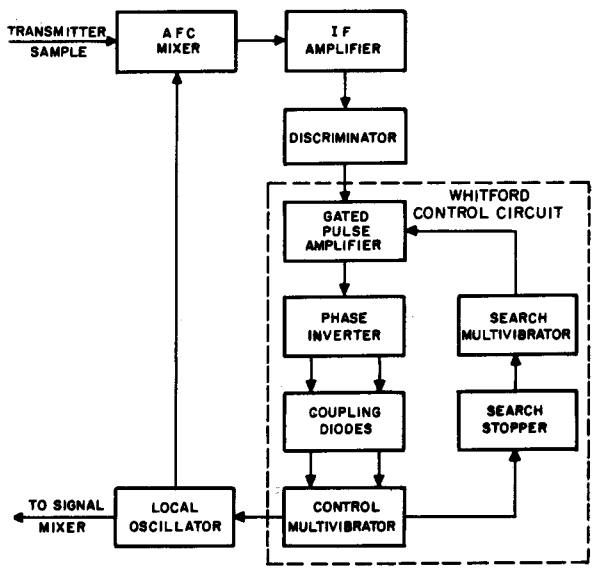


Figure N13–3.—Whitford AFC circuit

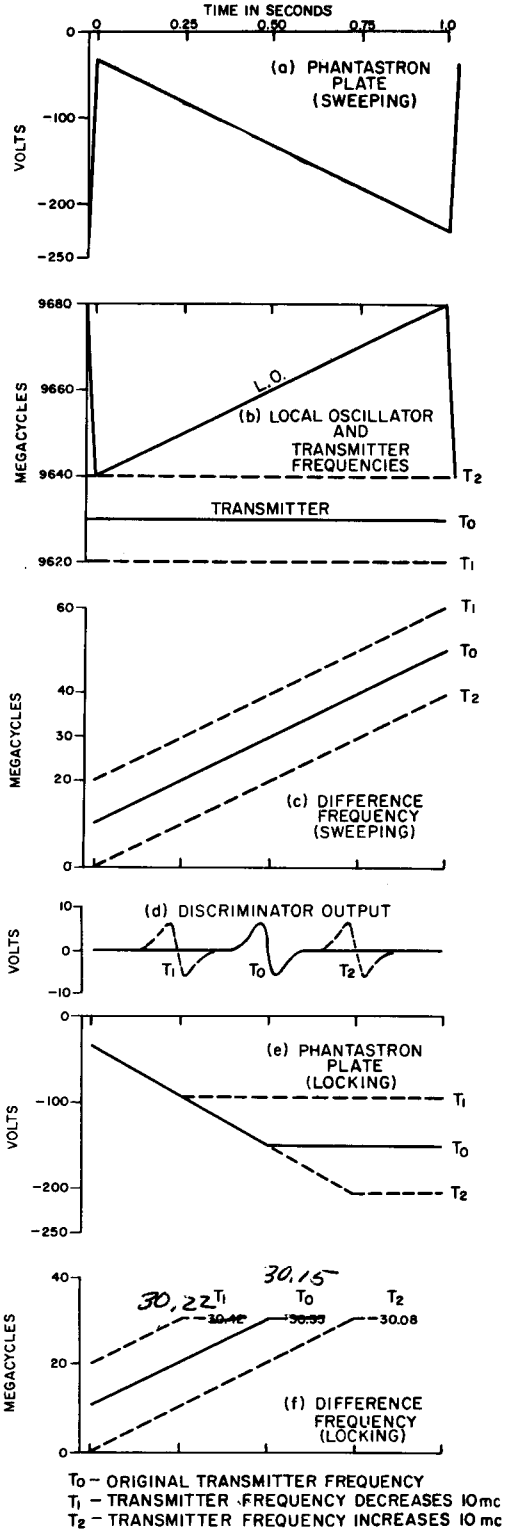
phantastron system, and is designed to prevent locking on the wrong sideband. It was developed for use with thermally-tuned klystrons,[4] but has also been used for electronic control (table N13–1, systems I and J). This circuit and other similar systems are more complex than the systems previously described.

13.3 *Additional Data for Automatic Frequency Control Circuit:* The following discussion of automatic frequency control applies to diode-phantastron control systems only.

(*a*) Operation of afc circuit: Figure N13–4 illustrates the operation of a typical diode-phantastron circuit. When the phantastron is free running, its plate voltage varies with time, as shown in figure N13–4 (a). (Straight lines have been used to simplify the illustration.) When the amplitude of this sweep voltage is reduced to 20 volts by a suitable divider and applied to the repeller of a typical 2K25, the local oscillator sweeps through a 40 mc range as shown in (b). If the transmitter is adjusted to operate at a lower frequency than that of the local oscillator, as indicated by solid line T_o, a difference frequency will be produced as shown by the solid line in (c), and an output from the discriminator will be obtained when the difference frequency is in the vicinity of 30 mc, as shown in (d).

The output of the discriminator consists of pulses of a width and repetition rate determined by the transmitter signal. This is because the transmitter signal is not continuous as the solid line in (b) seems to indicate, but consists of a series of pulses each a few microseconds wide recurring at a rate between 200 and 2000 pulses per second. The difference frequency produced by the mixing of the transmitter and local oscillator signals is therefore also pulsed rf. In the discriminator circuit, the rf is bypassed to ground leaving only the pulse modulation as output. Figure N13–4 (d) shows the variation of the peak amplitude of these pulses with change in input frequency.

The discriminator output is amplified by the video amplifier, integrated in the search stopper circuit, and applied as bias to the grid



To – ORIGINAL TRANSMITTER FREQUENCY
Ti – TRANSMITTER FREQUENCY DECREASES 10mc
T2 – TRANSMITTER FREQUENCY INCREASES 10 mc

Figure N13–4.—Operation of AFC circuit

[4] Pound and Durand, *op. cit.*, pp. 331–337; Van Voorhis, *op. cit.*, pp. 69–74.

of the phantastron. Provided the lock-on requirements are met, the sweeping of the phantastron will be interrupted and the phantastron plate voltage will become constant (fig. N13–4 (e)). As a result, the local oscillator frequency becomes stable at a frequency determined by the repeller voltage, and a difference frequency of approximately 30 mc is produced, as illustrated in figure N13–4 (f).

With the discriminator crossover adjusted for 30 mc, the system cannot lock at a difference frequency of exactly 30 mc, since the discriminator output at that frequency is zero, and no bias is developed at the phantastron grid. The 0.15 mc error in the illustration is the amount by which the difference frequency must exceed the crossover frequency (adjusted to 30 mc in this case) to produce sufficient bias to arrest the sweeping of the phantastron. The magnitude of this error is a function of the amplification of the feedback loop. Increasing the amplification to reduce the error also increases the possibility of locking improperly on crystal harmonics. If the 0.15 mc error is objectionable, a 30 mc difference frequency could be produced by adjusting the discriminator crossover for 29.85 mc.

If now the transmitter frequency shifts 10 mc (this may be a slow drift such as is caused by temperature changes or a rapid change produced by the pulling of the magnetron as the antenna rotates), the 30 mc difference frequency occurs at a different point in the sweep. Discriminator output is produced at T_1 or T_2 (fig. N13–4 (d)). As a result, the circuit stabilizes at a different phantastron plate voltage and a different local oscillator frequency, but at a difference frequency which is still approximately 30 mc above the transmitter frequency as shown in figure N13–4 (f). The action of the afc circuit has reduced the 10 mc change in transmitter frequency to a difference frequency change of only 0.07 mc.

For convenience, a change in transmitter frequency has been used to illustrate the operation of the circuit. In practice, with the local oscillator frequency adjusted for the correct 30 mc difference frequency near the center of its electronic tuning range and near the center of the phantastron sweep range, the difference frequency will be maintained in spite of drifts in either or both the transmitter and local oscillator frequencies. Notice also that the circuit is capable of maintaining a 30 mc difference frequency in spite of local oscillator or transmitter frequency changes several times as large as the peak separation of the discriminator output. In other words, although the sweeping feature is required to bring the circuit to the correct operating point when it is turned on, or after an interruption of one of the signals, the afc circuit can maintain the difference frequency over approximately the same range without resorting to sweeping once the correct operating point has been established. This is true provided the rate of change of frequency does not exceed the speed at which the circuit is capable of following these changes. This is largely determined by the time constants of the diode-phantastron control circuit.

(*b*) Wrong-sideband locking: For stable operation, the output voltage of the afc circuit must change the local oscillator frequency in a direction to counteract the change in difference frequency which produced the original voltage change. The discriminator can be connected for either direction of output voltage change relative to the input frequency. The correct discriminator connection is determined by the slope of the electronic tuning characteristic of the local oscillator and by the local oscillator frequency relative to the transmitter frequency. If the local oscillator frequency is higher than the transmitter frequency, the intermediate frequency varies directly with the local oscillator frequency (or inversely with the transmitter frequency), while the opposite is true if the local oscillator frequency is lower than the transmitter frequency. With a klystron local oscillator, the negative output voltage of the phantastron must decrease with an increase in intermediate frequency in the first case, but must increase with frequency in the second.

Figure N13–5 illustrates the input to the afc circuit and the discriminator output in a system with a 30 mc intermediate frequency and a local oscillator whose frequency range is centered at the transmitter frequency and whose electronic tuning range is ± 40 mc. Discriminator output

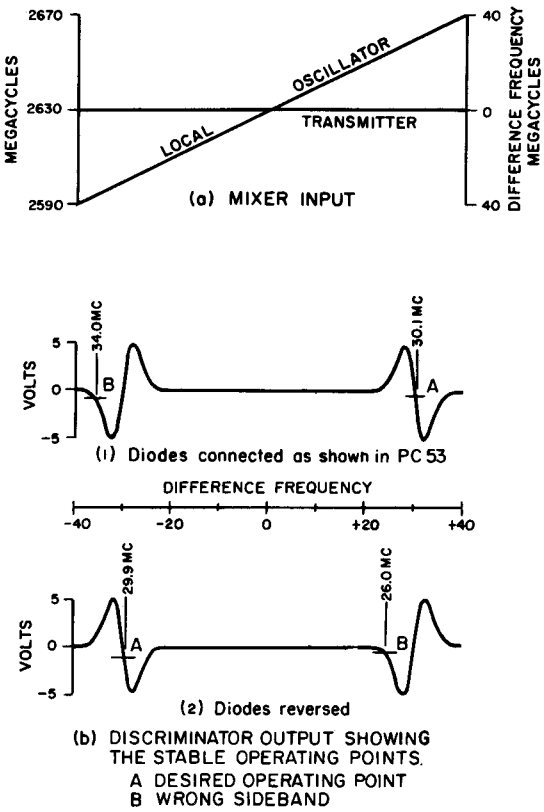


Figure N13–5.—AFC performance showing the results of locking on the wrong sideband

is obtained at frequencies approximately 30 mc higher and lower than the transmitter frequency (fig. N13–5 (b)), with the crossover at 30 mc in either case. If the diode-phantastron circuit is used to control a reflex klystron, stable operation is obtained when the discriminator output is negative and has a negative slope. Examination of figure N13–5 (b) shows that there are two regions in which this condition is satisfied.

If the discriminator diodes are connected to produce negative output at frequencies greater than 30 mc (this is the connection used in PC 53), the correct stable operating point is obtained when the local oscillator frequency is 30 mc higher than the transmitter frequency (fig. N13–5 (b)(1)). If the local oscillator is allowed to sweep through the frequency which is about 34 mc lower than the transmitter frequency, the circuit will also lock at a stable operating point, but the operation of the radar receiver will be seriously impaired. If the discriminator diodes are reversed, the discriminator output will be negative at frequencies less than 30 mc, and the correct stable operating point will be obtained when the local oscillator is operating at a frequency 30 mc lower than the transmitter. PC 53 can be wired to lock correctly on either side of the transmitter frequency, but the local oscillator sweep must be centered so that there is no possibility of locking on the wrong side. Some rejection of harmonics can be obtained by operating the local oscillator at a higher frequency than the transmitter.

14. HIGH VOLTAGE CRT POWER SUPPLIES

The final anodes of cathode-ray tubes require high-voltage low-current supplies. The supplies in common use fall into two general categories: line-voltage step-up transformer and self-excited oscillator types.

In the oscillator types the generated voltage is either sinusoidal or square wave in form, and the frequencies range from below 1 kc to above 100 kc. Rectifier configurations of the half-wave and the full-wave doubler types predominate. The filter networks are determined by their output impedance and by the driving source frequency. In most instances, the need to present a reasonable value of output impedance will predominate over the need to reduce the source frequency ripple component in the output.

A 400-cycle line-voltage operated supply can be made in a size small enough to be satisfactory. In general, the chief disadvantage of a line-voltage operated unit lies in the lack of a source of regulated voltage; this, combined with the greater physical size and somewhat greater danger to personnel, makes the self-excited oscillator preferable.

The output of a self-excited oscillator at a given current load can be kept as constant as the regulated dc source supplying it. Since dc voltages regulated to within $\pm 1\%$ are available in most equipment, this presents no problem. Electronic means for regulation of the output impedance or reduction of output ripple can be more readily applied to the self-excited oscillator supply than to the line-voltage operated unit whose range of input variation is much greater.

14.1 *Examples of Circuits in Use:* Thirteen high-voltage supplies for use with electromagnetic deflection cathode-ray tubes were surveyed. The electrostatic tubes found in current equipment require supplies that are too specialized for standardization. Of the supplies surveyed, line-voltage transformers were used in three, audio oscillators were used in nine, and an rf oscillator was used in one. Vacuum tubes were used in all oscillators.

Two supplies, one providing 3.6 kv and the other 14 kv, were used to power a special-purpose dark-trace tube. The accelerating voltage of the other eleven supplies ranged from 4.8 kv for a 5-inch tube to 10 kv for a 12-inch tube. Seven of these supplies were in the range of 5.9 to 8 kv, with 7 kv being both the mean and the voltage that appeared most often in this group. The magnitude of the screen grid voltages for the cathode-ray tubes ranged from 220 to 400 volts, 400 volts being the most common value.

Examples of line-voltage transformer type supplies are illustrated in figures 14–1, 14–2, and 14–3. The circuit of figure

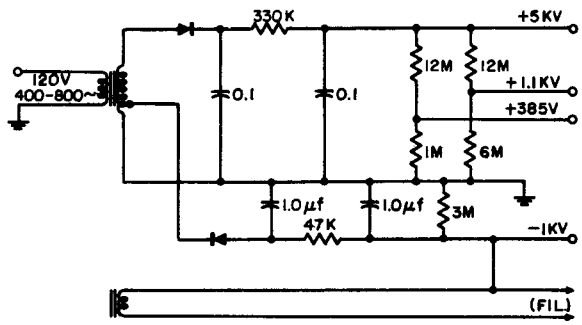


Figure N14–1—Line-voltage transformer type supply

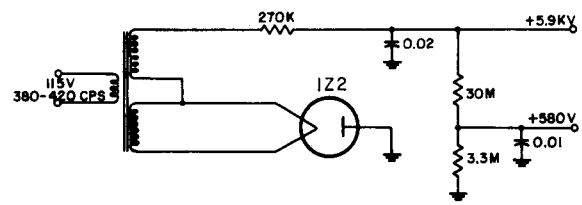


Figure N14–2—Line-voltage transformer type supply

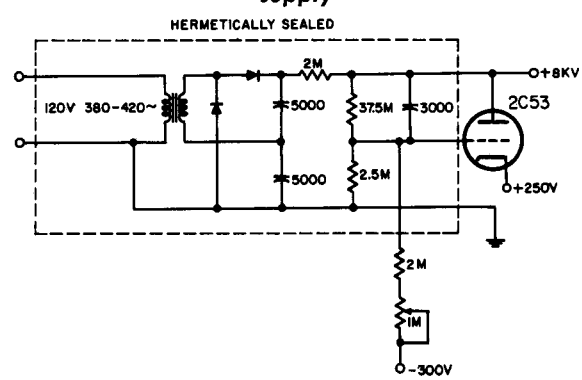


Figure N14–3—Line-voltage transformer type supply

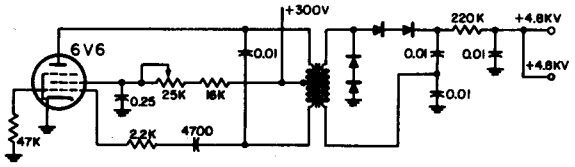


Figure N14–4—Pentode audio oscillator type supply

N14–1 supplies the voltage for an electromagnetic deflection tube, and through taps on the high-voltage output divider, also supplies the voltages required by an associated electrostatic deflection A-scope indicator. The circuit of figure N14–2 has an output capacitor of 0.02 μf, which is small compared with the two 0.1 μf units used in the circuit of figure N14–1. In both circuits the line voltage is unregulated, resulting in a large output voltage variation. In the circuit of figure N14–3, a vacuum tube is connected in parallel with the output terminals to provide voltage regulation for overcoming the effects of changing line voltage. The regulator also improves the output ripple and output impedance characteristics of the supply. This unit has been designed to supply power to several magnetically deflected cathode-ray tubes.

The circuit of figure N14–4 is from one of the earliest equipments in which audio-frequency sine-wave oscillators were used as power sources. The filter capacitors are significantly smaller electrically than those in the simple line-transformer units.

The circuits of figures N14–5 through N14–8 are examples of pentode audio oscillators taken from recent production. The high-voltage transformer, rectifier, and filter components of each unit are hermetically sealed in a metal

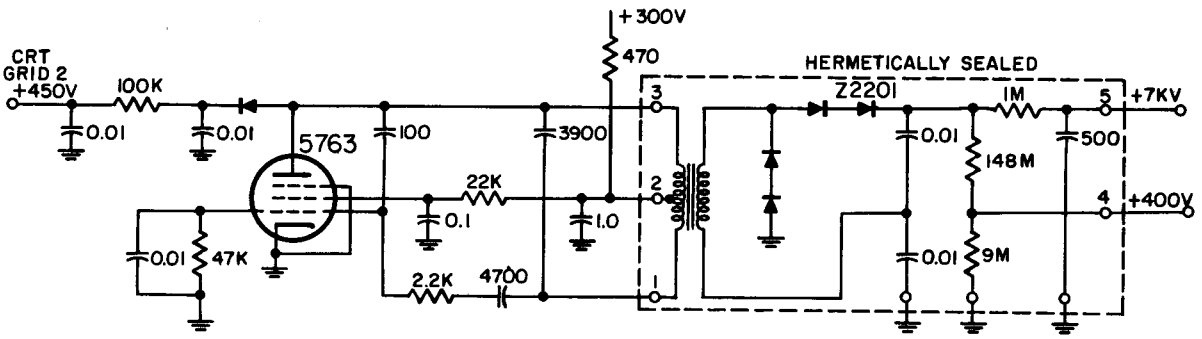


Figure N14–5—Pentode audio oscillator type supply

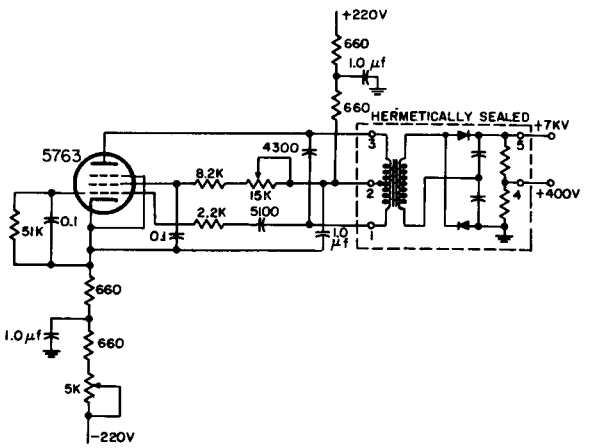


Figure N14–6—Pentode audio oscillator type supply

container. Any of the sealed units may be used with any of the circuits with negligible differences in output characteristics.

Figure N14–9 is an example of a pentode audio oscillator similar to the previously described oscillators in all respects but voltage output. The hermetically sealed container does not differ appreciably either in size or weight from the previously noted sealed containers, one of which, therefore, could have been used in the supply shown in figure N14–9, with only slight circuit modification being required. This would have eliminated the necessity of carrying two different hermetically sealed units as equipment spares, since the sealed unit of figure N14–9 and one of the

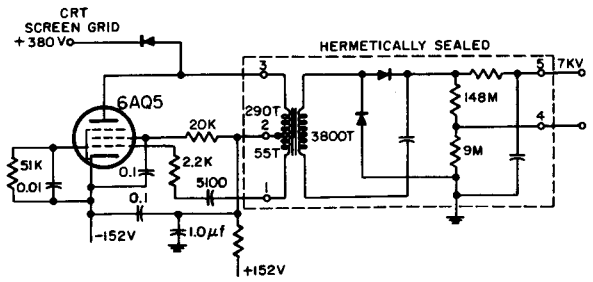


Figure N14–7—Pentode audio oscillator type supply

sealed units noted above were used in the same equipment.

Figure N14–10 is the only example of an rf oscillator type of power supply. It is also the only example of a supply having an associated regulator that controls the oscillator output. The equipments containing this circuit and the circuit of figure N14–4 have been in service for approximately the same length of time. The higher output impedance (before adding the

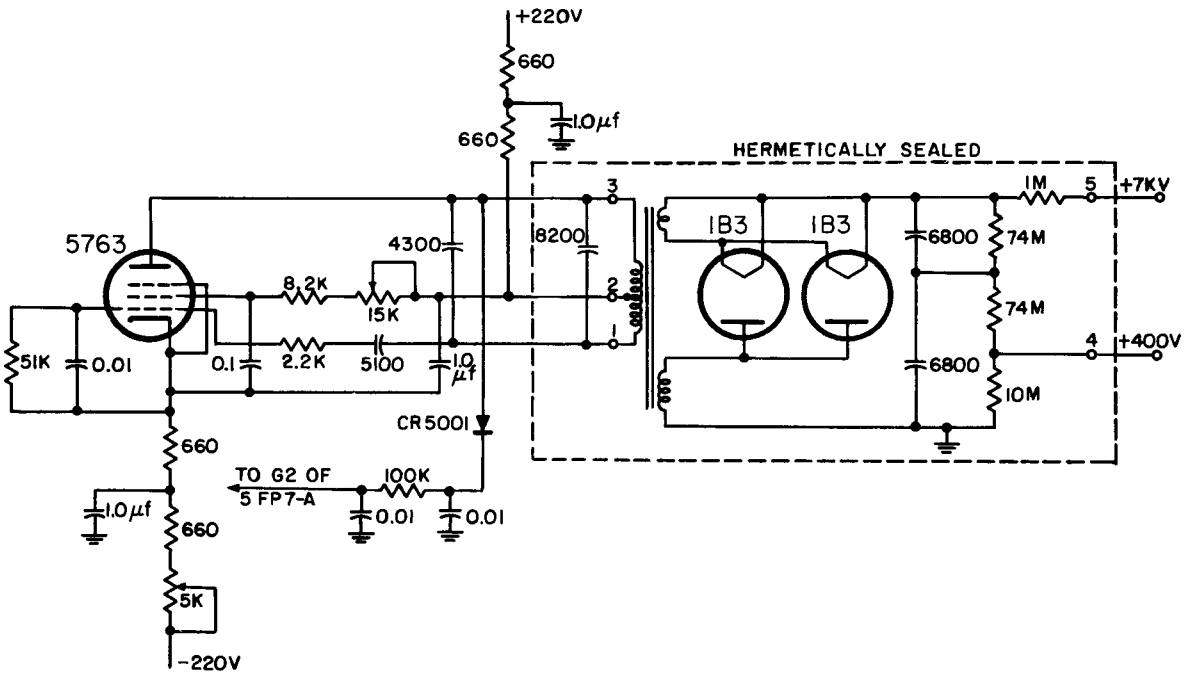


Figure N14–8—Pentode audio oscillator type supply

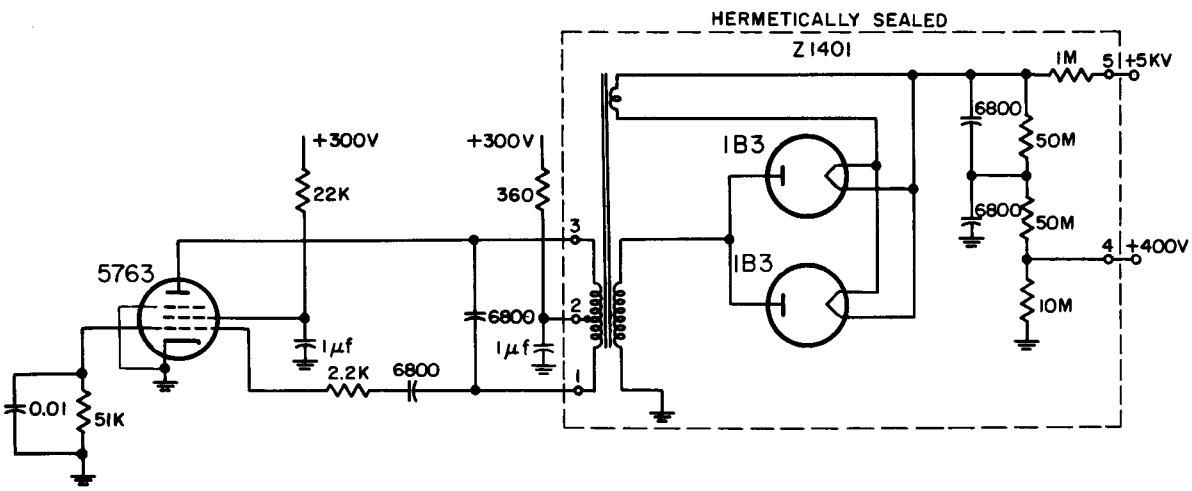


Figure N14–9—Pentode audio oscillator type supply

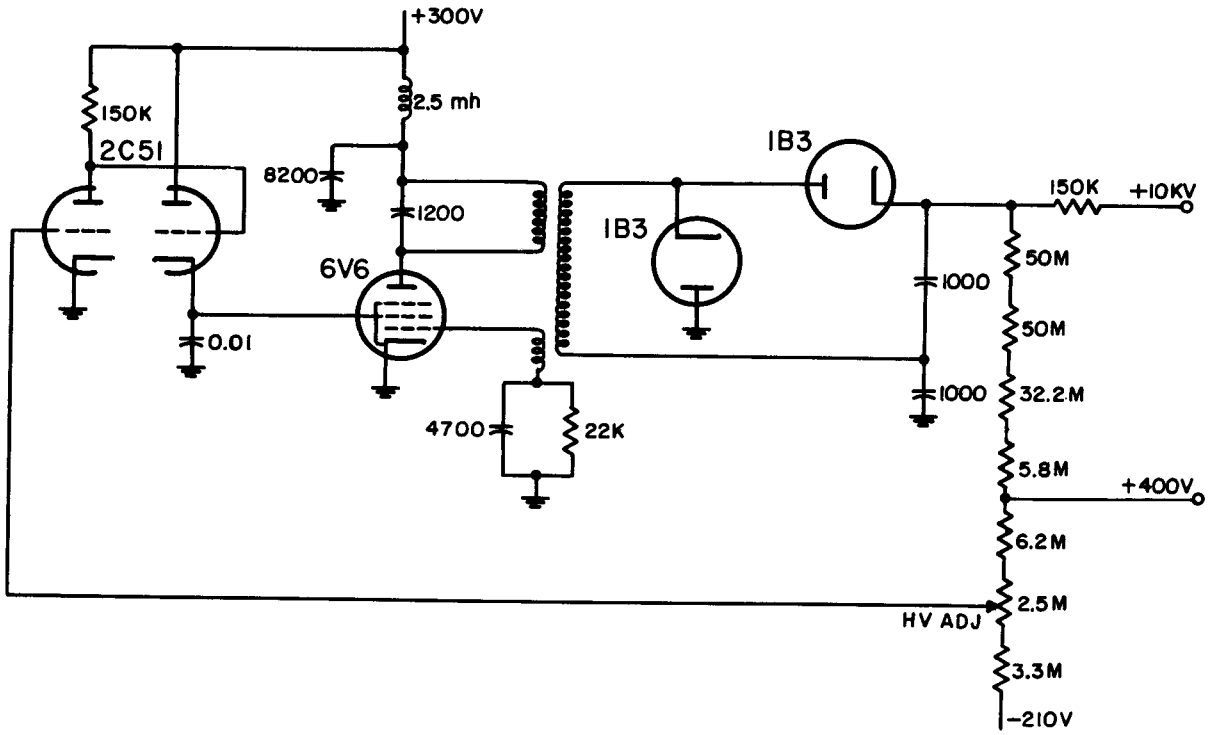


Figure N14–10—Pentode rf oscillator type supply with twin-triode voltage regulator

regulator) of this type of unit, plus the added problem of higher frequency radiation, makes it less desirable than the audio-frequency type.

The circuit of figure N14–11 reflects a slightly different approach to the oscillator power-supply problem. Although a twin triode is used, the average load on the dc supply is only 10 ma for an output of 100 μa at 7000 volts as compared to 25 ma for any of the pentode circuits shown used with the same output voltage and current and input voltage. Further, the unit will continue to operate with reduced but usable output should one of the twin-triode sections become inoperative. The reduced output will allow continued operation during a mission, but will alert the operator to the necessity for replacement of the tube at the first opportunity. The unit operates as a square-wave generator and at a lower frequency (approximately 700 cps) than any of the other audio oscillators (approximately 3 kc). The output capacitor in the filter is three times as large electrically, although not physically, as those capacitors used in the sine-wave units (.02 as opposed to .007). Although .007 is about one-third of .02, the space taken up by the case, terminals, etc. for high-voltage capacitors of this size is such that the physical size would differ by a factor of two rather than three. The need to keep the output impedance low rather than the need to reduce power-supply ripple will in many instances be the controlling factor in selection

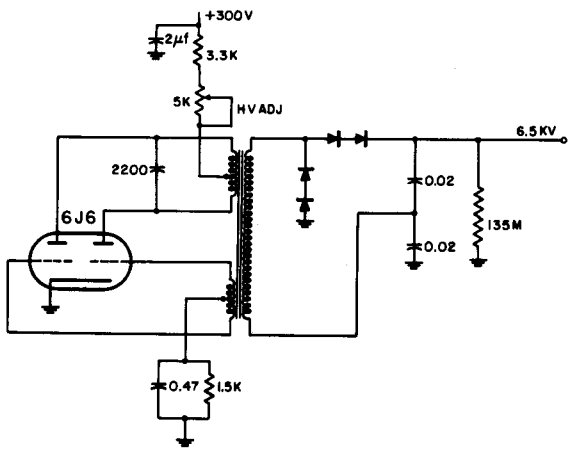


Figure N14–11—Twin-triode audio-frequency square-wave oscillator type supply with saturable square-loop core material

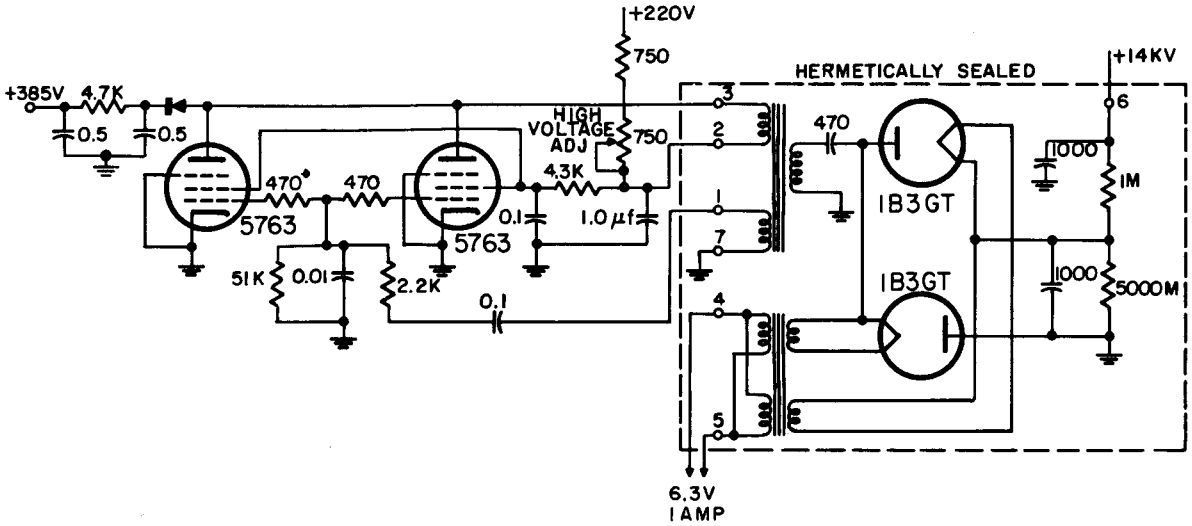


Figure N14–12—Pentode audio oscillator type supply for final anode of dark-trace tube

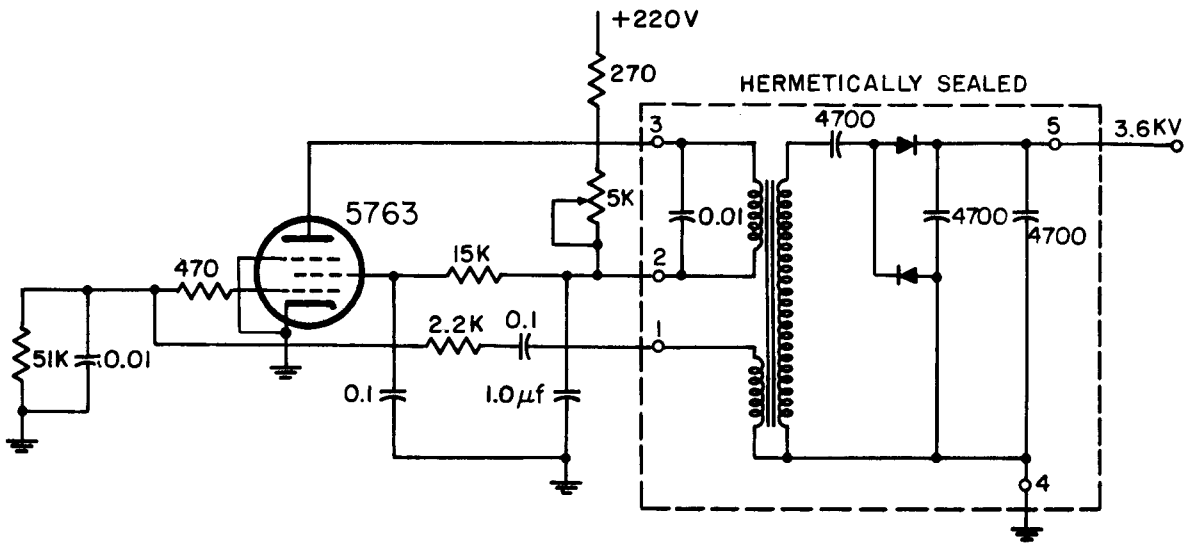


Figure N14–13—Pentode audio oscillator type supply for screen grid supply of dark-trace tube

of output capacitor size. Despite the larger output capacitor, the peak-to-peak ripple in the output voltage of this supply is slightly higher than that of the higher frequency supplies noted previously; however, the output impedance is lower. The operating efficiency of this unit, which is much higher than that of any of the units reviewed previously, results in low oscillator tube plate dissipation. Further, the constancy of output voltage with change in time and load is equal to or better than that of the sine-wave oscillators previously reviewed.

The circuits of figures N14–12 and N14–13 were used for the same dark-trace tube. Circuit N14–12 has two pentodes in parallel to provide sufficient power at 14 kv for the final anode potential; circuit N14–13 supplies 3.6 kv for the screen potential. These circuits are similar to the pentode oscillator circuits of figures N14–5 through N14–9. The application of circuits N14–12 and N14–13 is too specialized to include in the specifications for the preferred circuit.

14. 2 *Comparison of Pentode Oscillators with Twin-Triode Oscillators:* The survey of oscillator-type high-voltage crt power supplies indicated that the choice of circuit type for use as a preferred circuit lay between the single-pentode sine-wave oscillator and the twin-triode square-wave oscillator. Measurements were made on several oscillator-rectifier-filter units. Two of these units were selected as representative of their types for illustration and comparison.

The unit selected to illustrate the pentode oscillators of circuits N14–5 through N14–9 was that shown in figure N14–9. It was chosen because it operates from a supply voltage of 300 volts. The example of a twin-triode square-wave oscillator is shown in figure N14–11 and it too operates from a supply voltage of 300 volts. Thus, comparison of efficiency and economy of B+ current drain is simplified. The rectifier-filter-bleeder and transformer were, in every case, contained in a hermetically sealed enclosure. Because of this, it was necessary to compare a pentode oscillator using a high vacuum rectifier with a twin-triode oscillator using a selenium rectifier. The high vacuum rectifier tube filaments were heated by a winding taken off the high-voltage transformer. This, therefore, added an external load to the pentode oscillator which was not present when using the twin-triode oscillator. In order to equalize the comparison, one must deduct from the input power of the pentode oscillator the power needed to heat the rectifier filaments.

The two circuits were compared by adding external loads to each and measuring output voltage and input current of each as a function of output load current. The results of these measurements are shown in figures N14–14 and N14–15 for the pentode and twin-triode oscillators, respectively. The twin-triode oscil-

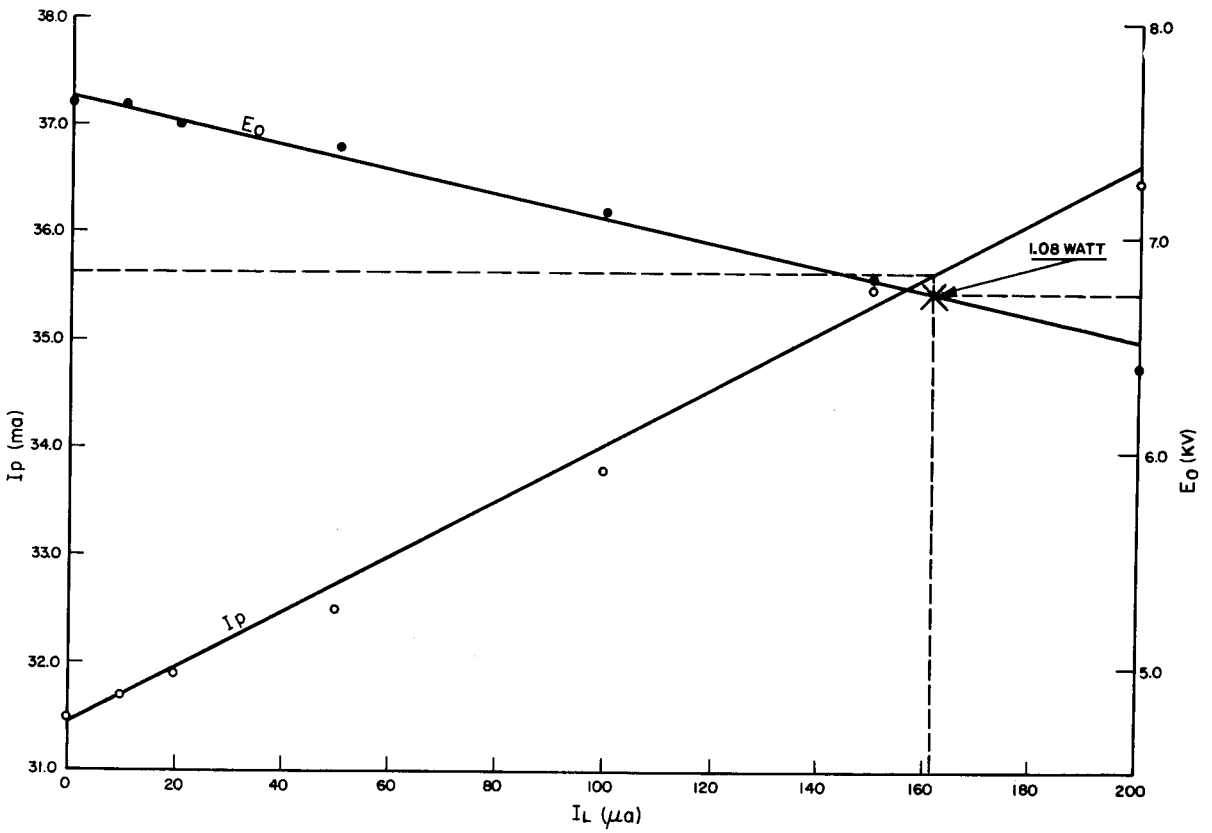


Figure N14–14—Variation of output voltage and input current, as a function of output current, for pentode audio-frequency sine-wave oscillator type supply

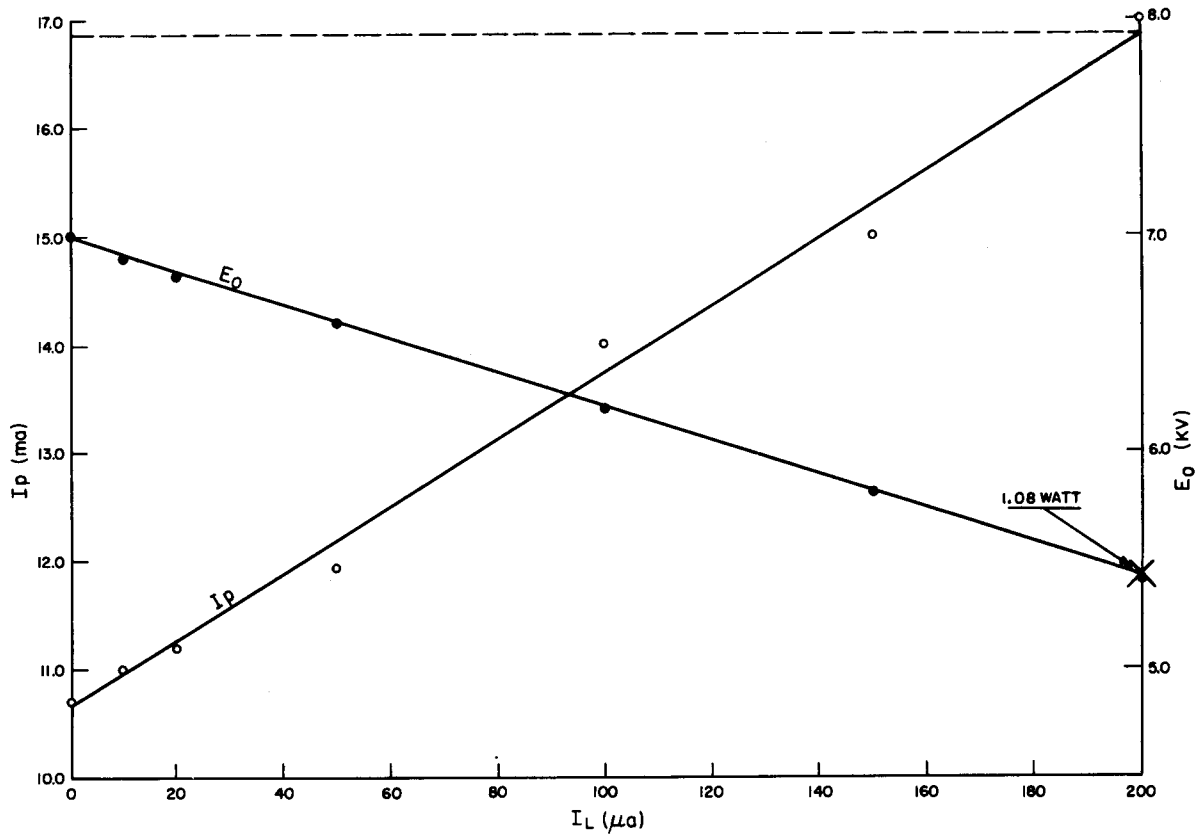


Figure N14–15—Variation of output voltage and input current, as a function of output current, for dual-triode audio-frequency square-wave type supply

lator curve has been corrected to compensate for the smaller power drain of its bleeder resistor. From the graphs a comparison can be made of the currents drawn by each of these oscillators when delivering identical power, approximately one watt, to their loads. The twin-triode oscillator draws 16.8 ma and appears more efficient than the pentode oscillator which draws 35.7 ma. However, one must subtract the power supplied by the pentode oscillator to its associated vacuum tube rectifier filaments. The heaters draw slightly less than ½ watt. Now if the loading on the output of the pentode oscillator unit were reduced by 60 μa, its loading would be reduced by approximately 0.42 watts if it were assumed that the output voltage was in the vicinity of 7 kv. It can now be seen from figure N14–14 that a change in output current of 60 μa will result in a change of input current of 1.5 ma. If this 1.5 ma of input current is subtracted from the 35.7 ma of input current used previously in comparing the two circuits, it can be seen that the ratio which remains is now 17 ma to 34.2 ma, which does not reduce the advantage of the twin-triode oscillator by a significant amount. Thus it is evident from what was noted above and from a comparison of the curves of figures N14–14 and N14–15 that the circuit of figure N14–11 is considerably more sparing of input power for the range of power output used with cathode ray tube display units than are the pentode circuits of figures N14–5 through N14–9.

14.3 *Choice of CRT Operating Voltages*:[1] [2] In the operation of electromagnetic cathode-ray

[1] Theodore Soller, Merle A. Starr, George E. Valley, Jr., *Cathode Ray Tube Displays*, Rad. Lab. Series, Volume 22, pp. 91, 92.

[2] U. S. Naval Air Development Center, Johnsville, Pa., Report No. NADC–EL–55100, Phase Report, Improvement of Radar Cathode Ray Tube Performance Using the Double Pulse Technique of Spot Size Measurement as a Criterion.

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tubes, high screen and final anode voltages are desirable from the standpoint of spot brightness and resolution. These voltages in turn determine the modulation characteristics of the tube, the sweep amplitude required, and the power required to drive the deflection coils. Although an increase in the screen voltage decreases the spot size, it also increases the cutoff bias of the tube and decreases the slope of the modulation characteristic so that a higher grid drive is necessary to obtain a given beam current. As the accelerating voltage is raised, the spot size decreases, but the power required to drive the deflecting coils increases proportionally. Further, at high accelerating voltages, the sweep length is more critical. If the beam is deflected beyond the edges of the screen, electrons that bounce off the sides and neck of the tube cause annoying back lighting. The desired light intensity at moderate beam currents can generally be achieved by careful selection of the screen and final anode voltages.

In a particular instance, a unit using a CRT screen grid voltage of 220 volts was found to operate unsatisfactorily. The spot size, being too large, caused operator eye fatigue. The unit was modified by increasing the screen grid voltage to 400 volts which was the maximum possible without also modifying the video drive. The decreased spot size was a noticeable improvement from the operator's standpoint.

14.4 *Preferred Voltages:* The voltages chosen for PC 6 were 7000 volts for the final anode, and 300 or 400 volts for the screen grid. The 7000 volt choice resulted from the equipment survey. The supply required to power the oscillator provides the 300 volts whenever the circuitry requires this potential. Four hundred volts is specifically provided as a separate tap on the high voltage bleeder, because it is the highest screen grid voltage that can be used with present video drive systems. Four hundred volts is the preferable screen grid voltage to use because the smaller spot size thereby achieved provides a clearer image and less operator eyestrain.

15. AIRBORNE FIRE CONTROL COMPUTER CIRCUITS

The fire control computer circuits starting with PC 70 are preferred vacuum tube circuits of sufficient variety to make possible the construction of an analog fire control computer in which potentiometers are used for multiplying and function forming.

15.1 *Basis of Selection:* These fire control computer circuits have been selected because they are the simplest which can be used repeatedly in computers designed to:

(1) Permit use of standard electronic component parts requiring no matching or trimming.

(2) Perform adequately under the environmental conditions specified for military service.

(3) Require no adjustment or calibration in service and a minimum of adjustment and calibration during manufacture.

(4) Use sufficient negative feedback to permit replacement of defective vacuum tubes and components without recalibration of the equipment, yet do not employ feedback of such magnitude that the danger of high-frequency oscillation can cause undue wiring, component, and layout difficulties.

15.2 *Detail Design and Construction Precautions:*

(*a*) Capacitors and resistors: In general, the circuits may be constructed using 200 volt dc rated capacitors and ½ watt composition resistors both with ±20% limits. Usually, composition resistors with a ±5% tolerance will stay within ±20% limits. When ratings other than those mentioned above apply, they are indicated on the preferred circuit page.

In some circuits capacitors must be shielded to avoid extraneous pickup. Grounded metal case types are recommended. These capacitors are identified in the schematic diagrams of the preferred circuits by a third connection, a ground connection to their shell. (See fig. N15–1.)

Decoupling and filtering networks are included in the schematic diagrams of the preferred circuits. When combinations of these circuits are operated together, the decoupling and filtering networks associated with the individual preferred circuits should be adequate, provided that low impedance power supplies are used.

Low frequency resonances in the power supply caused by the total inductance of the transformer and filter choke forming a parallel resonant circuit with the filter capacitor are especially troublesome in analog computer power supplies because low output impedance in the vicinity of dc is important. The power supply must be designed to minimize the amplitude of the low frequency peaks caused by these resonances. The output impedance must be so low that no combination of line voltage and load current changes can cause a ripple voltage greater than 2.5 volts rms. This figure includes the residual ripple of the rectifier and filter itself and the transient oscillations which can occur when low frequency load or line variations occur at the power supply resonant frequency.

These requirements can be met by use of a three-phase power supply of minimal complexity containing the following: silicon rectifiers, a well designed transformer, and a single-section filter having a low L/C ratio when operated from the 400 cycle supply of a typical military aircraft in which the voltage and frequency are maintained within 5% of their nominal values. Power supplies of this type with 1 volt rms steady state ripple and 2.5 volts rms ripple under the worst transient conditions have given satisfactory service.

(*b*) Tube types: The tube types indicated have given satisfactory service in numerous analog computer applications. Subminiature tubes are used where permissible. If all-miniature tubes are to be used, the 5718 can be replaced by one-half of a 5814A, the 6112 by the 5751, the 5840 by the 6AU6WA, and the 6021 by the 5670. These replacements require only minor changes in component values. In all cases, tubes conforming to the latest approved military specifications should be used.

(*c*) Wiring and layout: In typical fire control computers, circuit repetition is the rule; for example, one computer contained 10 motor controllers, 16 resolver drivers, and 5 low-gain preamplifiers. Such computers contain more than 100 tubes and by means of relays may be connected in several different configurations. These large electronic units require special precautions in wiring and layout not ordinarily

required for smaller conventional electronic equipments of 20 tubes or less.

(*d*) Ground system: Conductors large enough to make voltage drops negligible cannot be provided, especially in the ground circuits. Even if the chassis is used as a common ground, troublesome errors due to voltage drops can occur. A satisfactory grounding system can be obtained by dividing the grounds into three classes as follows:

Power ground: Those elements that are connected to the power ground include all components that draw current and are insensitive to the voltage drops in and electrical interactions caused by the grounding system. Such components are fans, servo motors, power amplifier stages, filament transformers, relays, etc.

Signal ground: Those elements that are connected to the signal ground include all components that draw current and require accurate voltages for computing purposes and/or those components sensitive to voltage drops in the grounding system due to high gain. Such components are reference transformers, computing potentiometers, low-level preamplifiers, etc. Component shields in high impedance signal circuits should also be connected to the signal ground. In such instances, care must be taken to insure that no extraneous connection is established between the signal ground and the ground system to which the other shields are connected.

Shielding and chassis ground: Elements that are returned to the chassis include those that draw no current and are used for shielding, such as cans for transformers and choppers, tube shields, capacitor cases, and braid used to shield wire, all of which would be difficult to isolate from the chassis.

These ground systems (power, signal, and shielding) must be connected together at one point and never more than one. It is best that they be wired completely independently and that an ohmmeter test be made to determine if they are entirely separate. Then, removable jumpers should be placed in the junction box to tie together the three grounds and the power supply returns.

Typical examples of the grouping of grounds are illustrated in figure N15–1. When this system of grounds is used, the large currents of the fans, servo motors, and power amplifiers do not flow in the signal ground wires, and the voltage drops in the signal grounds can be maintained at negligible levels with conductors of reasonable size. The schematic diagrams of the preferred circuits do not indicate the three types of grounds, however, as the division is determined by the computer size, type of construction, and other special requirements peculiar to an individual computer.

Two wire heater circuits should be used so that no heater current flows in the ground system of the chassis. The chassis should not be used for any grounds that carry current because protective coatings on the chassis often make for poor connections and large voltage drops. Also, as the chassis is attached to the airplane in more than one place, currents entirely foreign to the equipment may flow through the chassis. Currents through the

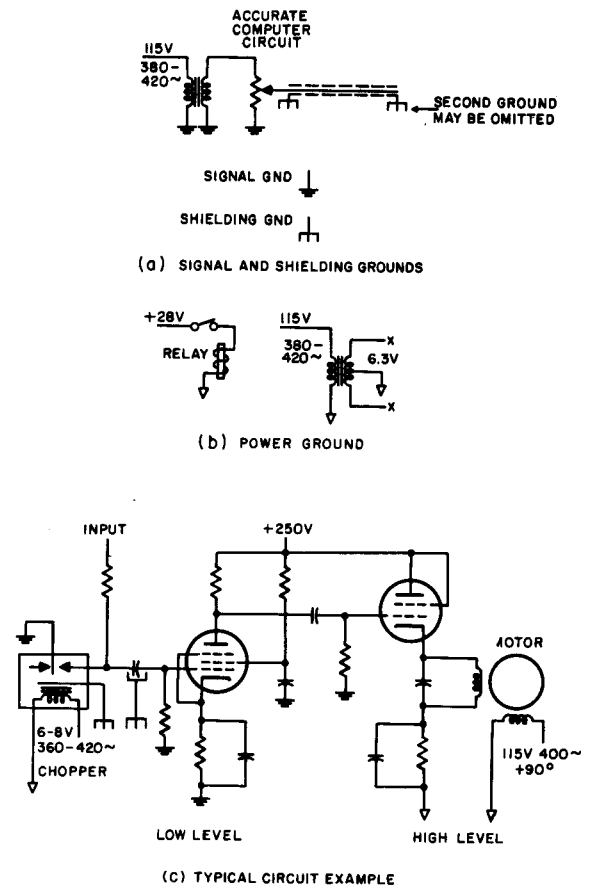

Figure N15–1—Examples of grounds

chassis may prevent the equipment from passing corrosion and salt-spray tests.

(*e*) Nulls: Poor nulls are sometimes encountered at the inputs of the servos in computers. Satisfactory nulls can be insured by minimizing extraneous pickup through the use of adequate shielding, moderate circuit impedance levels, and transformers with carefully controlled interwinding capacitance.

(*f*) Feedback: Most of the circuits in airborne computers employ large amounts of degenerative feedback to make the performance of the computer depend on a certain set of precision components and be as independent as possible of the remaining components which include vacuum tubes, motors, carbon resistors, etc. The complete problem of obtaining sufficient feedback with good stability cannot be adequately treated here.

15.3 *References:* An understanding of the material presented in the following publications is essential for successful application of the building block circuits presented here.

(1) H. Chestnut and R. W. Mayer, *Servomechanisms and Regulating System Designs* (2 vols.), John Wiley and Sons, Inc., New York, New York, 1951.

(2) J. G. Truxal, *Automatic Feedback Control System Synthesis*, McGraw-Hill Book Co., Inc., New York, New York, 1955.

(3) Korn and Korn, *Electronic Analog Computers*, McGraw-Hill Book Co., Inc., New York, New York, 1952.

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NAVAER 16-1-519

SUPPLEMENT NO. 1 (DATED AUG. 1, 1958) HANDBOOK PREFERRED CIRCUITS

INSTRUCTION SHEET

INSTRUCTIONS FOR INSERTING SHEETS DATED AUG. 1, 1958 IN HANDBOOK PREFERRED CIRCUITS AND REMOVING CORRECTED OR OBSOLETE SHEETS

REMOVE	INSERT
Table of Contents, p. xi, undated	Table of Contents, pp. xi and xii, dated Aug. 1, 1958.

PART 1. PREFERRED CIRCUITS MANUAL

PC 1, p. 1–2, undated	PC 1, p. 1–2, dated Aug. 1, 1958.[1]
PC 2, p. 2–2, undated	PC 2, p. 2–2, dated Aug. 1, 1958.[1]
PC 3A, p. 3–2, undated	PC 3A, p. 3–2, dated Aug. 1, 1958.[2]
PC 4, p. 4–2, undated	PC 4, p. 4–2, dated Aug. 1, 1958.[3]
PC 5, p. 5–2, undated	PC 5, p. 5–2, dated Aug. 1, 1958.[4]
	PC 6, pp. 6–2—6–7, dated Aug. 1, 1958.
	PC 7, pp. 7–2—7–8, dated Aug. 1, 1958.
	PC 8, pp. 8–2—8–7, dated Aug. 1, 1958.
	PC 53, pp. 53–2—53–17, dated Aug. 1, 1958.
	PC 70, p. 70–2, dated Aug. 1, 1958.
	PC 71, p. 71–2, dated Aug. 1, 1958.
	PC 72, p. 72–2, dated Aug. 1, 1958.
	PC 73, p. 73–2, dated Aug. 1, 1958.
	PC 74, pp. 74–2—74–11, dated Aug. 1, 1958.
	PC 201, pp. 201–2—201–5, dated Aug. 1, 1958.
	PC 202, pp. 202–2—202–8, dated Aug. 1, 1958.

PART 2. NOTES TO THE PREFERRED CIRCUITS MANUAL

13. Automatic Frequency Control, pp. N13–1—N13–10, dated Aug. 1, 1958.
14. High Voltage CRT Power Supplies, pp. N14–1—N14–8, dated Aug. 1, 1958.
15. Airborne Fire Control Computer Circuits, pp. N15–1—N15–2, dated Aug. 1, 1958.

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[1] The regulator tubes have been changed from type 5651 to 5651WA. It is important to use the 5651WA because its restricted voltage range allows adjustment with components operating at their extreme limits.

The term "limits" has been defined in the Notes on pp. 1–2 and 2–2.

[2] The center tap of transformer T1 is connected to a voltage divider across the regulated output, instead of to a voltage divider across the unregulated input as shown in the original circuit diagram.

The regulator tube has been changed from type 5651 to 5651WA.

The term "limits" has been defined in the Notes on p. 3–2.

[3] V4 has been changed to 5651WA. In the original circuit diagram, it was shown as 5651.

For clarity, the circuit diagram has been partially redrawn.

The limits of R19 have been corrected to read ±1%. In the original specifications, R19 was listed as having both ±1% and ±10% limits.

The limits of R7 and R8 have been changed from ±1% to ±2%.

The term "limits" has been defined in the Notes on p. 4–2.

[4] The value of R19 has been corrected to read 150K. The value of 100K shown on the original circuit diagram was an error in the drawing. The limits of R19 have been corrected to read ±1%. In the original specifications, R19 was listed as having both ±1% and ±10% limits.

The limits of R7 and R8 have been changed from ±1% to ±2%.

V4 has been changed to 5651WA. In the original circuit diagram it was shown as 5651.

For clarity, the circuit diagram has been partially redrawn.

The term "limits" has been defined in the Notes on p. 5–2.

16. CRYSTAL OSCILLATORS

Crystal oscillators are used as sources of stable signals. They are also used in frequency synthesis systems of electronic communications and test equipment. In these systems, crystal oscillators are usually associated with frequency multipliers and mixers. The frequency stability of such oscillators is generally measured in parts per million, whereas stability measurements for frequency standards are in parts in 10^8 or 10^9.

There are two basic types of crystal oscillators:[1] the type whose frequencies of oscillation are dependent upon the antiresonant or high-impedance properties of the crystal and the type dependent upon the series resonant or low-impedance properties of the crystal. The former type is usually restricted to frequencies below 20 mc, while the latter is useful up to frequencies of 100 mc and higher.

The circuits discussed here will be limited to those operating in the antiresonant mode in the frequency range from 0.8 to 20 mc.

16.1 *Examples of Oscillator Circuits in Current Use:* A total of 27 equipments, 16 Air Force and 11 Navy, were surveyed to determine the most commonly used oscillator circuits and their performance requirements. Sixty-nine oscillators were used in the 27 equipments. The basic types and the number of each type used are listed below.

Cathode Coupled	23
Colpitts	15
Electron-Coupled Colpitts	15
Pierce	6
Electron-Coupled Pierce	2
Miller	2
Electron-Coupled Miller	1
Transformer Coupled	1
Quintuplex	1
Grounded Plate Hartley	3

The first three types comprise more than 75% of the total. Essentially, all military oscillator requirements can be met by use of these three types. Certain design changes may be necessary to meet special requirements. These design changes will be discussed later.

16.2 *Characteristics of Piezoelectric Crystal Units:* The equivalent circuit of a piezoelectric quartz crystal is characterized by a series *RLC* combination shunted by C_o, the holder static capacitance. For this type of network, there are two frequencies at which the reactance becomes zero. The lower frequency is called the series resonant frequency and the crystal impedance is low. The higher frequency is called the anti- or parallel-resonant frequency, where the crystal acts as a high impedance.

In practical oscillator circuits, the antiresonant crystal is associated with a load capacitance, and the crystal equivalent circuit is inductive, forming a parallel resonant circuit at a frequency slightly less than that of the antiresonant frequency of the crystal alone. The impedance of this arrangement is high.

In the frequency range of the Preferred Circuits (PC 101 and 102), the crystals used are of the thickness shear mode of oscillation and oscillate in the fundamental mode.

16.3 *Description of Various Oscillator Circuit Types:* An analysis and description of the more common types of antiresonant oscillators listed in section 16.1 are given below. A more detailed analysis is presented for those types chosen as preferred circuits.

(*a*) Pierce oscillator: The Pierce oscillator, shown schematically in figure N16-1, is an antiresonant type. The equivalent crystal reactance is inductive and forms a tuned tank circuit with the series combination of C_g and C_p in parallel with C_{pg}. The capacitance presented to the crystal is called the load

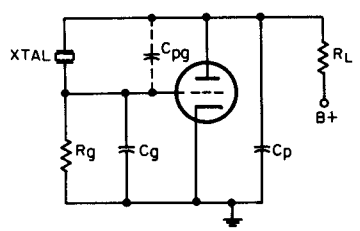


Figure N16-1.—Pierce oscillator.

[1] William A. Edson, *Vacuum-Tube Oscillators*, John Wiley & Sons, New York, N.Y., 1953, pp. 197–226.

capacitance, C_t. The output is developed across the load resistor, R_L. With an untuned load, the output voltage is low, but frequency changes can be accomplished by simply switching crystals on a plug-in basis. For operation at a single frequency, the output may be tuned, resulting in voltage levels considerably greater than those for the untuned output. The circuit is not critical in operation and will oscillate with variations in external circuit component values. The oscillator requires a minimum number of circuit components.

(*b*) Miller oscillator: The Miller oscillator circuit schematic is shown in figure N16–2. Although the operating frequency is more dependent on plate tuning conditions than is that of the Pierce, and the circuit is more complex in design, this oscillator is widely used, since the output voltage is larger than that of the Pierce. The load capacitance of the crystal is a function of C_g, C_{pg}, L_p, and frequency. The frequency dependence precludes use of the oscillator at more than a single frequency on a crystal plug-in basis. Instead, a tuning adjustment is required for operation at a new frequency. Generally, this is accomplished by using a variable capacitor or inductor in the plate circuit. The plate tank is tuned to a frequency above that of the crystal so that the plate impedance will appear inductive, and thus provide the proper phase condition for oscillation. Since C_{pg} is small for pentode tubes, use of this type of tube normally requires the addition of a small capacitor from plate to grid.

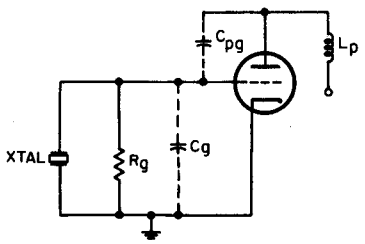


Figure N16–2.—Miller oscillator.

(*c*) Colpitts oscillator: The Colpitts, or grounded plate Pierce, circuit is shown in figure N16–3. The plate is ac grounded and the output voltage is developed between cathode and ground. The feedback voltage is developed across the grid cathode portion, C2, of the capacitive voltage divider C2, C3. Grid bias is developed on positive voltage peaks when the grid conducts and charges the grid ground capacitance C1. R_g acts as a grid leak and together with C1 performs an amplitude regulating function. The capacitance across the crystal, together with that of the voltage divider, provides the required capacitive load for the crystal. The antiresonant tank is composed of this load capacitance and the equivalent inductance of the crystal.

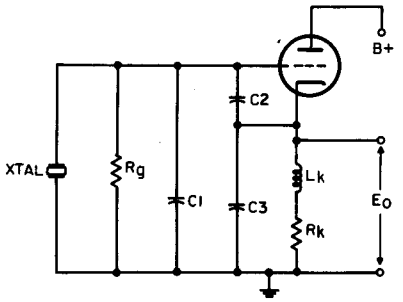


Figure N16–3.—Colpitts oscillator.

If C1 of figure N16–3 is kept constant, and the ratio of C3/C2 is changed to keep the total capacitance looking out from the crystal terminals constant at 32 $\mu\mu$f, then the voltage amplitude across the crystal and the voltage amplitude across the load will vary as shown in figure N16–4.[2] These voltage amplitudes have been normalized with respect to the maximum voltage across the crystal. The measured quantities are shown as dashed lines, and the computed quantities are shown as solid lines. In the computed case the factor due to grid loading was neglected. This factor effectively reduces the C3/C2 ratio, and a higher output results. The measured data does not go below a ratio of 1.0 because the output load and distributed capacitances make a value less than 1.0 impractical. The broken line curve shows the change in parts per million of the output frequency as a function of capacitance ratio for a 10% change in supply voltage. This is a measure of the stability of the circuit, since a decrease in transconductance with tube life will tend to change the plate resistance of the tube in the same direction

[2] H. E. Gruen, "How to Design Colpitts Crystal Oscillators," Electronics, January 1, 1957.

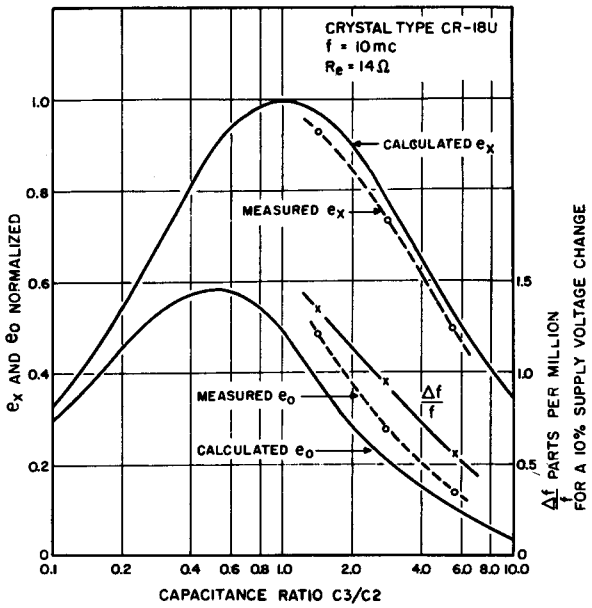


Figure N16-4.—Circuit performance, $\Delta f/f$, vs. capacitance ratio, C3/C2, for total capacitance $C_t = 32$ μμf. (e_x is the voltage across the crystal; e_o is the output voltage.)

as a decrease in supply voltage. This change in plate resistance will be translated into a change in output frequency.

(*d*) Electron-coupled oscillators: The oscillators described in the preceding sections (a) through (c) are all adaptable to electron coupling. Generally, the oscillators as given utilize triode tube sections. For electron coupling, pentodes are used.

The most commonly used electron-coupled pentode is the electron-coupled Colpitts oscillator (see list in section 16.1). The pertinent circuit parameters of this oscillator are shown in figure N16-5. The load is well isolated from the oscillator portion of the circuit, and the load circuit is readily adjustable to obtain harmonics of the crystal frequency.

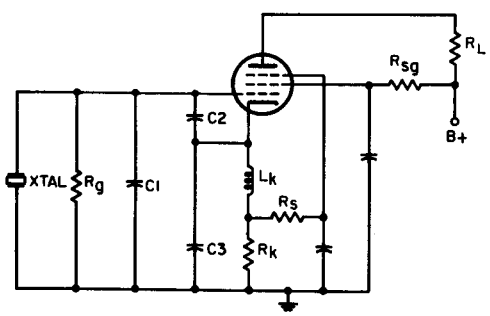


Figure N16-5.—Electron-coupled Colpitts oscillator

Pentode tube types having internal suppressor-to-cathode connections are not the most desirable types for electron-coupled circuits, since the capacitance from plate to cathode allows coupling external to the electron stream. Use of a pentode with an external suppressor lead allows grounding of the suppressor by a capacitor. The suppressor-to-cathode dc potential may be maintained substantially at zero by returning the suppressor through a resistor (R_s) to the junction of the cathode inductor (L_k) and the cathode bias resistor (R_k).

16.4 *Criteria for the Selection of the Preferred Circuits:* The factors influencing the selection of Preferred Circuits 101 and 102 are discussed below.

(*a*) Selection of PC 101: The primary advantage of the Colpitts oscillator is circuit simplicity. Output is fair over the range of crystal resistances specified by MIL-C-3098B. Frequency change is accomplished by utilizing crystals on a plug-in basis. From an operational standpoint, the Colpitts and Pierce oscillators are similar, but the former circuit offers greater advantage when operation over a range of frequencies is required.

In the Colpitts design, only adjustments for proper load capacitance and capacitance ratio values are necessary. These adjustments are made by measuring the grid-to-cathode, cathode-to-ground, and grid-to-ground capacitances and adding physical capacitors to obtain the desired values of each. For most military type crystals, the load capacitance, C_t, is 32 ± 0.5 μμf, which is the value used in PC 101.

Although the Miller circuit produces higher output voltage than do the Colpitts or Pierce circuits, it has the disadvantage of requiring a tuning adjustment, which must be accurately set for each operating frequency. Its frequency is also more sensitive to changes in load impedance. Comparison of the characteristics and information on usage of these circuits formed the basis for selection of the Colpitts oscillator as a preferred circuit for low frequency operation where a reliable circuit providing reasonable output into low to medium impedance loads is required.

(*b*) Selection of PC 102: The electron-coupled Colpitts oscillator has advantages similar to those of the Colpitts circuit, plus the desirable characteristics of isolating the effects of load impedance changes from the oscillator portion of the circuit. Harmonics of the crystal frequency may be obtained by tuning the plate circuit for the desired frequency. Tuning is accomplished by adjusting the plate tank to obtain a maximum output voltage at the desired frequency, be it fundamental or harmonic. Changes in fundamental frequency are made on a crystal plug-in basis, as in the Colpitts. The electron-coupled Colpitts oscillator produces nearly as high a voltage as the Miller, and can be made almost completely independent of loading effects. It was thus selected for a preferred circuit to provide a stable fundamental or harmonic signal for use in control and synthesis systems.

April 1, 1959

U.S. GOVERNMENT PRINTING OFFICE : 1959 O—502632

SUPPLEMENT NO. 2 (DATED APRIL 1, 1959) HANDBOOK PREFERRED CIRCUITS

INSTRUCTION SHEET

INSTRUCTIONS FOR INSERTING SHEETS DATED APRIL 1, 1959 IN HANDBOOK PREFERRED CIRCUITS AND REMOVING INCORRECT OR OBSOLETE SHEETS

REMOVE	INSERT
Table of Contents, pp. xi and xii, dated Aug. 1, 1958.	Table of Contents, pp. xi and xii, dated April 1, 1959.

PART 1. PREFERRED CIRCUITS MANUAL

PC 79, pp. 79-2—79-9, dated April 1, 1959.
PC 101, pp. 101-2—101-9, dated April 1, 1959.
PC 102, pp. 102-2—102-10, dated April 1, 1959.
PC 250, pp. 250-2—250-6, dated April 1, 1959.
PC 251, pp. 251-2—251-4, dated April 1, 1959.

PART 2. NOTES TO THE PREFERRED CIRCUITS MANUAL

16. Crystal Oscillators, pp. N16-1—N16-4, dated April 1, 1959.

POWER SUPPLY VOLTAGES FOR TRANSISTORS

A supplement to MIL-STD-706,* which will include regulated power supply voltages for transistors, is under consideration. The voltages which appear most likely to be adopted are 1.5, 3, 6, 12, 25, 50, and 100 volts, positive or negative. These are the power supply voltages which are used in the transistor circuits in this manual.

*MIL-STD-706, 23 December 1958, establishes nominal values for regulated direct current power supply voltages within the range of 100 to 500 volts for use in military electronic equipment. This standard provides in part as follows: "Nominal values of all regulated direct current voltages within the range of 100 to 500 volts, positive or negative, shall be selected from the following list: 100 volts, 150 volts, 250 volts, 300 volts, and 450 volts."

17. TRANSISTOR DIGITAL LOGIC CIRCUITS

17.1 *General:* Preferred Circuits 210 through 216 are a compatible set of transistor digital logic circuits for use in computer, control, and communication equipment. These circuits were designed to operate and were tested over a temperature range of −30 to +60° C and at repetition rates up to 150 kc, which is the maximum repetition rate at which the preferred digital logic circuits will operate under maximum load and worst operating conditions (limit transistors, limit resistors, limit voltage-supply magnitude, limit temperature). When tandem-connected logic circuit chains are interconnected through feedback chains, signals should not be introduced into a circuit before it has recovered from a previous signal input. Timing charts must be drawn for each logic circuit loop, therefore, to make certain that this does not occur. For example, the time interval between the introduction of a signal into the trigger input of a binary counter chain and the sampling of the output must be sufficiently long to allow settling of the last stage of the counter prior to the sampling.

The terms "logic" and "logical" are used in connection with circuits that perform the basic functions of AND, OR, inversion, delay, and storage.[1] These are the basic functions of a digital computer, or of the binary operations of data processing, control, and communication systems. The source of the terms "logic" and "logical" is Boolean algebra, which was originally developed as a mathematical analysis of logic, but has been applied to notating and improving assemblages of the basic functions of digital computers. In the set of preferred circuits, PC 210 performs the general purpose AND, OR, and inversion function. PC 211 performs a special purpose AND function. PC 212 performs the storage function, and PC 213 performs the delay function. PC 214, 215, and 216 are auxiliary circuits used in conjunction with the logic circuits. PC 214 reconstitutes pulses which have deteriorated in the course of passage through a chain of logical circuits, and is used in conjunction with the time delay to provide a standard pulse output from that circuit. PC 215 is a power amplifier used to permit a circuit of restricted load capability to drive a multitude of other logic circuits. PC 216 is an indicator.

17.2 *Power Supplies:* Voltages of +6, −6, and −18 volts are required for operation of the set of compatible digital logic circuits. The −18 volt supply is made by connecting the positive side of a 12-volt floating source to the negative side of the −6 volt supply. This arrangement prevents flow of current in the reverse direction through the −6 volt supply. Such reverse current flow can occur, for example, when the transistor of PC 210 is cut off and the −18 volt potential is supplied by a separate source. Here, positive current will flow from ground, up through the −6 volt supply, then through the collector resistor of Q1 and into the negative terminal of the −18 volt supply, and back to ground. If, however, the −18 volt potential is derived from a floating 12-volt supply which is connected in series with the −6-volt supply, the current will flow from the positive side of the 12-volt supply, through the collector resistor of Q1 and into the negative terminal of the 12-volt supply. Thus, no current (neglecting I_{CBO}) will flow through the −6 volt supply.

Preferred Circuits 210 through 216 are designed to operate from a supply which does not vary more than ±10% from the nominal values of −6 volts, −18 volts, and +6 volts. The noise level of the −6 volt supply is restricted by the characteristics of the bistable multivibrator and can be no greater than 1.7 volts in peak magnitude if spurious triggering is to be prevented.

As a general rule, digital circuits such as PC 210–216 are packaged into counters, shift registers, and groups of gates. Insertion of a 50 μf capacitor between the −6 volt supply and ground, for every group of 10 packages which average 4 circuits per package, will serve to keep the noise level within limits. In addition, bypass capacitors must be spotted along the

[1] R. K. Richards, *Digital Computer Components and Circuits*, D. Van Nostrand Inc., New York, 1957, pp. 64, 65.

power distribution lines to filter out transient noise. A disturbance such as that induced by the starting of a fluorescent desk lamp can cause voltages as high as 4 or 5 volts with respect to ground at frequencies in the 10 mc range. Such pulses of noise will trigger a sensitive flip-flop and cause an error. To filter out such noise, 0.4 μf extended-foil polystyrene capacitors can be used. These capacitors should be spotted along the power distribution lines for every group of ten 4-circuit packages. For larger or smaller packages, the linear distribution should be proportioned to achieve the same amount of filtering. The above rules are general. For any given installation, the filtering requirement should be determined by checking the distribution points of the power-supply leads with an oscilloscope. A high-frequency oscilloscope should be used, because of the possibility of outside interference in the 10 mc range.

In computer and data processing equipment, hundreds of transistors may be installed in a single equipment bay. The current flow can exceed 20 amperes in the steady state, and variational currents of amperes can flow at a given time. This large variational current flow gives rise to a difference of potential along the ground bus which may be of sufficient amplitude to cause an equipment error. General precautions to observe in laying out grounds are:

1. Use flat strip conductors to decrease lead inductance.
2. Use a fanning out of ground distribution, i.e., where possible run each circuit or circuit group common ground directly to the ground bus.
3. Run these intermediate ground busses to a main ground bus with an increased size comparable to the number of intermediate busses joining it.
4. To check the adequacy of the ground system, use a high frequency oscilloscope with its ground connected to the central ground point or to a point on the main ground bus, and run the oscilloscope probe along the main and intermediate ground busses. The magnitude of the voltage transients along the bus caused by variational currents flowing in the bus will serve as an indication of the effectiveness of the ground system.

17.3 *Loads:* The input impedance and maximum output load for each circuit of this series are given in terms of "F" and "G" loads in order to simplify the loading rules. The equivalent circuits of these loads are shown in figure N17–1. The actual input impedance may vary somewhat from the equivalent circuit describing it; however, allowances were made for this in formulating the output loading rules for each circuit. The basic criterion in the determination of maximum circuit loading is the allowable rise time.

(a) *"F" Load:* The "F" load is derived from the input impedance of the bistable multivibrator, PC 212. An RC approximation of this input impedance is less accurate than that of the "G" load because of the transistor loading at the junction of the capacitor and resistor. The two forms of the "F" load represent the possibility of coupling capacitively or resistively into the flip-flop input.

(b) *"G" Load:* The "G" load is derived from the input impedance of the general purpose NOR gate, PC 210.

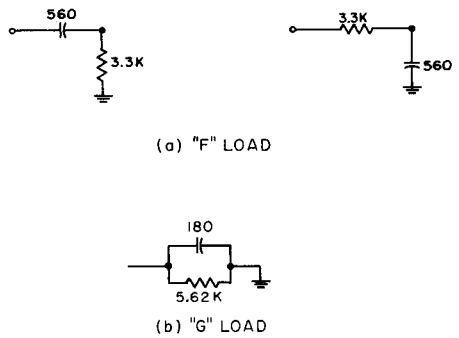


Figure N17–1.—Equivalent circuits of loads and input impedances.

17.4 *Pulses and Levels:* The terms "pulse(s)" and "level(s)" are used in the descriptions of the preferred digital circuits. A level may be thought of as a steady-state signal which is used to gate a pulse-type signal. In many cases the steady-state signal is the output signal from a switching array, and the pulse transforms this signal to a type of binary digit representation that can be used to acuate a flip-flop

or other binary storage device. The information is sometimes viewed as being in the pulse and sometimes as being in the steady-state signal, but the functioning of the circuit is the same. In a sense, both signals contain information regardless of the application, even when one of the signals, usually the pulse, is applied in a continuous repetitive fashion in the form of a "clock pulse." [2]

Pulses with positive-going leading edges are referenced to −6.2 volts (+10%), and pulses with negative-going leading edges are referenced to ground. The pulse with a negative-going leading edge occurs at a transistor output when a PNP transistor is switched from on to off; a pulse with a positive-going leading edge occurs when a PNP transistor is switched from off to on. The pulses have a minimum width of 0.8 μsec at an amplitude of 50% of maximum with a leading edge rise time [3] of 0.2 μsec or less.

17.5 *Definitions of Terms:* Special terms used in PC 210 through 216 are defined below.

(*a*) *AND gate:* A gate whose output is energized when and only when every input is in its prescribed state.[4]

(*b*) *Binary cell:* An elementary unit of storage which can be placed in either of two stable states.[4] (In the text of the preferred circuits, such a unit is represented by the bistable multivibrator, PC 212.)

(*c*) *Clear:* To restore a storage or memory device to a prescribed state, usually that denoting zero.[4] (See also Reset.)

(*d*) *Delay time:* The time required for the collector voltage to complete the first 10% of its total change when a switching transistor is turned on. It is measured from the instant that the signal applied to the transistor to turn it on completes 10% of its amplitude change. This definition, which is used in preferred circuits 210 through 216, permits the delay time to be determined by measuring circuit voltages. It is derived from the basic definition of delay time found in the General Specification for Semiconductor Devices, MIL-S-19500B, which refers to the semiconductor itself and reads: "the delay time of a pulse is the time interval from a point at which the leading edge of the input pulse has risen to 10 percent of its maximum amplitude to a point at which the leading edge of the output pulse has risen to 10 percent of its maximum amplitude." The input and output pulses referred to in this basic definition are current pulses, which are not easily measured in the preferred circuits.

(*e*) *Fall time:* The time taken for the trailing edge of a pulse to decay from 90% to 10% of its steady state amplitude. In preferred circuits 210 through 216 the fall time is determined by measurement of the voltage waveform.

(In computer terminology, fall time is often defined in terms of the fall of the current in the collector circuit of the transistor. The computer definition may refer either to the leading or the trailing edge of the output voltage waveform. When referring to the output of a normally ON transistor, it would apply to the leading edge of the voltage waveform, but when referring to the pulse output of a normally OFF transistor, it would apply to the trailing edge.)

(*f*) *Inhibit:* To apply a biasing potential to a diode gate in such a direction as to increase its resistance to the flow of current in the forward direction.

(*g*) *Level:* A level, as contrasted with a pulse, is a signal of relatively long existence in a given state ("1" or "0"). Levels are dc coupled and are used to prime or inhibit the gating logic and the diode gates which control the multivibrator input. The levels are always fed to the multivibrators through the resistor input of the diode gates. The minimum duration of a level is 5 μsec. (See also section 17.4.)

(*h*) *Logical "1":* A level represented by a voltage of −6.2 volts ±10% (−6 volts ±10% plus the drop of −0.2 volts across the clamping diode used in all the circuits) with respect to ground potential.

(*i*) *Logical "0":* A level represented by a voltage which has a potential of approximately zero volts (maximum −0.15 volts, the approximate drop across the emitter-collector terminals of a saturated transistor) with respect to ground potential.

[2] Ibid., p. 55.

[3] See definition of rise time, section 17.5.

[4] IRE Standards on Electronic Computers, Proc. IRE, Vol. 44, No. 9, September, 1956, pp. 1166-1173.

(*j*) *NOR gate:* A gate which is capable of operating either as an AND gate or as an OR gate.

(*k*) *On to Off and Off to On:* The action of a transistor in being switched from a conductive to a non-conductive state and vice versa respectively.

(*l*) *OR gate:* A gate whose output is energized when any one or more of the inputs is in its prescribed state.

(*m*) *Prime:* To apply a biasing potential to a diode gate in such a direction as to facilitate the flow of current through it in the forward direction.

(*n*) *Register:* A device capable of retaining information. (See PC 212, section 4.2.)

(*o*) *Reset:* To restore a storage device to a prescribed state. Also, to place a binary cell in the initial or "zero" state.[5] (See also Clear.)

(*p*) *Rise time:* The time taken for the leading edge of a pulse to rise from 10% to 90% of its final magnitude. This definition is independent of the polarity of the pulse. (See also Fall time.)

(*q*) *Set:* To place a storage device in a prescribed state. Also, to place a binary cell in the "one" state.[5]

(*r*) *Shift:* Displacement of an ordered set of characters one or more places to the left or right.[5]

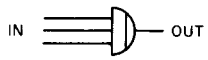
(*s*) *Storage time:* The time required for the collector voltage to complete the first 10% of its total change when a switching transistor is turned off. It is measured from the instant that the signal applied to the transistor to turn it off completes 10% of its amplitude change. (See also Fall time.)

17.6 *Symbols:*

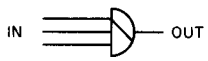
(a) Pulse:

(b) Level:

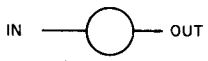
(c) AND Gate:



(d) OR Gate:



(e) Inverter:



[5] Ibid.

U.S. GOVERNMENT PRINTING OFFICE: 1960 O—548679

NAVWEPS 16-1-519

SUPPLEMENT NO. 3 (DATED APRIL 1, 1960) HANDBOOK PREFERRED CIRCUITS INSTRUCTION SHEET

INSTRUCTIONS FOR INSERTING SHEETS DATED APRIL 1, 1960 IN HANDBOOK PREFERRED CIRCUITS AND REMOVING INCORRECT OR OBSOLETE SHEETS

REMOVE	INSERT
Introduction, p. vii, undated, and Organization of the Manual and Directions for Use, p. ix, undated.	Introduction, pp. vii—ix, dated April 1, 1960.
Table of Contents, pp. xi and xii, dated April 1, 1959.	Table of Contents, pp. xi and xii, dated April 1, 1960.

PART 1. PREFERRED CIRCUITS MANUAL

Half-title page reading: "PART 1, PREFERRED CIRCUITS MANUAL". (Reverse side is page 1–2)	After Table of Contents, insert half-title page reading: "PART 1, PREFERRED CIRCUITS MANUAL, A. VACUUM-TUBE CIRCUITS". (Reserve side is blank)
PC 4, p. 4–2, dated Aug. 1, 1958	Half-title page reading: "NBS PREFERRED CIRCUIT NO. 1, DC REGULATOR FOR POSITIVE OUTPUT 150 VOLTS". (Reverse side is page 1–2.)
	PC 4, p. 4–2, dated April 1, 1960
	PC 78, pp. 78–2—78–4, dated April 1, 1960. (Insert after PC 74 issued in Supplement 1.)
	After PC 102 (issued in Supplement 2), insert half-title sheet reading: "B. TRANSISTOR CIRCUITS"
	PC 210, pp. 210–2—210–7, dated April 1, 1960.
	PC 211, pp. 211–2—211–6, dated April 1, 1960.
	PC 212, pp. 212–2—212–12, dated April 1, 1960.
	PC 213, pp. 213–2—213–9, dated April 1, 1960.
	PC 214, pp. 214–2—214–8, dated April 1, 1960.
	PC 215, pp. 215–2—215–8, dated April 1, 1960.
	PC 216, pp. 216–2—216–3, dated April 1, 1960. (Insert PC 210—216 after PC 202, issued in Supplement 1.)
	PC 252, pp. 252–2—252–8, dated April 1, 1960.
	PC 253, pp. 253–2—253–7, dated April 1, 1960. (Insert PC 252 and 253 after PC 251, issued in Supplement 2.)

PART 2. NOTES TO THE PREFERRED CIRCUITS MANUAL

17. Transistor Digital Logic Circuits, pp. N17–1—N17–4, dated April 1, 1960.

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[1] In the schematic diagram of the circuit dated Aug. 1, 1958, the connections to the plates of V5 were interchanged. The new schematic diagram corrects this mistake.

PEN AND INK CHANGES

PC 202:

Transistor type 2N387 which was used in PC 202, Transistorized 7 KV CRT Power Supply (issued in Supplement 1), has been dropped from the MIL preferred list. In PC 202 the 2N387 can be replaced by the 2N174. Note that although the two transistors are electrically similar, they are not mechanically interchangeable.

The following pen and ink changes should be made in PC 202:

Page 202–2: On the preferred circuit schematic diagram, change the transistor type from 2N387 to 2N174.

Page 202–3, section 2.2, first line: Change "2N387" to "2N174".

Page 202–6, second column, first sentence beginning on second line to semicolon on 4th line: Change "The 2N387 has a rated input impedance of 60 ohms, but this is in series with a 180-ohm resistor;" to "The 2N174 has an input impedance which is small compared to the 180-ohm resistor in series with its base;"

Page 202–8, figure 202–8: Change the transistor type from 2N387 to 2N174.

Page N2–8: The equations for $K_1^{2/3}$ and $K_2^{2/3}$ in the right hand column should read as follows:

$$K_1^{2/3}=\frac{(0.15)^{2/3}}{135-(2.4)(0.15)(250)}=6.27\times10^{-3}$$

$$K_2^{2/3}=\frac{(0.1)^{2/3}}{135-(3.6)(0.1)(250)}=4.8\times10^{-3}$$

The equation for $K_1^{2/3}$ was erroneously changed in the errata sheet of June 22, 1956. The equation for $K_2^{2/3}$ was correctly changed in the errata sheet of April 1, 1959 (Supplement No. 2) but the error in the previous errata sheet was not corrected.